



US00D956707S

(12) **United States Design Patent**
Yamauchi

(10) **Patent No.:** **US D956,707 S**
(45) **Date of Patent:** **** Jul. 5, 2022**

(54) **CIRCUIT BOARD**
(71) Applicant: **LAPIS Semiconductor Co., Ltd.**,
Yokohama (JP)
(72) Inventor: **Shigeki Yamauchi**, Yokohama (JP)
(73) Assignee: **LAPIS SEMICONDUCTOR CO., LTD.**,
Yokohama (JP)
(**) Term: **15 Years**

D471,524 S * 3/2003 Ebihara D13/182
D547,371 S * 7/2007 Miller D19/1
D552,098 S * 10/2007 Nishizawa D14/436
D603,812 S * 11/2009 Johnson D13/182
7,864,540 B2 * 1/2011 Takiar H01L 24/97
361/737
D637,193 S * 5/2011 Andre D14/436
D669,478 S * 10/2012 Lepp D14/436
D669,479 S * 10/2012 Lepp D14/436
D673,921 S * 1/2013 Ozawa D13/182
D673,922 S * 1/2013 Moriai D13/182
D681,640 S * 5/2013 Aoki D14/436
D690,672 S * 10/2013 Yoshida D13/182

(Continued)

(21) Appl. No.: **29/729,267**

(22) Filed: **Mar. 25, 2020**

(30) **Foreign Application Priority Data**

Sep. 26, 2019 (JP) 2019-21604
Sep. 26, 2019 (JP) 2019-21605
Sep. 26, 2019 (JP) 2019-21606

(51) **LOC (13) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182; 361/748, 752, 760, 761, 807,
361/808, 736, 719, 720; 174/250, 253,
174/255, 68.1; 363/144, 147
CPC H05K 3/30; H05K 3/301; H05K 3/284;
H05K 3/303; H05K 1/18; H05K 1/181;
H05K 1/182; H05K 1/183; H05K 1/185;
H05K 1/00; H05K 7/1417; H05K 7/02;
H05K 7/12; H05K 7/06; H01L 2924/14
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

D273,582 S * 4/1984 Bolt D13/182
D273,860 S * 5/1984 Bolt D13/182
D459,706 S * 7/2002 Ebihara D13/182
D466,093 S * 11/2002 Ebihara D13/182
D471,167 S * 3/2003 Ebihara D13/182

FOREIGN PATENT DOCUMENTS

KR 30-0605883 7/2011

OTHER PUBLICATIONS

Japanese Office Action dated May 12, 2020, for related Japanese Appln. No. 2019-021606 4 Pages.

Primary Examiner — Elizabeth J Oswecki
(74) *Attorney, Agent, or Firm* — Brooks Kushman P.C.

(57) **CLAIM**

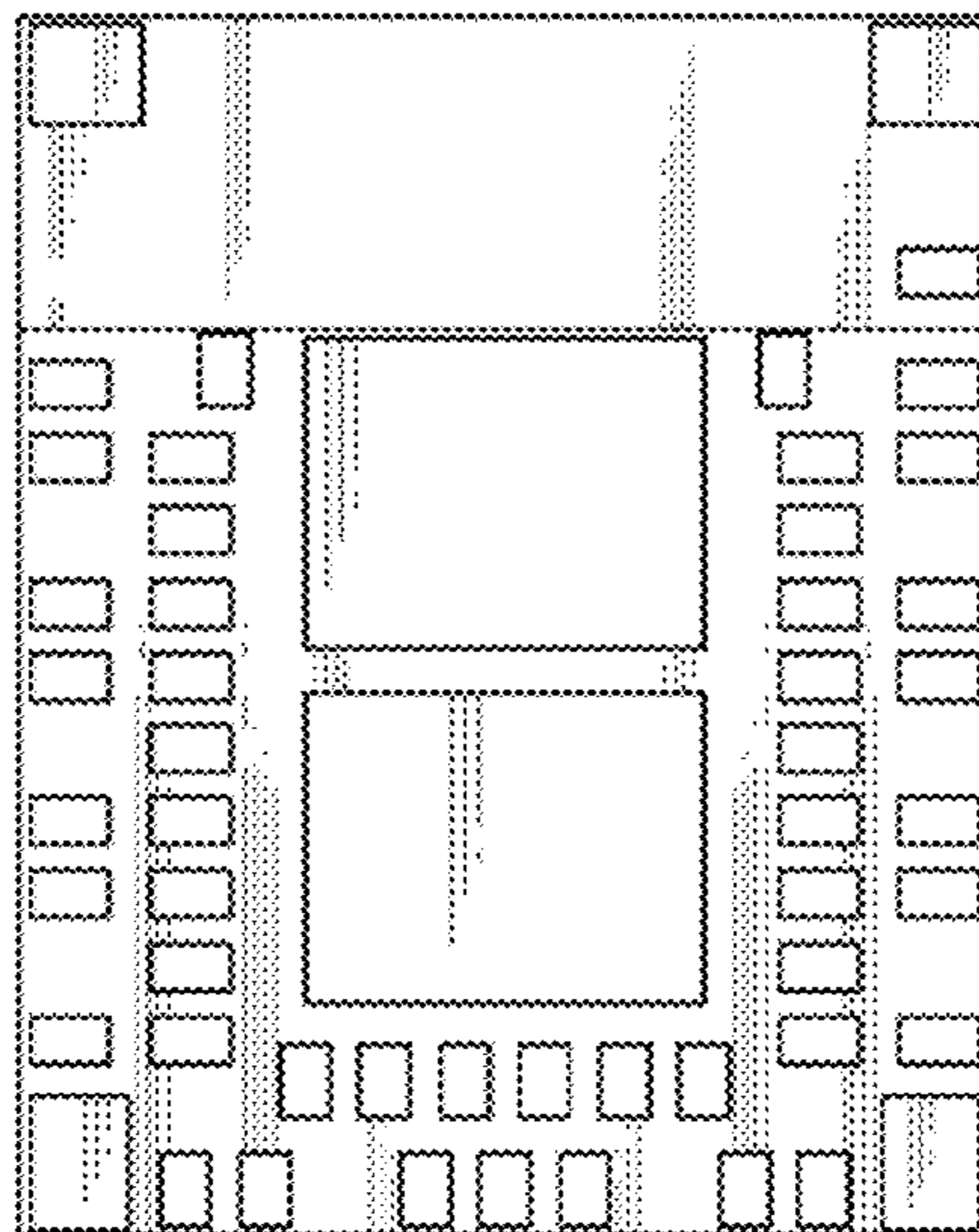
The ornamental design for a circuit board, as shown and described.

DESCRIPTION

FIG. 1 is a front view of a circuit board showing my new design;
FIG. 2 is a rear view thereof;
FIG. 3 is a right side view thereof;
FIG. 4 is a left side view thereof;
FIG. 5 is a top view thereof; and,
FIG. 6 is a bottom view thereof.

Throughout the drawings, the dash-dash broken lines are for the purpose of illustrating environment only and form no part of the claimed design.

1 Claim, 2 Drawing Sheets



(56)

References Cited

U.S. PATENT DOCUMENTS

D699,201 S *	2/2014	Petsch	D13/182	D814,473 S *	4/2018	Kadonaga	D14/436
D734,756 S *	7/2015	Stone	D14/436	D821,339 S *	6/2018	McCurley	D13/182
D735,203 S *	7/2015	Kim	D14/436	D831,009 S *	10/2018	Horn	D14/230
D735,204 S *	7/2015	Kim	D14/436	D837,171 S *	1/2019	Vasoya	D13/182
D735,962 S *	8/2015	Cruz	D34/38	D848,432 S *	5/2019	Lim	D14/436
D736,212 S *	8/2015	Kang	D14/436	D856,948 S *	8/2019	Vasoya	D13/182
D736,213 S *	8/2015	Kang	D14/436	D864,968 S *	10/2019	Beals	D14/436
D736,216 S *	8/2015	Kang	D14/436	D869,469 S *	12/2019	Lim	D14/436
D739,856 S *	9/2015	Kang	D14/436	D869,470 S *	12/2019	Lim	D14/436
D755,163 S *	5/2016	Yokoyama	D14/230	10,510,626 B2 *	12/2019	Braun	H01L 22/30
D757,015 S *	5/2016	Amit	D14/435	D872,032 S *	1/2020	Morelli	D13/147
D759,022 S *	6/2016	Beals	D14/436	D872,033 S *	1/2020	Morelli	D13/147
D768,115 S *	10/2016	Kazanchian	D14/230	D892,774 S *	8/2020	Sudo	D14/230
D772,232 S *	11/2016	Cho	D14/436	D893,439 S *	8/2020	Vasoya	D13/182
D775,092 S *	12/2016	Vinciarelli	D13/182	D902,164 S *	11/2020	Kondo	D13/182
D783,621 S *	4/2017	Lee	D14/436	2003/0081387 A1 *	5/2003	Schulz	H05K 1/117 361/728
D813,182 S *	3/2018	Imai	D13/182	2006/0097374 A1 *	5/2006	Egawa	H01L 24/05 257/686
				2017/0034941 A1 *	2/2017	McCurley	H05K 7/1417

* cited by examiner



Fig-1



Fig-2



Fig-3

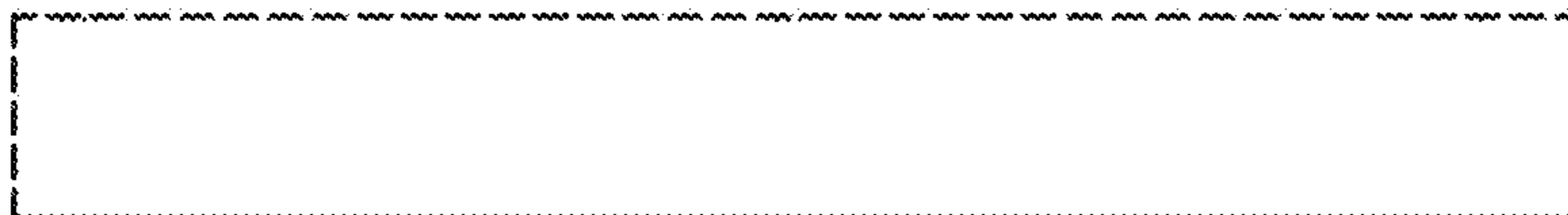


Fig-4



Fig-5

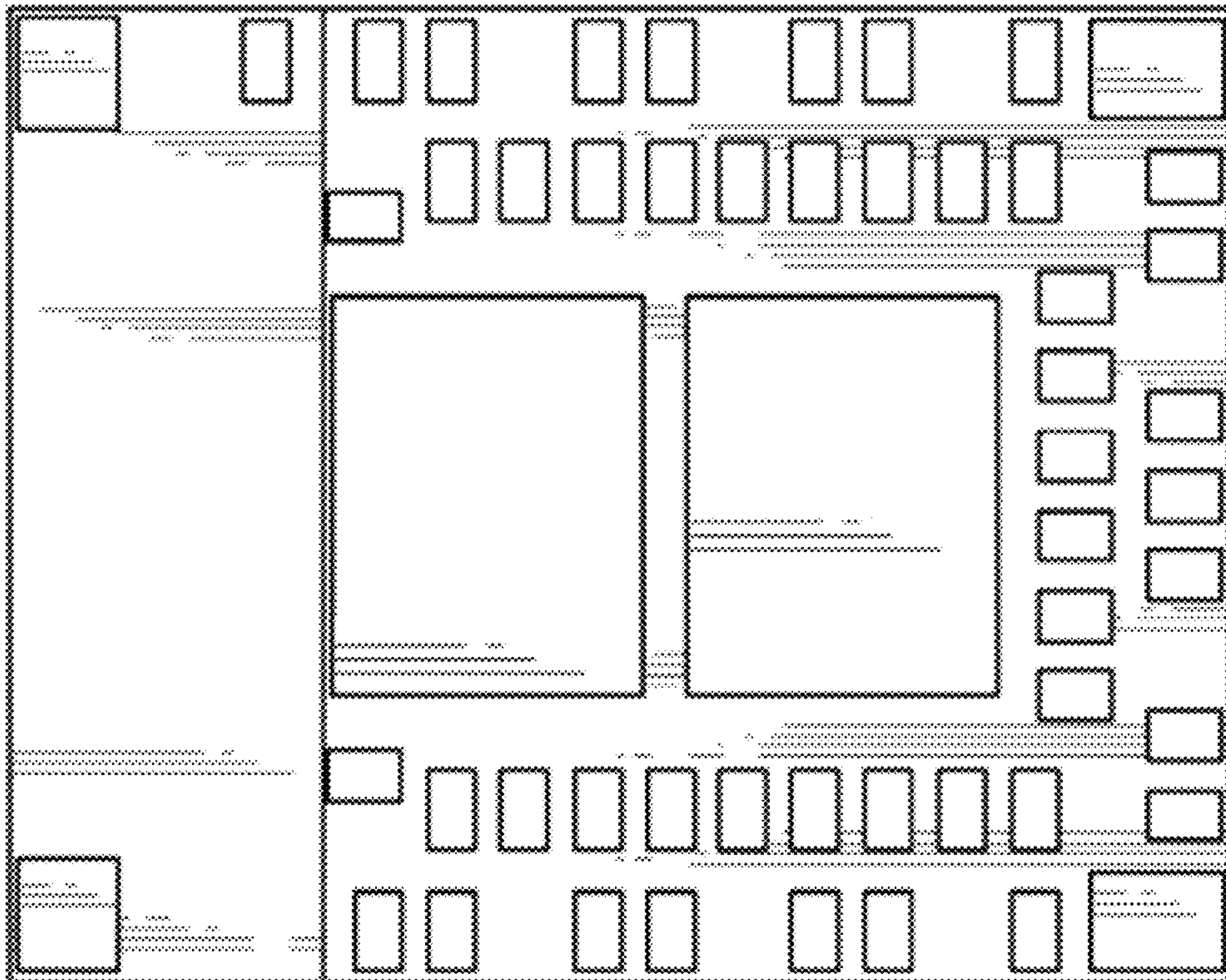


Fig-6