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(12) **United States Design Patent** (10) **Patent No.: US D951,214 S**
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(54) **SEMICONDUCTOR DEVICE**

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(*) Notice: This patent is subject to a terminal disclaimer.

(**) Term: **15 Years**

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(30) **Foreign Application Priority Data**

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(51) **LOC (13) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/123, 133, 146, 147, 158, 182, 184, D13/199
CPC .. H05K 1/18; H05K 7/00; H05K 7/20; H02M 7/00; H01L 25/07; H01L 25/16; H01L 25/18; H01L 23/00; H01L 23/31
See application file for complete search history.

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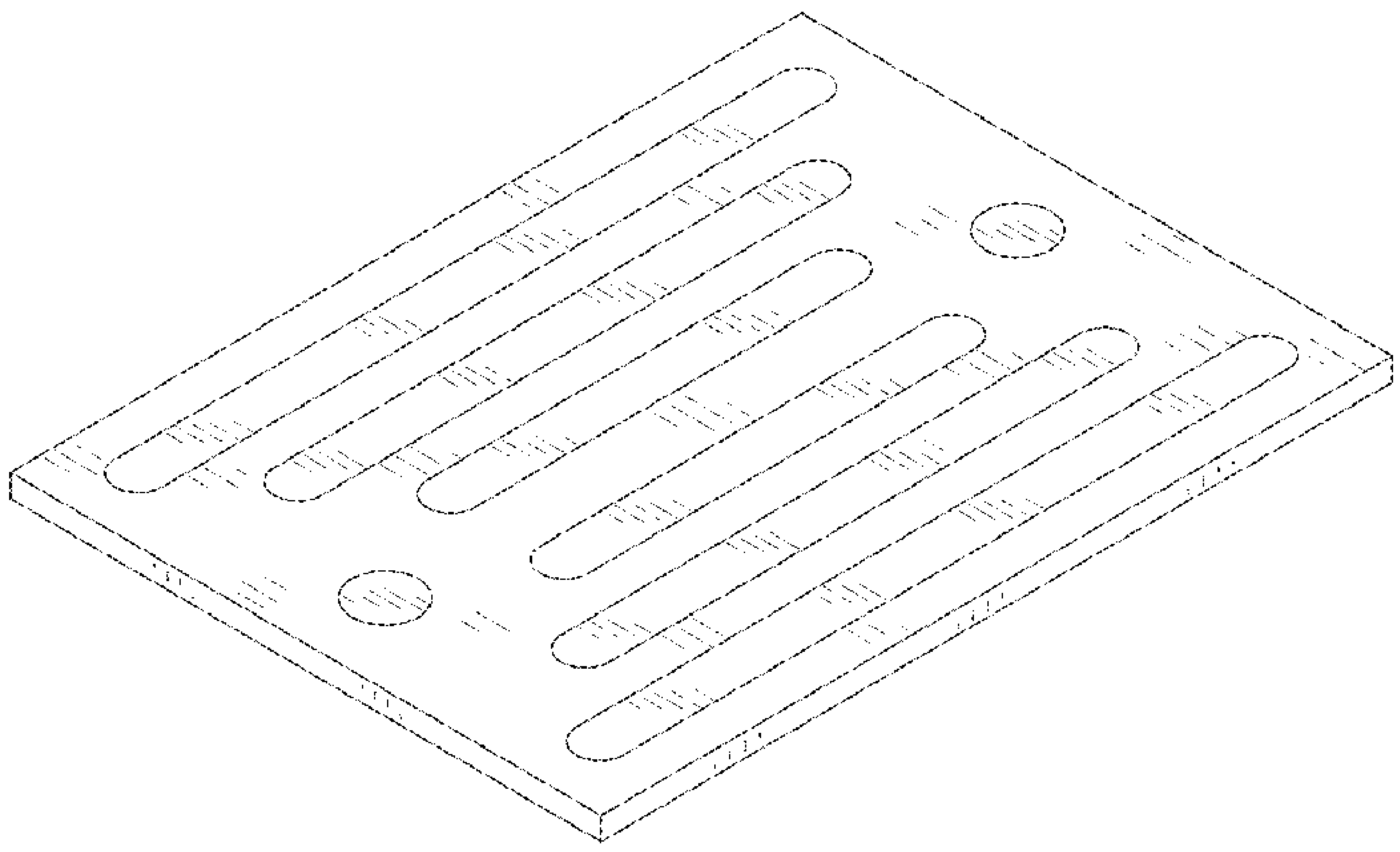
(57) **CLAIM**

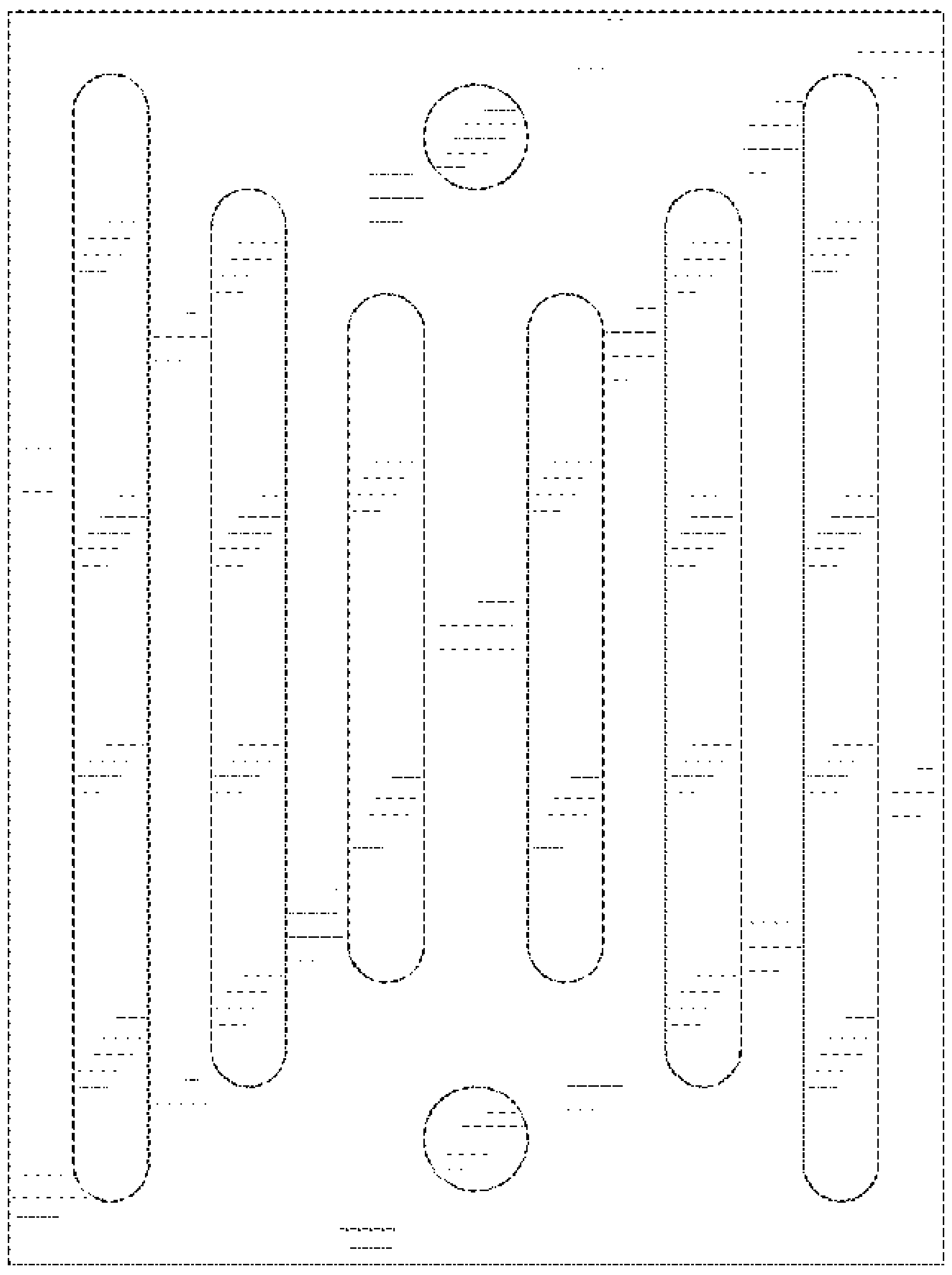
We claim the ornamental design for a semiconductor device, as shown and described.

DESCRIPTION

FIG. **1** is a front perspective view of a semiconductor device showing our new design;
FIG. **2** is a front view thereof;
FIG. **3** is a rear view thereof;
FIG. **4** is a left side view thereof;
FIG. **5** is a right side view thereof;
FIG. **6** is a top plan view thereof; and,
FIG. **7** is a bottom view thereof.

1 Claim, 7 Drawing Sheets





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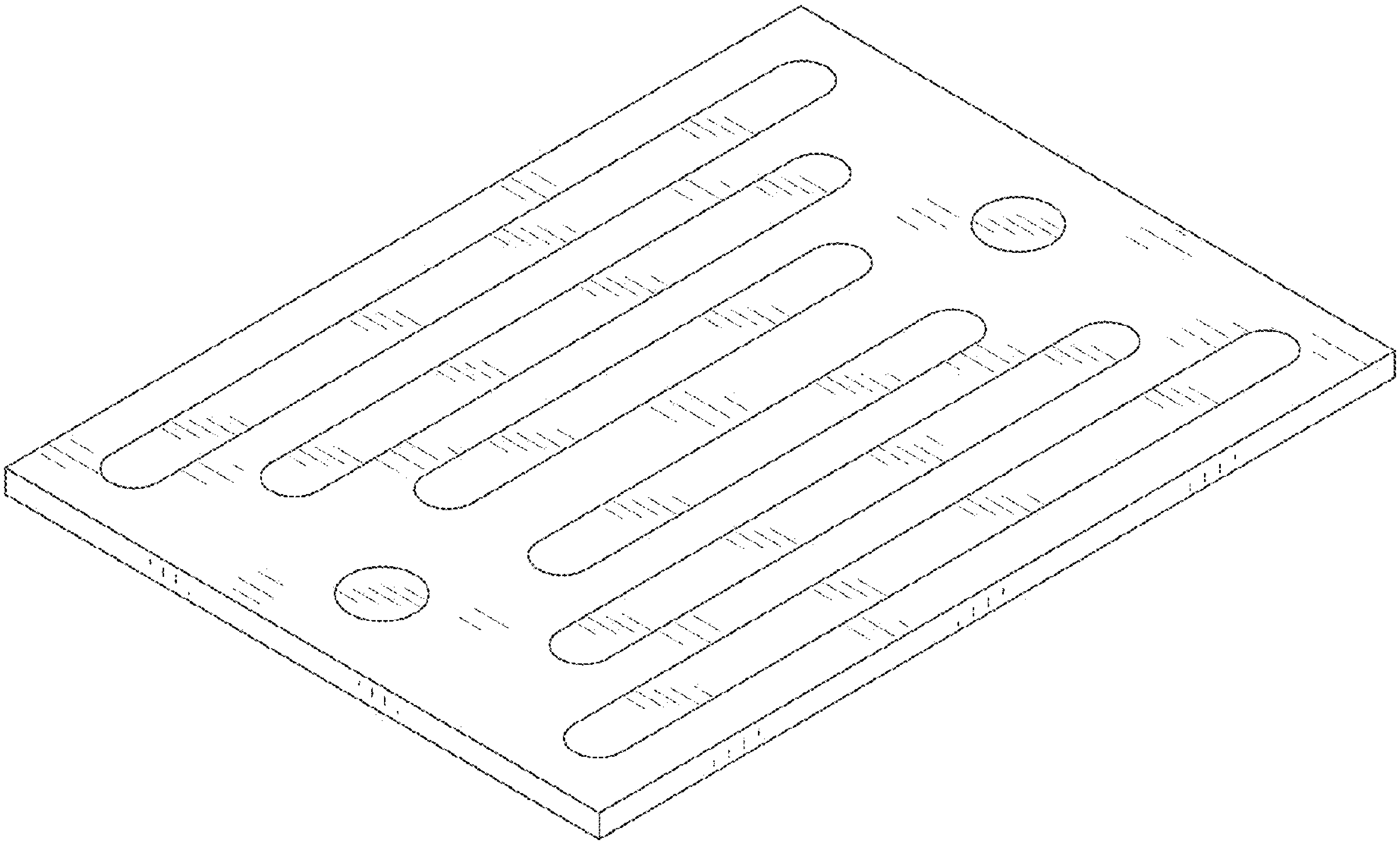

FIG.1

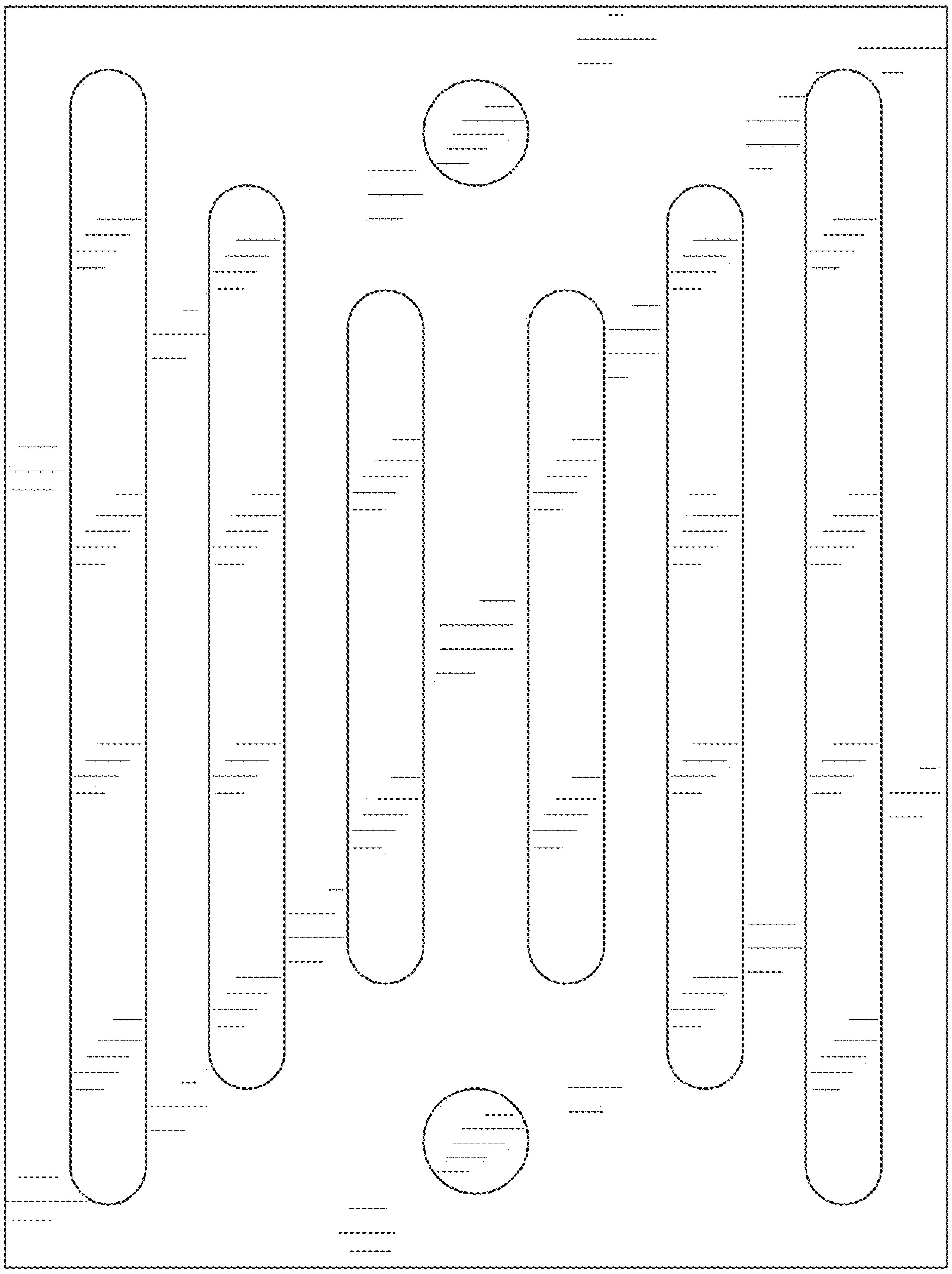

FIG. 2

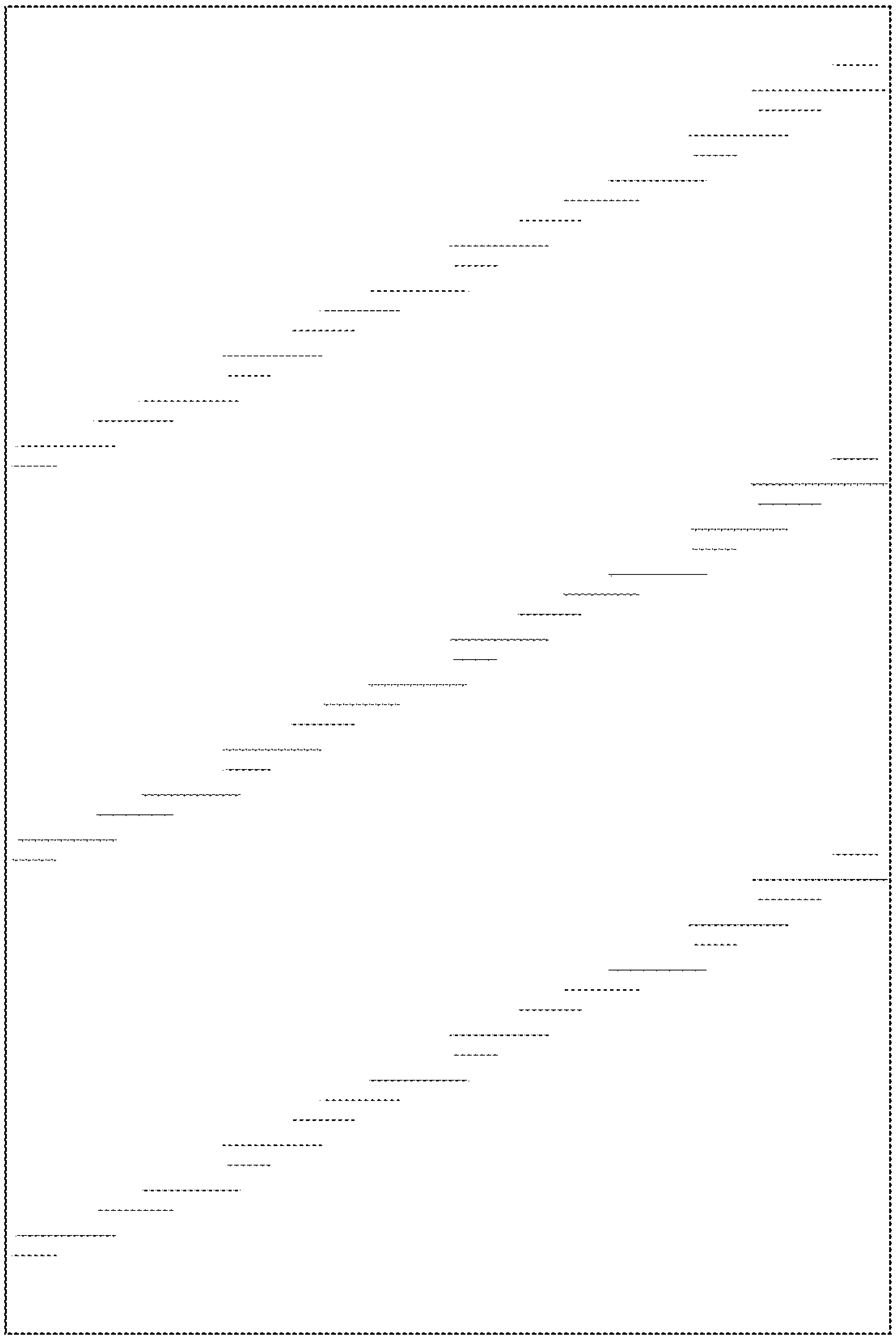

FIG.3

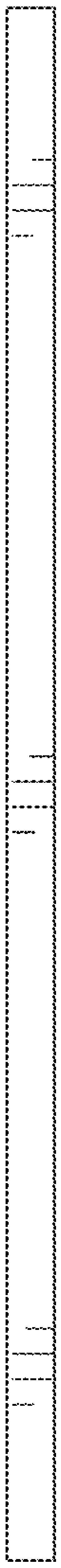

FIG.4

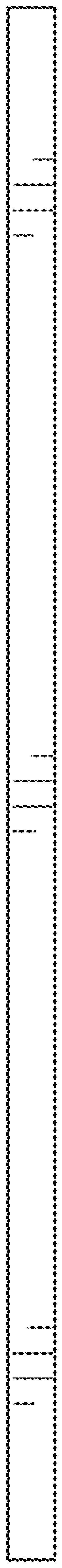

FIG.5

FIG.6

FIG.7