US00D949788S

(12) United States Design Patent

Sakamura et al.

(10) Patent No.: US D949,788 S
(45) Date of Patent: ** Apr. 26, 2022

(54) **SIGNAL INPUT AND OUTPUT CONVERTER**

(71) Applicant: **SMC CORPORATION**, Tokyo (JP)

(72) Inventors: **Naoki Sakamura**, Nagareyama (JP); **Takanori Saito**, Tsukubamirai (JP)

(73) Assignee: **SMC CORPORATION**, Tokyo (JP)

(**) Term: **15 Years**

(21) Appl. No.: **29/774,736**

(22) Filed: **Mar. 18, 2021**

Related U.S. Application Data

(62) Division of application No. 29/663,969, filed on Sep. 20, 2018, now Pat. No. Des. 920,909.

(30) **Foreign Application Priority Data**

Apr. 25, 2018 (CN) 201830175957.9

(51) **LOC (13) Cl.** **13-02**

(52) **U.S. Cl.**
USPC **D13/110**; D13/123

(58) **Field of Classification Search**
USPC D13/110, 123, 146, 147; D14/355, 357, D14/358, 433, 434
CPC G05F 3/04; G05F 3/06; G05F 3/08; G05F 3/10; H02M 7/003; H02M 7/06; H02P 27/04; H02P 27/047; H02P 27/06
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,020,149	A	5/1991	Hemmie	
D432,987	S	10/2000	Seo et al.	
D433,998	S	11/2000	Ishitsuka et al.	
D448,344	S	9/2001	Ishitsuka et al.	
D467,543	S	12/2002	Sakasegawa	
7,352,573	B2	4/2008	Wong	
7,397,668	B2	7/2008	Sekine et al.	
D597,027	S	7/2009	Tanabe et al.	
D729,171	S *	5/2015	Dietel	D13/147
D736,713	S	8/2015	Sekine et al.	
D737,765	S	9/2015	Sekine et al.	
D744,956	S *	12/2015	Sekine	D13/147
D747,690	S *	1/2016	Andersson	D13/147
D788,701	S	6/2017	Goto et al.	
D837,152	S *	1/2019	Wegerer	D13/110
D920,909	S *	6/2021	Sakamura	D13/110
D938,357	S *	12/2021	Aki	D13/123
2007/0133150	A1	6/2007	Sekine et al.	

* cited by examiner

Primary Examiner — Selina Sikder

(74) *Attorney, Agent, or Firm* — Birch, Stewart, Kolasch & Birch, LLP

(57) **CLAIM**

The ornamental design for a signal input and output converter, as shown and described.

DESCRIPTION

FIG. **1** is a front, top and left side perspective view of a signal input and output converter showing our new design;
FIG. **2** is a front, top and right side perspective view thereof;
FIG. **3** is a rear, bottom and right side perspective view thereof;
FIG. **4** is a rear, bottom and left side perspective view thereof;
FIG. **5** is a front view thereof;
FIG. **6** is a rear view thereof;
FIG. **7** is a top plan view thereof;
FIG. **8** is a bottom plan view thereof;
FIG. **9** is a left side view thereof; and,
FIG. **10** is a right side view thereof.
The broken lines depict portions of the signal input and output converter that form no part of the claimed design.

1 Claim, 10 Drawing Sheets

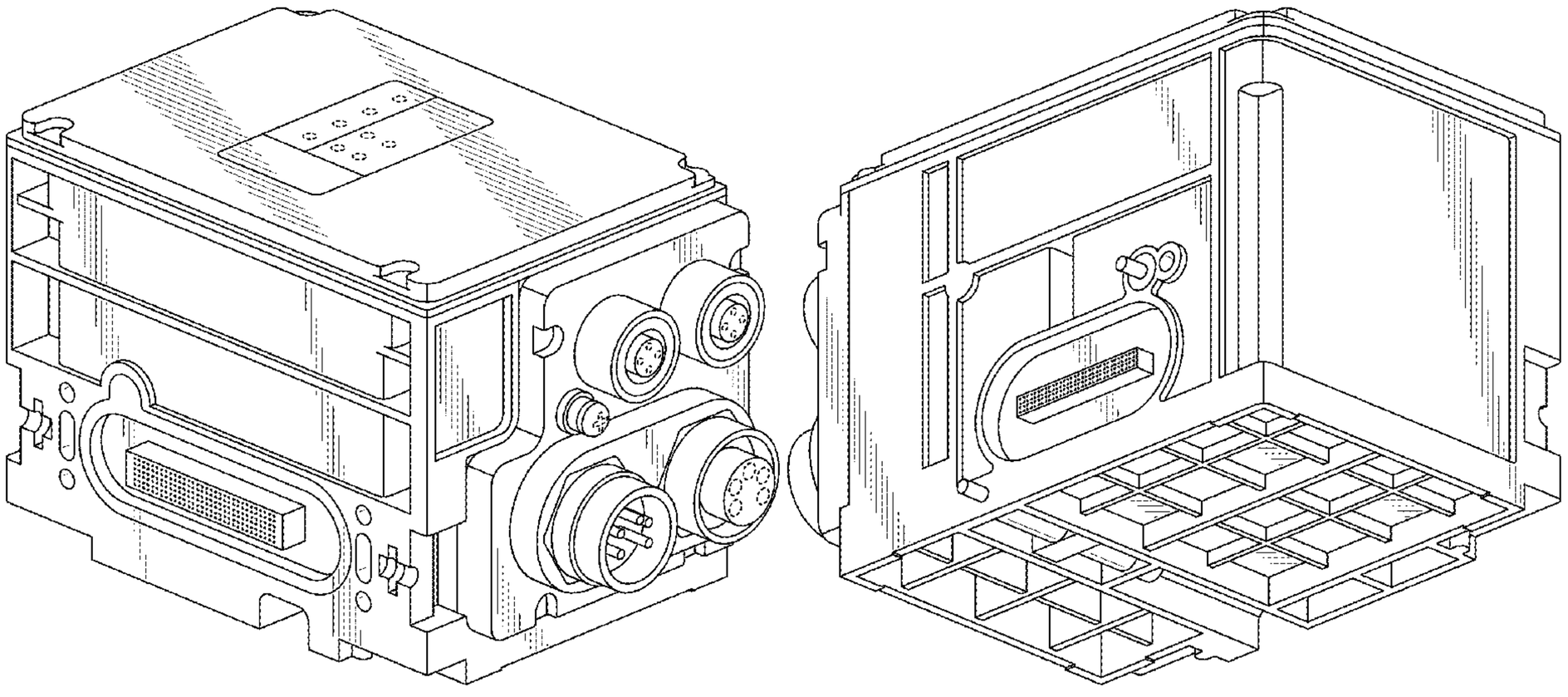

FIG. 1

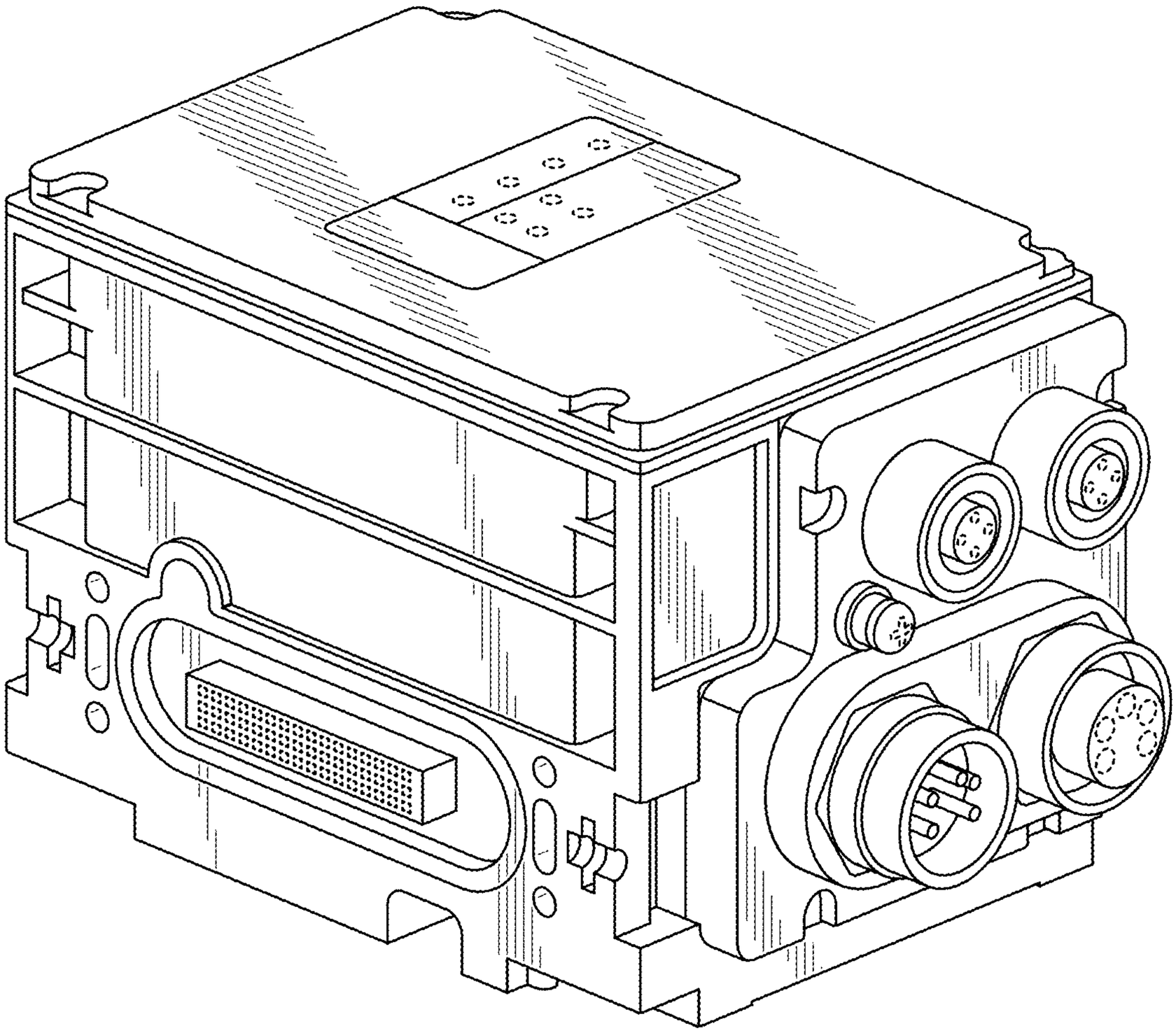

FIG. 2

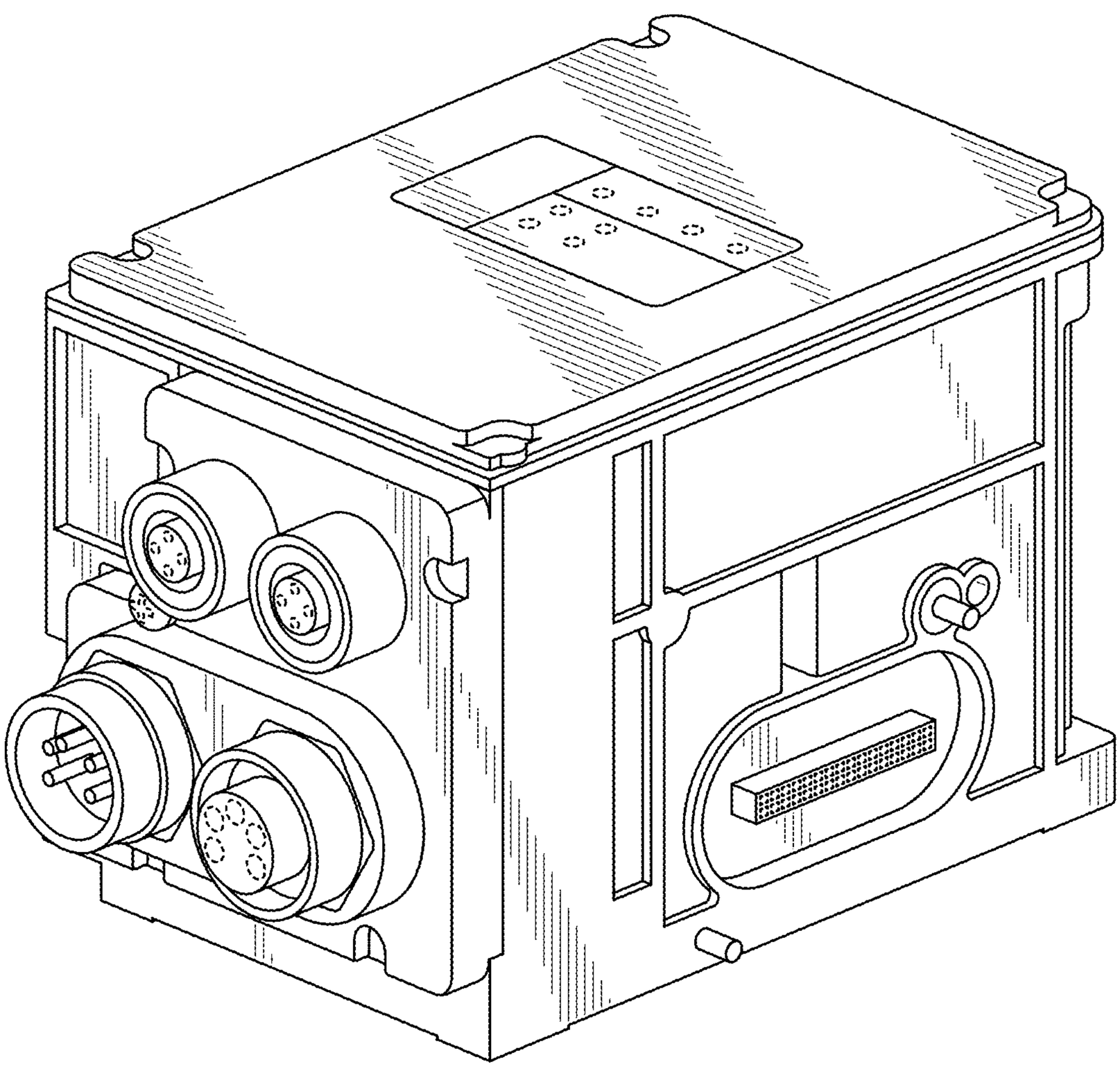

FIG. 3

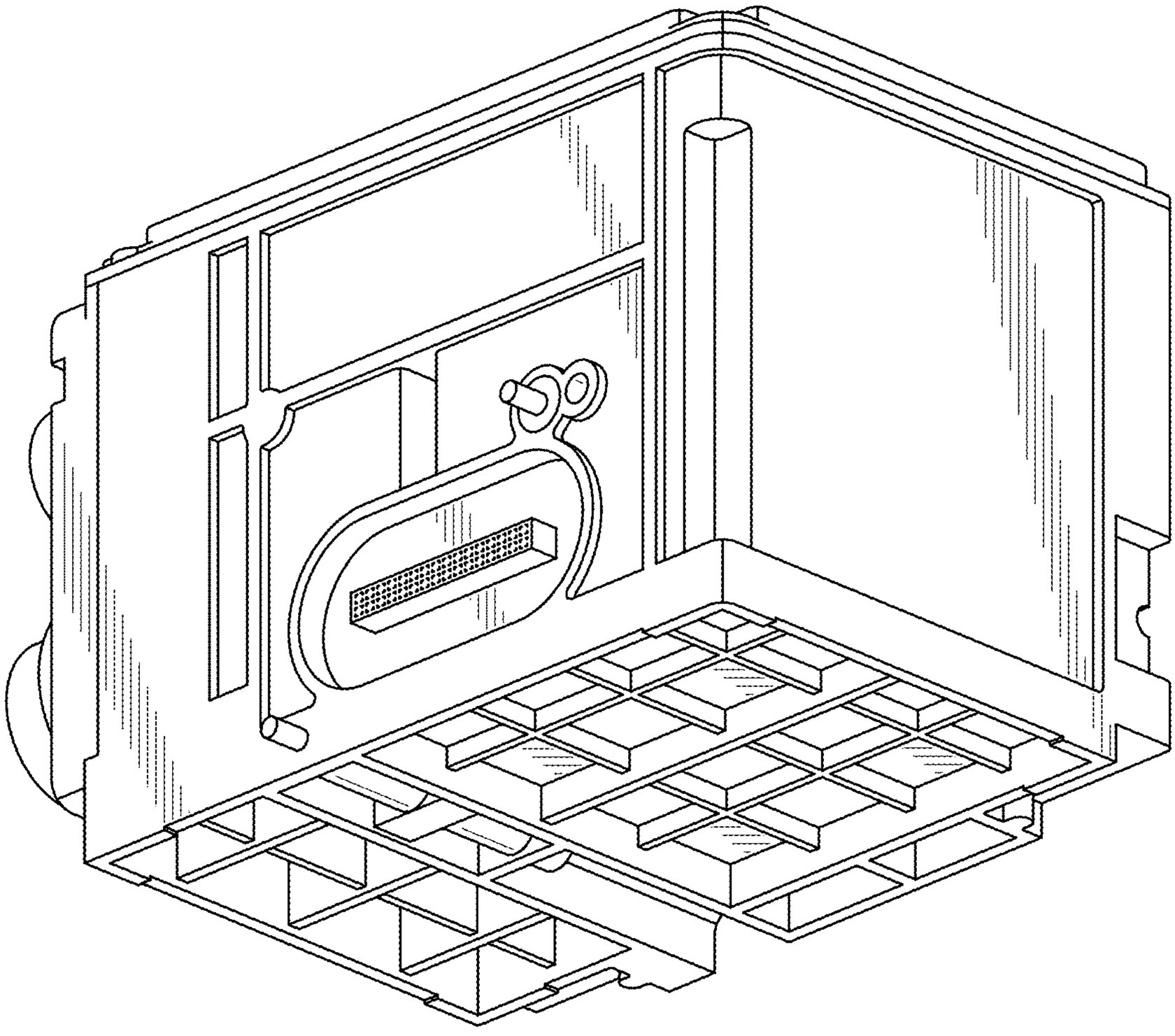

FIG. 4

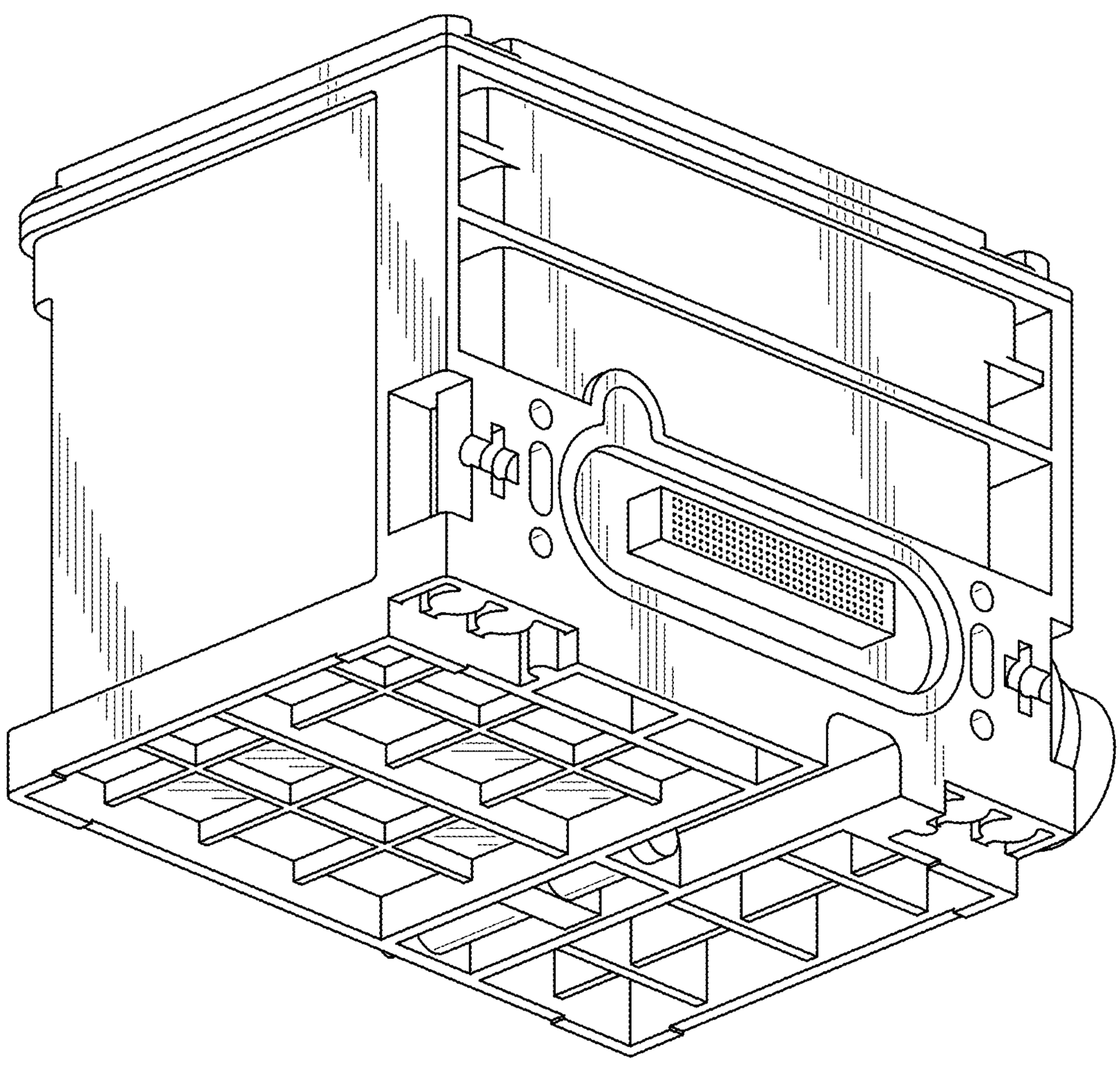

FIG. 5

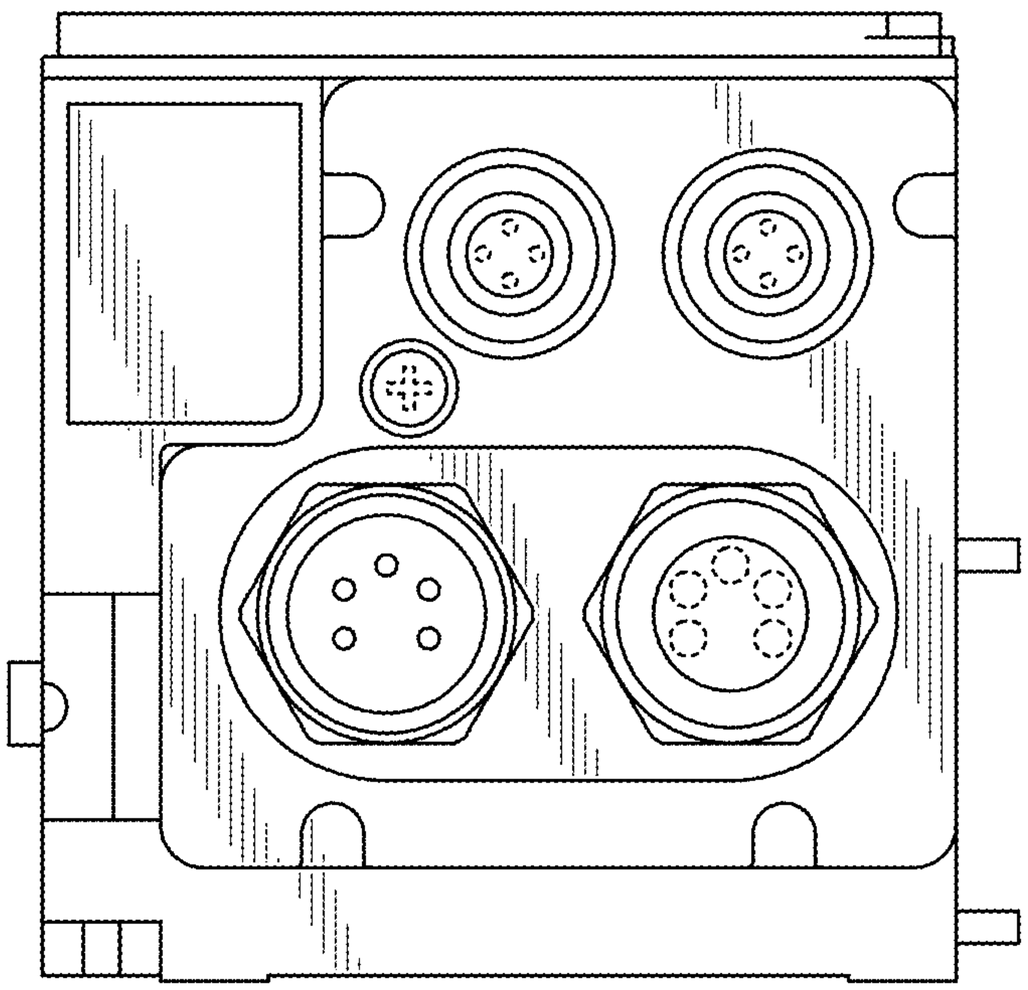

FIG. 6

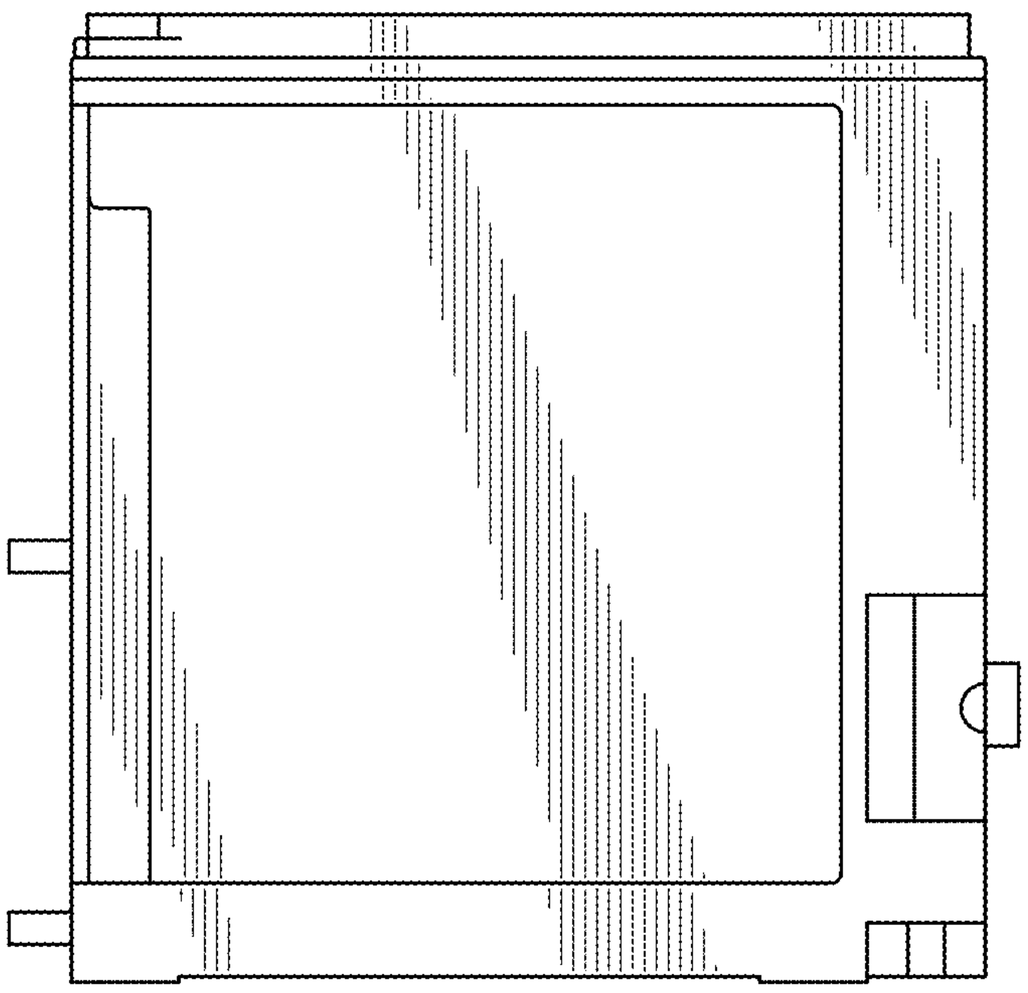

FIG. 7

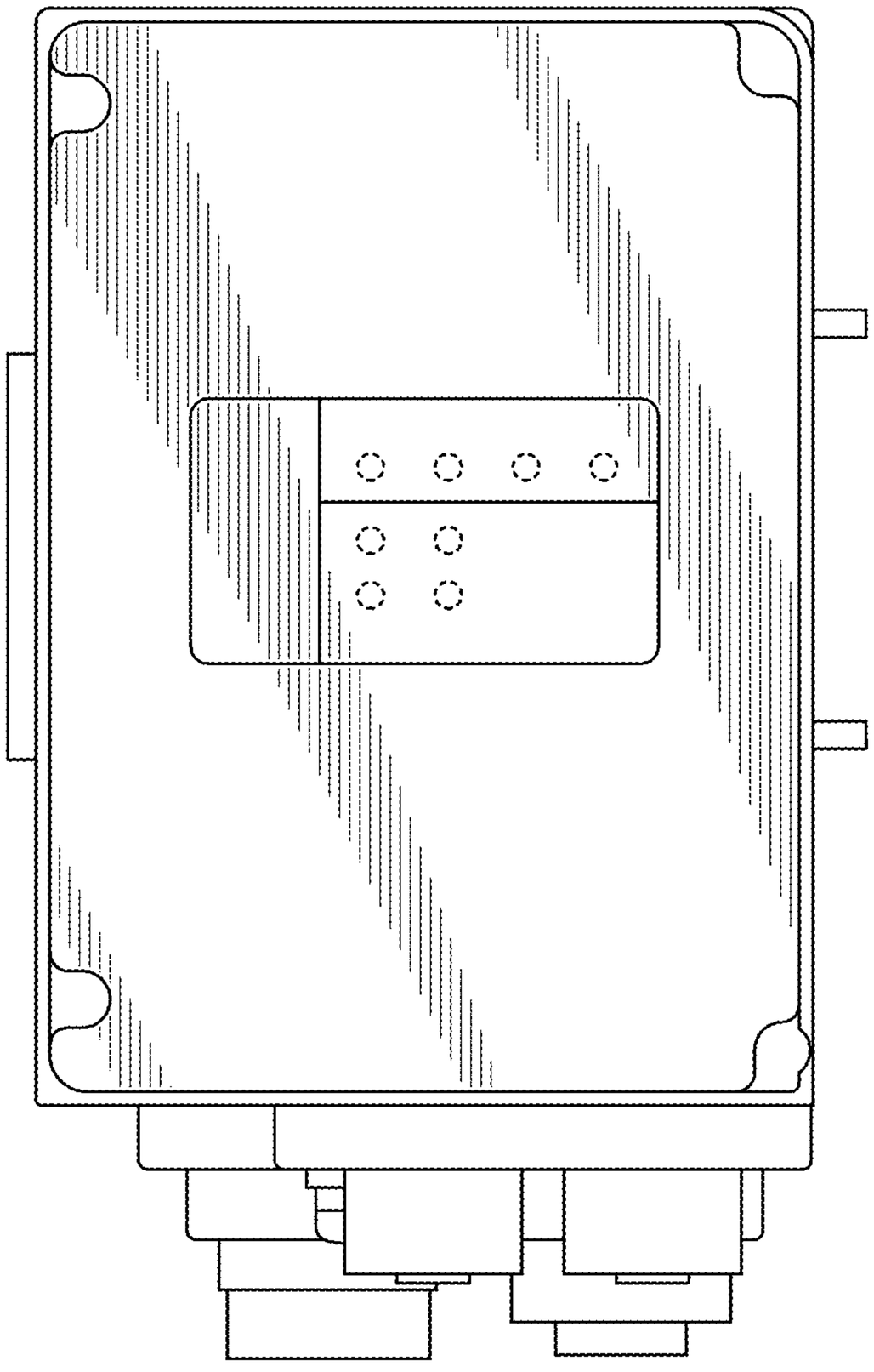

FIG. 8

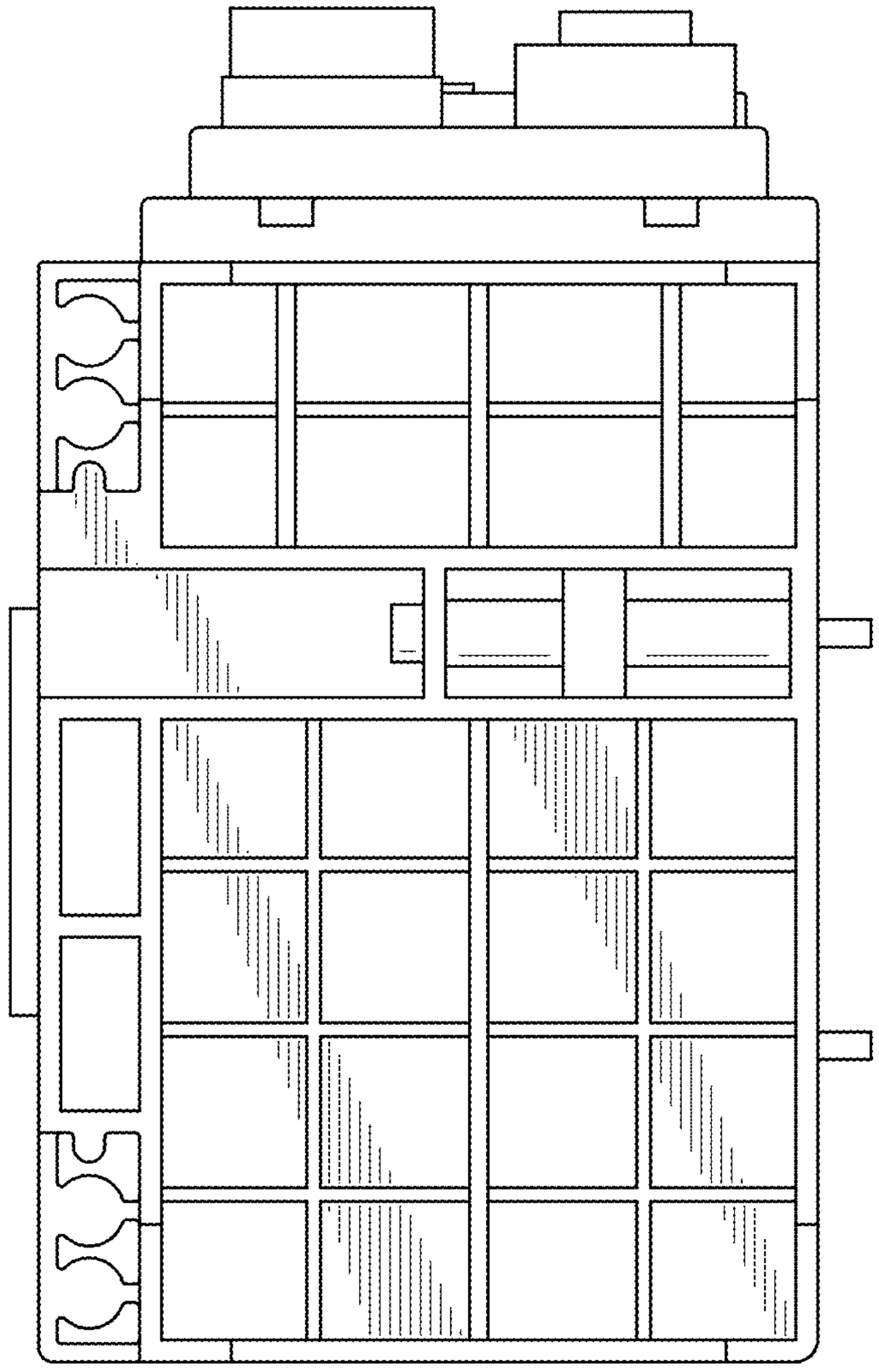

FIG. 9

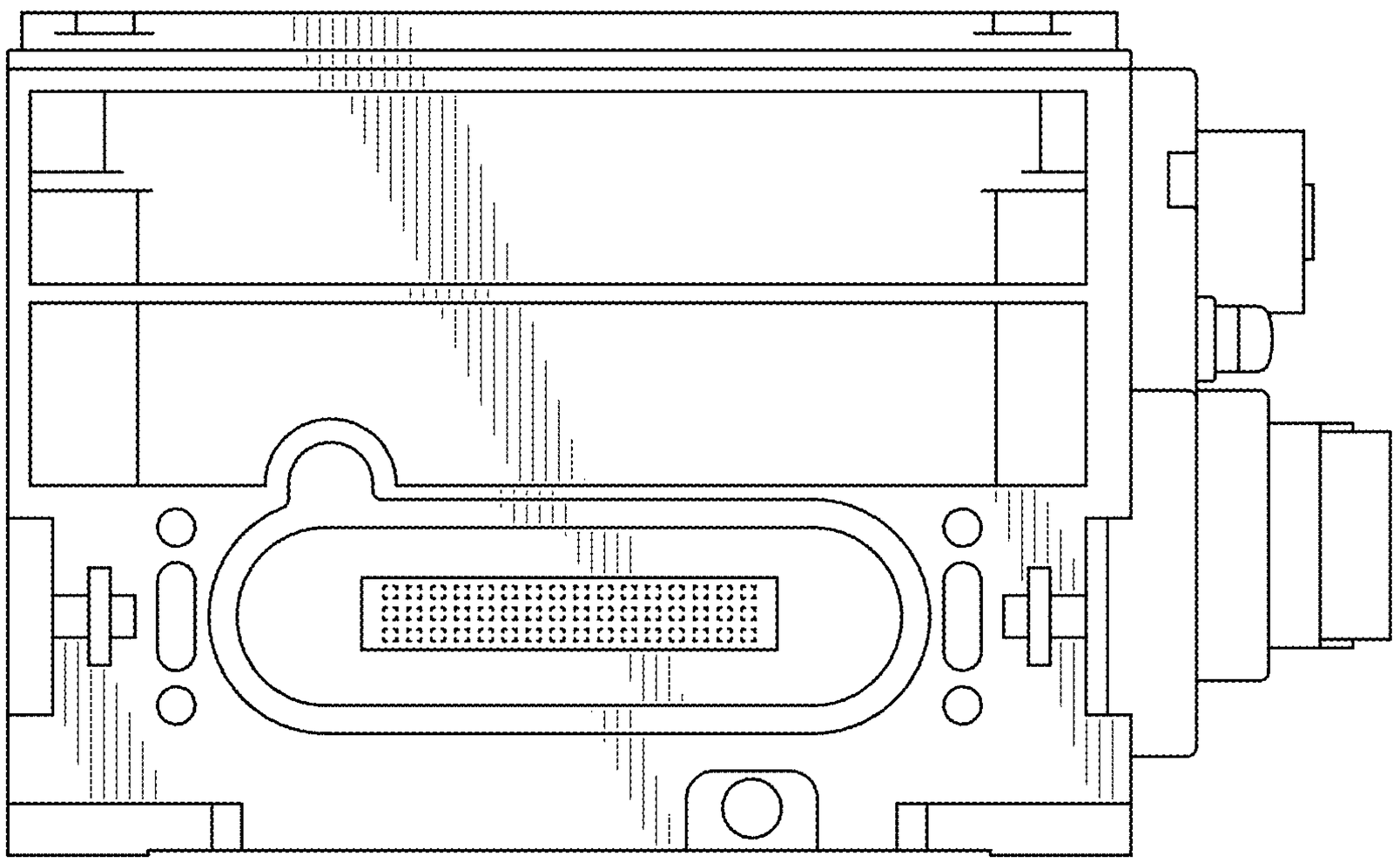

FIG. 10