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(12) **United States Design Patent**
Aiken et al.

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(54) **DICED SEMICONDUCTOR WAFER FOR MOSAIC SOLAR CELL FABRICATION**

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(**) Term: **15 Years**

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(51) **LOC (13) Cl.** **13-02**

(52) **U.S. Cl.**
USPC **D13/102**

(58) **Field of Classification Search**
USPC D10/104.1; D13/101, 102, 103, 107,
D13/109, 118, 119, 184, 199; D14/371,
D14/432, 439, 441, 447, 451; D21/480,
D21/484; D25/109, 140, 144
CPC .. F21S 8/086; F21S 8/088; F21S 9/032; F21S
9/035; H01L 31/042; H01L 31/022425;
H01L 31/18

See application file for complete search history.

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(57) **CLAIM**

The ornamental design for a diced semiconductor wafer for mosaic solar cell fabrication, as shown and described.

DESCRIPTION

The present application is related to U.S. patent application Ser. No. 29/768,304 filed simultaneously herewith.

FIG. 1 is a top perspective view of a diced semiconductor wafer for a mosaic solar cell fabrication showing our new design;

FIG. 2 is a top plan view the semiconductor wafer of FIG. 1 and the unclaimed environment of the semiconductor wafer which has been scribed to produce the four mosaic solar cell elements shown in the preceding Figure. The broken line represents unclaimed environment structure only and forms no part of the claimed design.

FIG. 3 is a bottom plan view thereof;

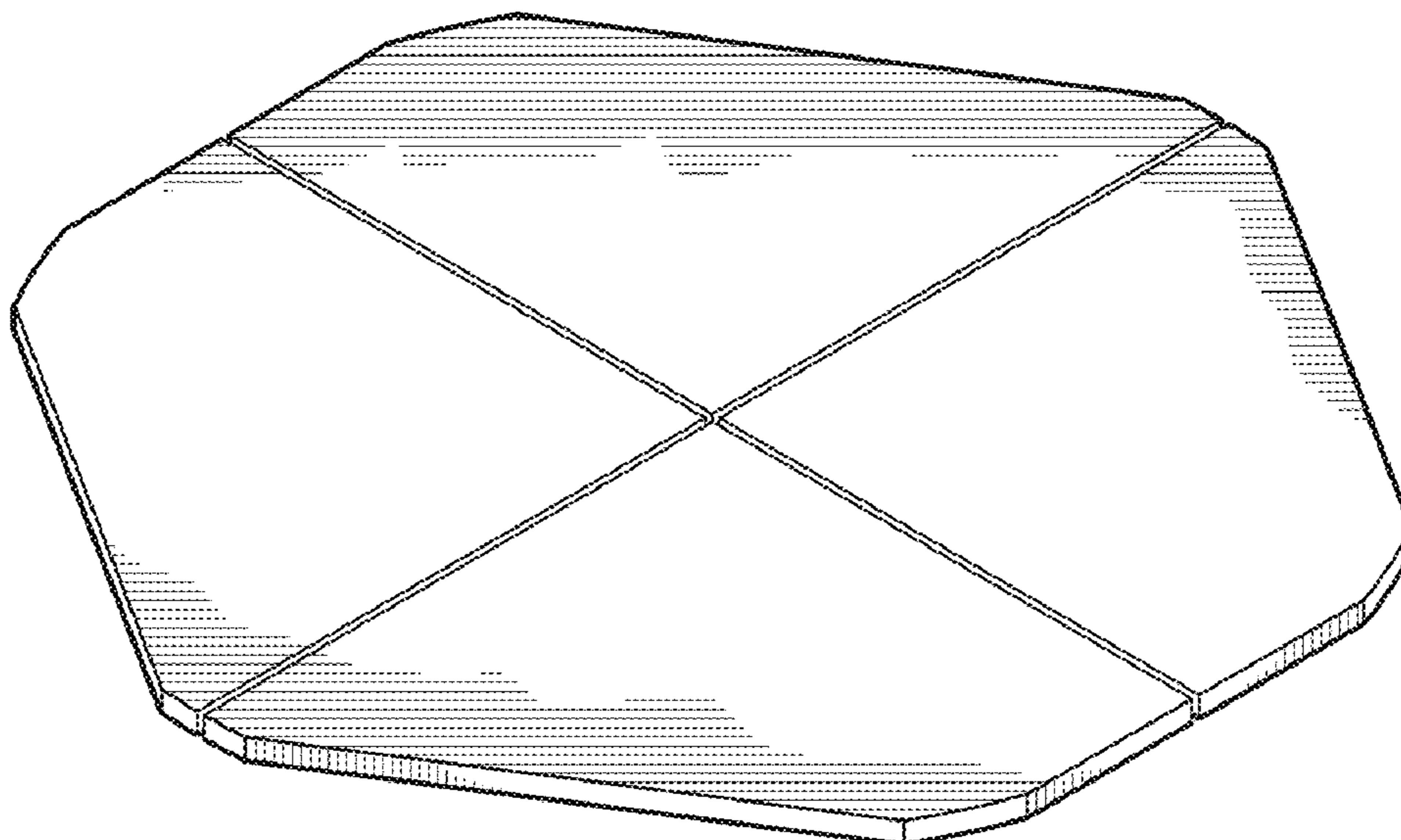
FIG. 4 is a front elevation thereof;

FIG. 5 is a rear elevation view thereof; and

FIG. 6 is a left elevation view thereof; and,

FIG. 7 is a right elevation view thereof.

1 Claim, 2 Drawing Sheets



(56)

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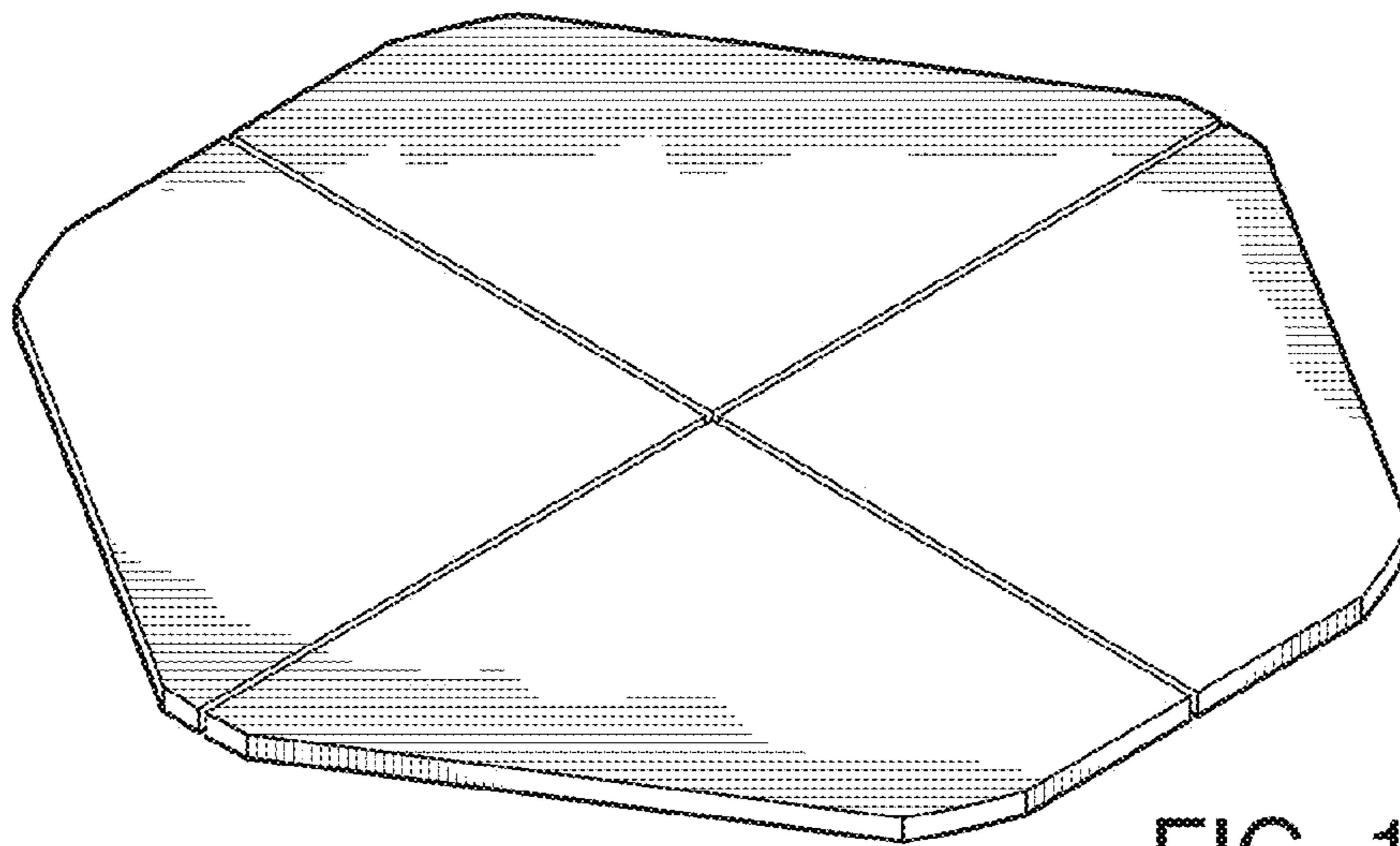


FIG. 1

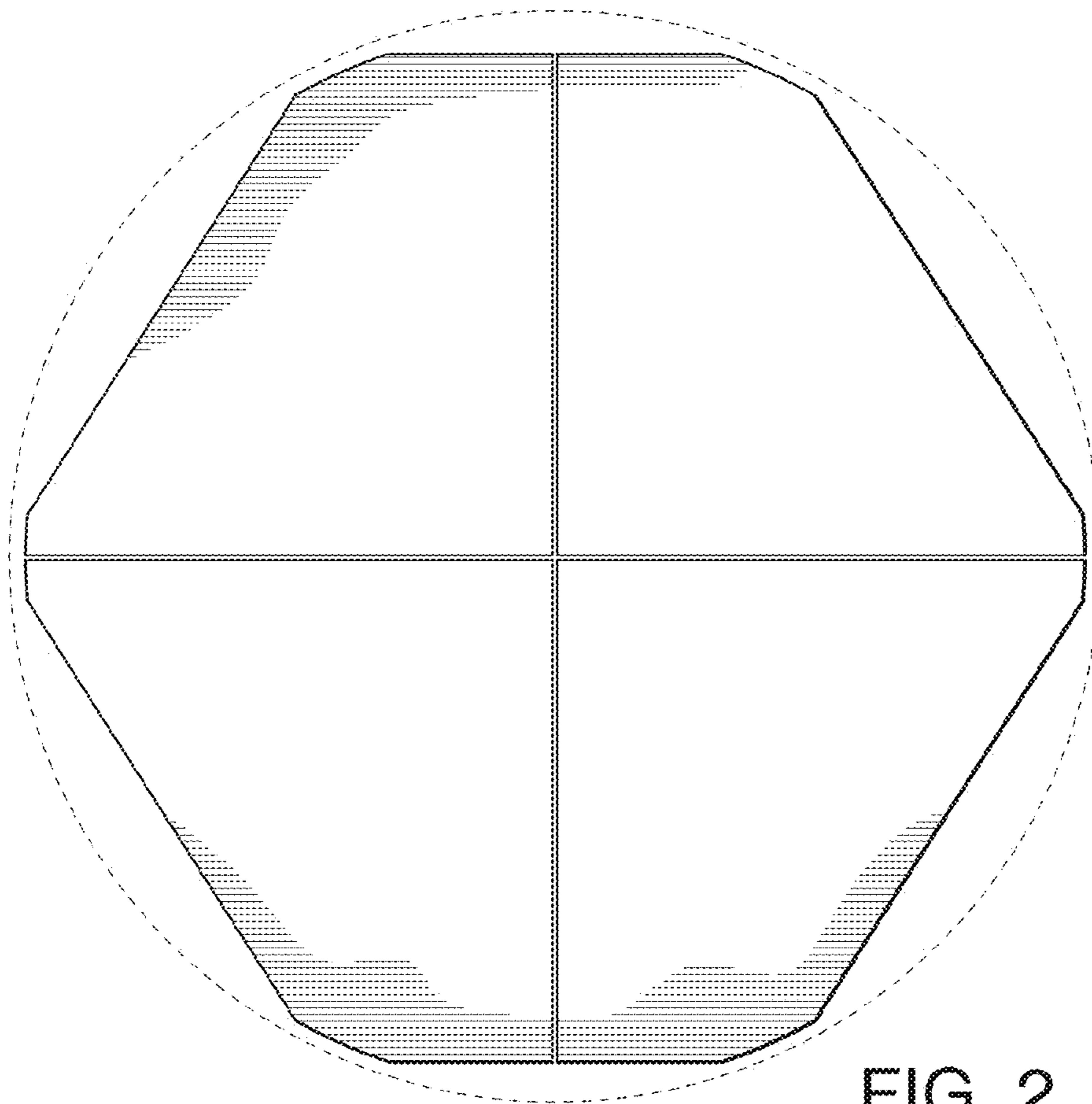


FIG. 2



FIG. 3



FIG. 4

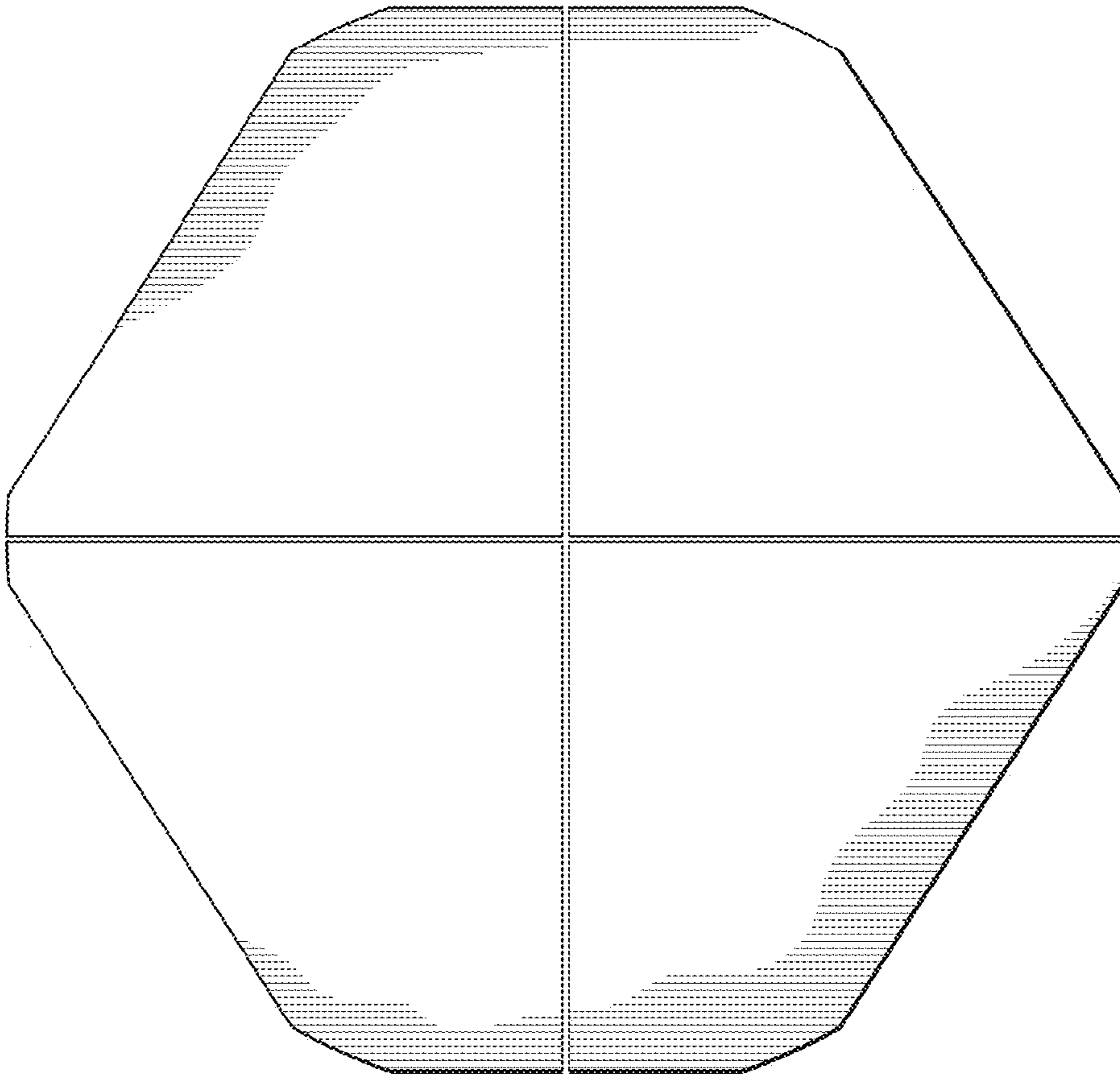


FIG. 5



FIG. 6



FIG. 7