



US00D942405S

(12) **United States Design Patent**
Soyano et al.

(10) **Patent No.:** **US D942,405 S**
(45) **Date of Patent:** **** Feb. 1, 2022**

(54) **SEMICONDUCTOR MODULE**

FOREIGN PATENT DOCUMENTS

(71) Applicant: **FUJI ELECTRIC CO., LTD.**,
Kawasaki (JP)

JP D1530503 S 8/2015
JP D1530504 S 8/2015

(Continued)

(72) Inventors: **Shin Soyano**, Shiojiri (JP); **Daisuke Inoue**, Matsumoto (JP)

OTHER PUBLICATIONS

(73) Assignee: **FUJI ELECTRIC CO., LTD.**,
Kawasaki (JP)

Semiconductor Modules. (Design—© Questel) orbit.com. [Online PDF compilation of references] 55pgs. Print Dates Range Aug. 13, 2020-Mar. 26, 2019 [Retrieved Jul. 20, 2021].*

(**) Term: **15 Years**

(Continued)

(21) Appl. No.: **29/696,618**

Primary Examiner — Manpreet S Matharu

(22) Filed: **Jun. 28, 2019**

Assistant Examiner — Suzanne E Tisdell

(30) **Foreign Application Priority Data**

(57) **CLAIM**

Jan. 11, 2019 (JP) 2019-000462

The ornamental design for a semiconductor module, as shown and described.

(51) **LOC (13) Cl.** **13-03**

DESCRIPTION

(52) **U.S. Cl.**

USPC **D13/182**

(58) **Field of Classification Search**

USPC D13/182

CPC H01L 24/72; H01L 21/00; H01L 2224/42;

H01L 2224/43; H01L 2021/00; H01L

2021/02; H01L 2021/04; H01L 2021/4814

See application file for complete search history.

FIG. 1 is a front view of a semiconductor module according to our new design;

FIG. 2 is a rear view of the semiconductor module of FIG. 1;

FIG. 3 is a top side view of the semiconductor module of FIG. 1;

FIG. 4 is a bottom side view of the semiconductor module of FIG. 1;

FIG. 5 is a left view of the semiconductor module of FIG. 1;

FIG. 6 is a right view of the semiconductor module of FIG. 1; and,

FIG. 7 is a perspective view illustrating the front, the top, and the left side of the semiconductor module of FIG. 1.

The thinner lines other than a thicker line in the front view, the rear view, the left side view the right side view, the top view, the bottom view, and the perspective view represents a shape of a three-dimensional shape.

(56) **References Cited**

U.S. PATENT DOCUMENTS

D432,096 S * 10/2000 Jeon D13/182

D774,479 S * 12/2016 Soyano D13/182

D810,706 S * 2/2018 Soyano D13/182

D814,433 S * 4/2018 Soyano D13/182

D827,593 S 9/2018 Soyano et al.

D847,103 S * 4/2019 Sawada D13/182

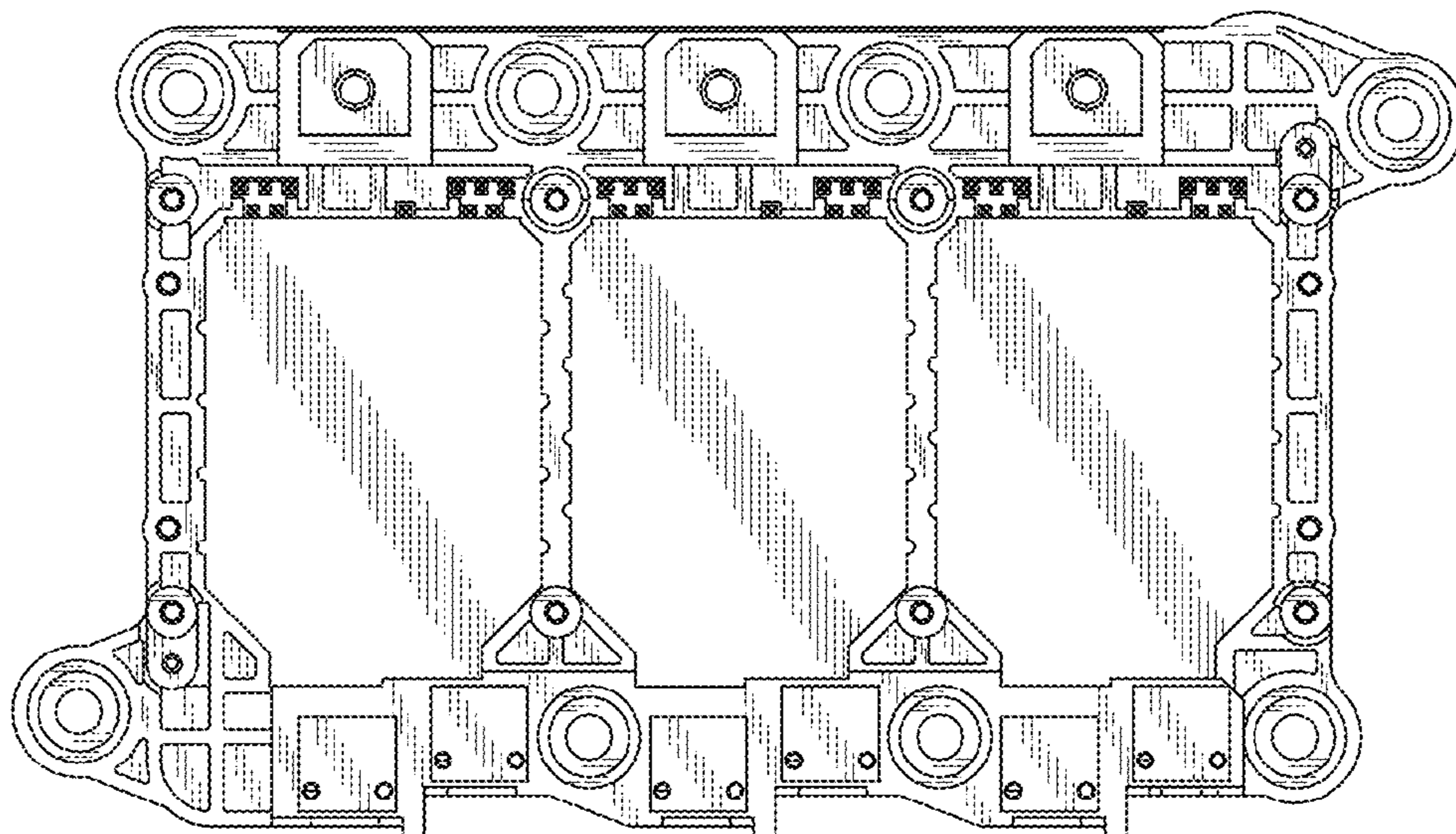
D847,104 S * 4/2019 Sawada D13/182

D858,467 S * 9/2019 Sawada D13/182

D864,132 S * 10/2019 Sawada D13/182

(Continued)

1 Claim, 7 Drawing Sheets



(56)

References Cited

U.S. PATENT DOCUMENTS

D875,058	S *	2/2020	Sawada	D13/182
D884,662	S *	5/2020	Itoh	D13/182
D903,612	S *	12/2020	Soyano	D13/182
D923,587	S *	6/2021	Aoki	D13/162
D923,591	S *	6/2021	Aoki	D13/182
2017/0006721	A1	1/2017	Soyano	
2017/0042053	A1	2/2017	Soyano	
2017/0263533	A1	9/2017	Koyama et al.	
2018/0183161	A1	6/2018	Soyano	
2019/0157221	A1	5/2019	Soyano et al.	

FOREIGN PATENT DOCUMENTS

JP	D1530505	S	8/2015
JP	2017-17195	A	1/2017
JP	2017-37892	A	2/2017
JP	2018-107395	A	7/2018
JP	2019-000461		1/2019
WO	2016/203884	A1	12/2016
WO	2016/204257	A1	12/2016
WO	2018/142863	A1	8/2018

OTHER PUBLICATIONS

“Diymore DC 12V 4-Wire PWM PC Fan Temperature Control.” Aug. 23, 2017. Amazon. https://www.amazon.com/Diymore-Temperature-Manumotive-Controller-High-Temperature/dp/B0752GMMPJ/ref=sr_1_20?dchild=1&keywords=thermostat+controller+module&qid=1626799125&sr=8-20.*

“Noyito Voltage to Current Module.” Mar. 11, 2018. Amazon. https://www.amazon.com/NOYITO-Voltage-Current-Module-Generator/dp/B07BDG984B/ref=sr_1_85?dchild=1&keywords=semiconductor+module&qid=1626799627&sr=8-85.*

“Discrete Semiconductor Modules.” Feb. 11, 2019. Amazon. https://www.amazon.com/Discrete-Semiconductor-Modules-Amps-1200V/dp/B00HKZ5VPM/ref=sr_1_195?dchild=1&keywords=semiconductor+module&qid=1626811298&sr=8-19511-2019.*

Japanese Notification for Reasons for Refusal dated Sep. 10, 2019 in corresponding Japanese Design Patent Application No. 2019-000462.

Japanese Written Directive dated Sep. 10, 2019 in corresponding Japanese Design Patent Application No. 2019-000462.

* cited by examiner

FIG. 1

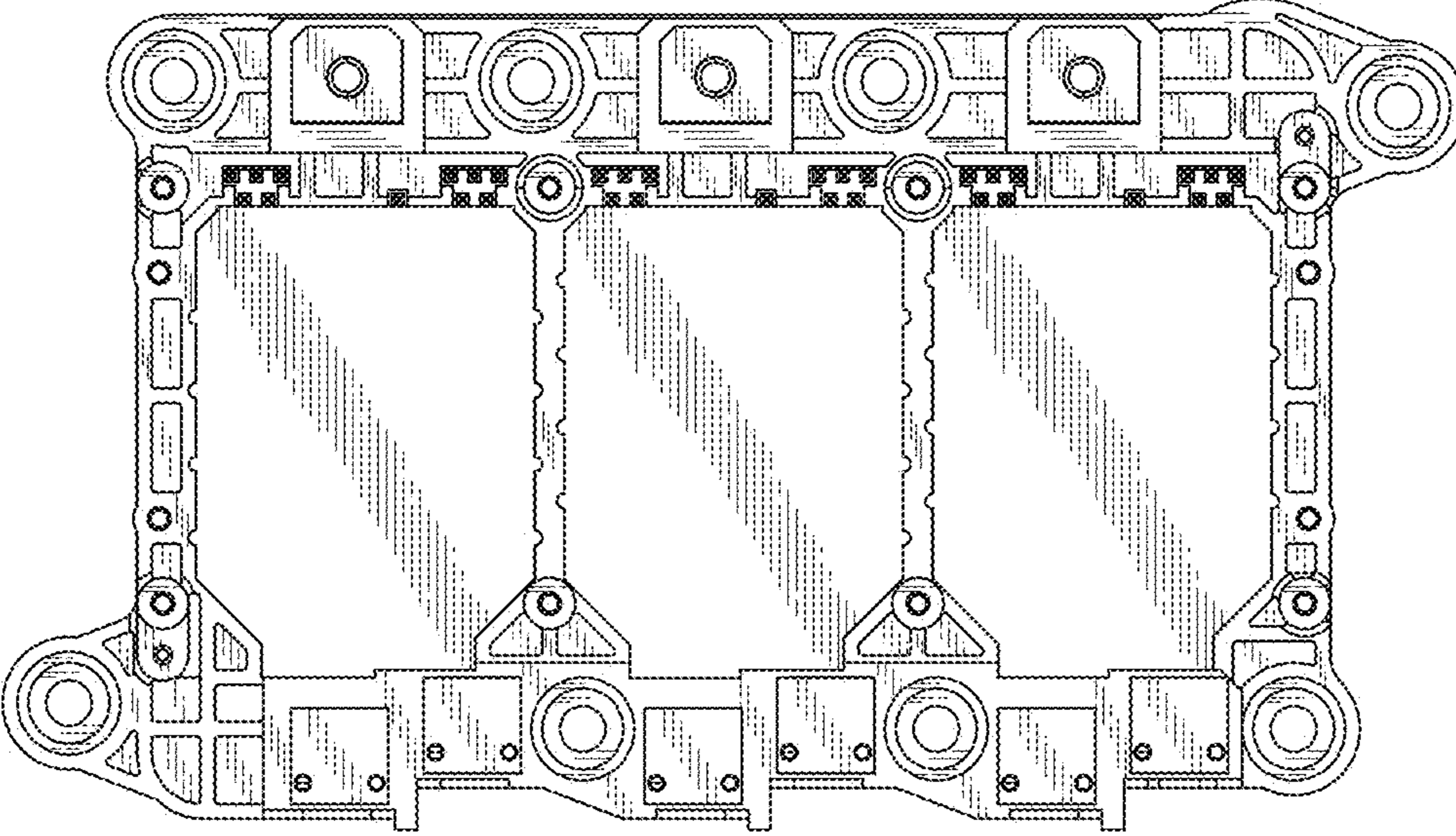


FIG.2

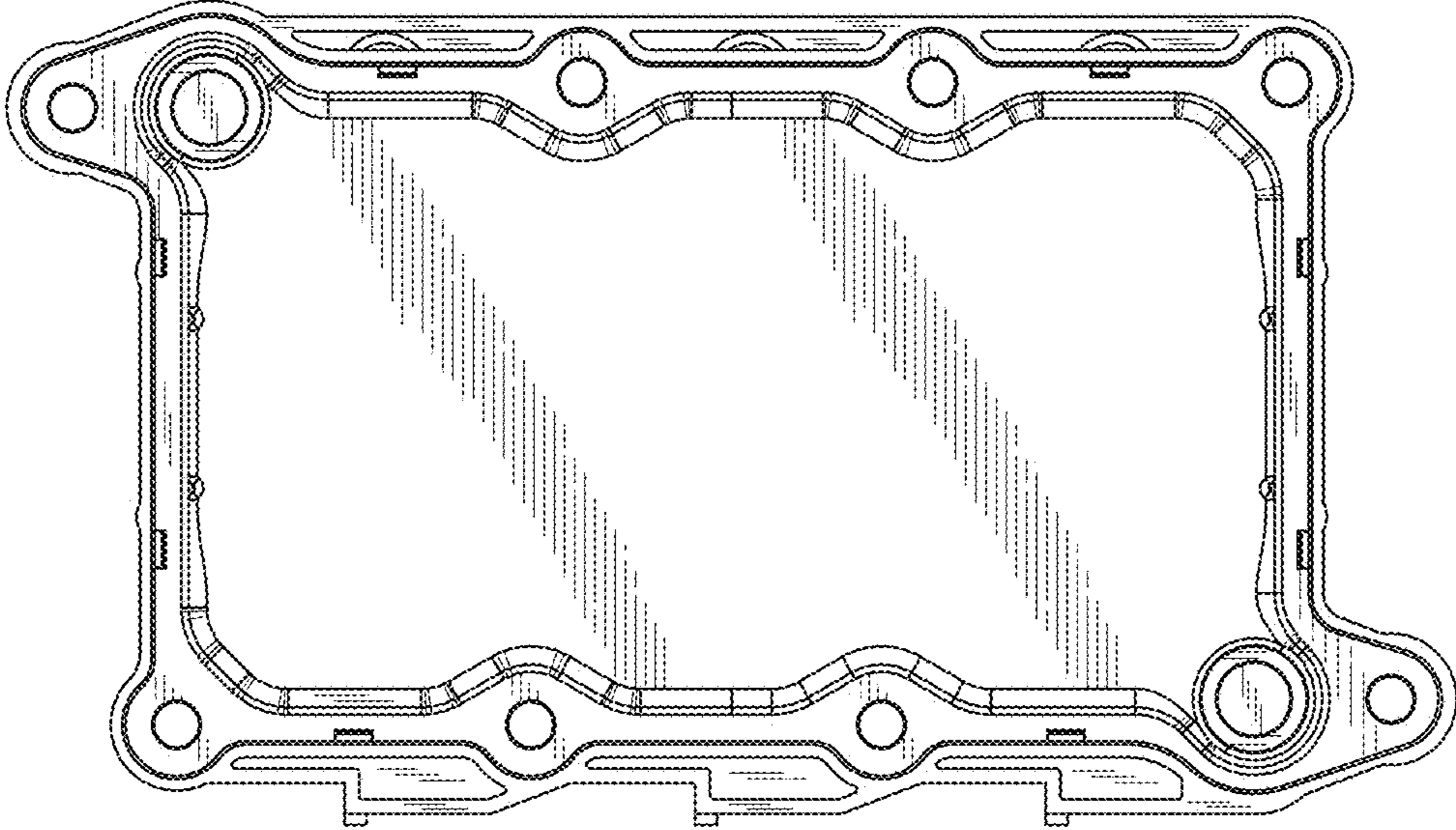


FIG.3

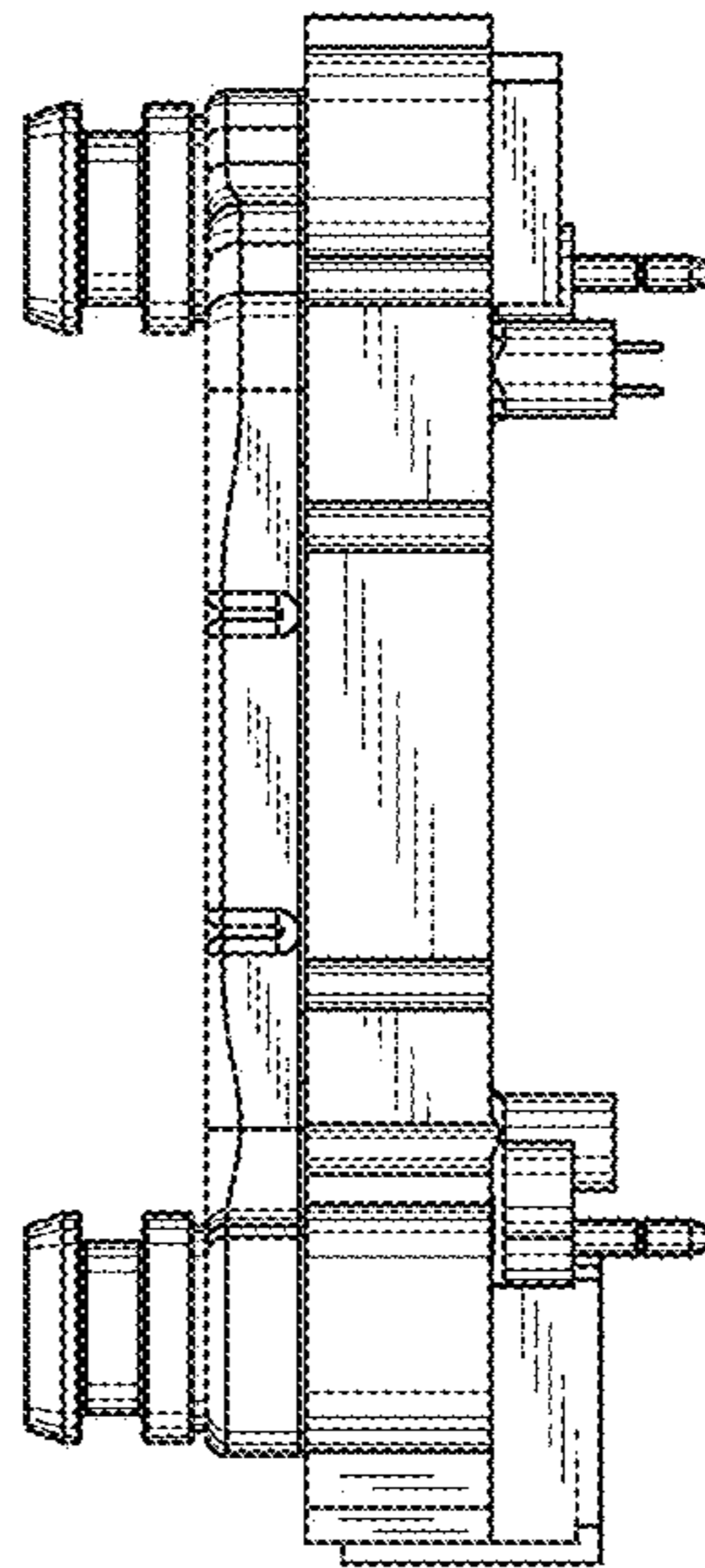


FIG.4

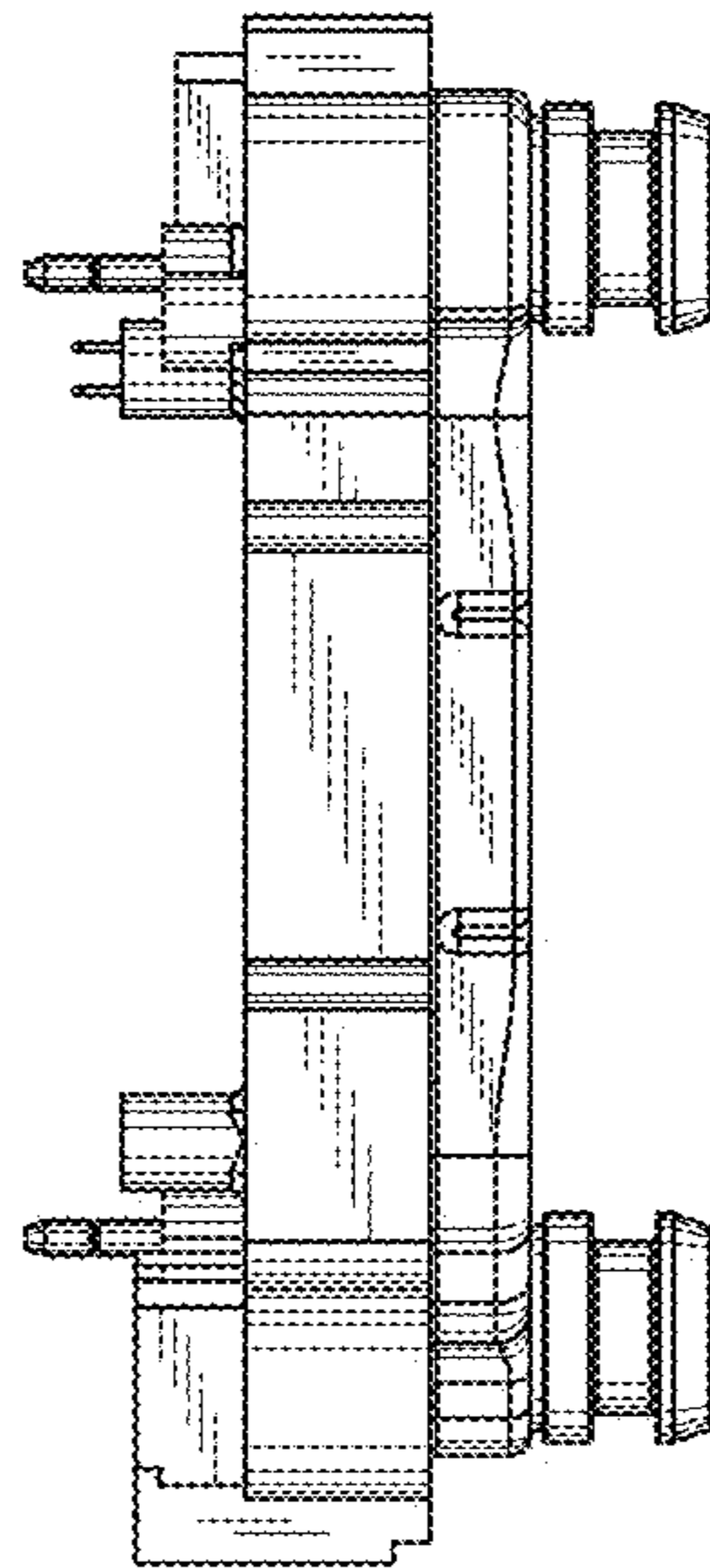


FIG.5

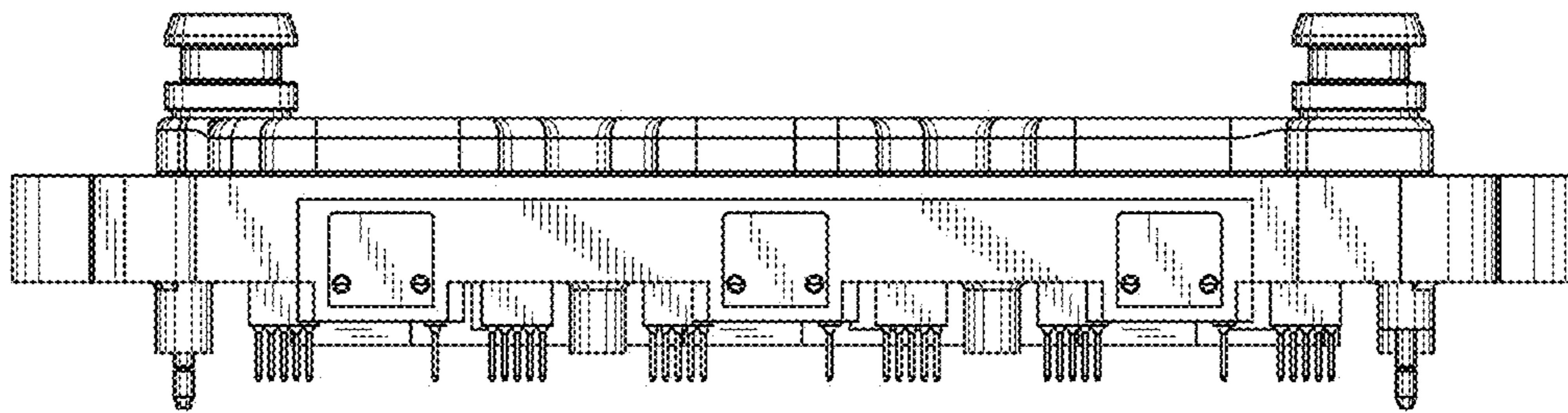


FIG.6

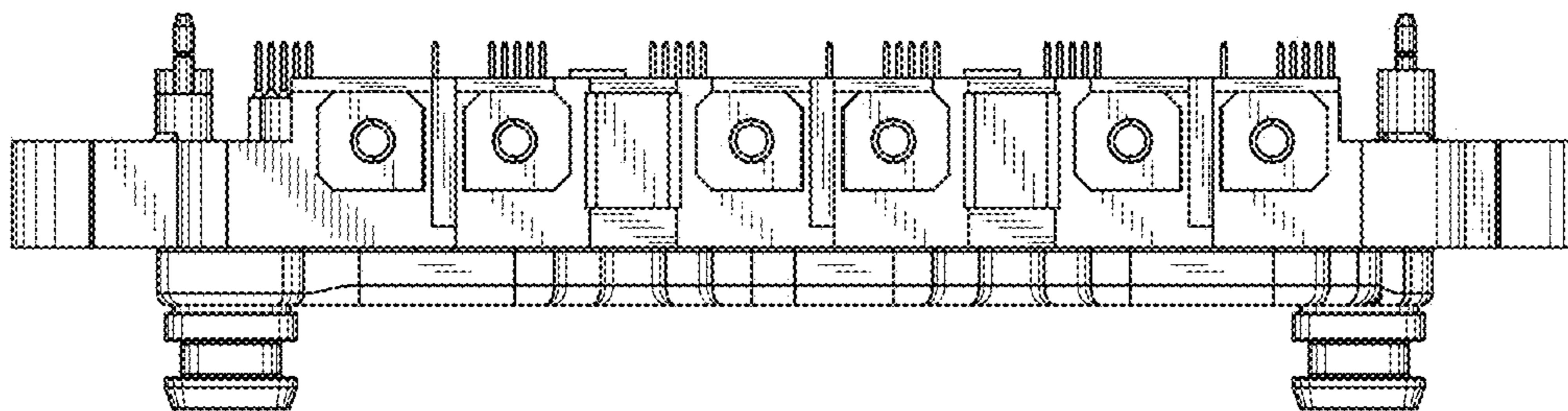


FIG.7

