



US00D934187S

(12) **United States Design Patent** (10) **Patent No.:** **US D934,187 S**
Cheng (45) **Date of Patent:** **** Oct. 26, 2021**

(54) **INTEGRATED CIRCUIT PACKAGE**
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(72) Inventor: **Lang Cheng**, Guangdong (CN)
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(51) **LOC (13) Cl.** **13-03**
(52) **U.S. Cl.**
USPC **D13/182**
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361/775, 783, 820; 174/250, 253;
438/15, 25, 26, 51, 55, 63, 106
CPC . H01L 21/00; H01L 2224/42; H01L 2224/43;
H01L 2021/00; H01L 2021/02; H01L
2021/04; H01L 21/4814; H01L 21/4846;
H01L 21/4871; H01L 21/67144; H01L
23/02; H01L 23/13; H01L 23/14; H01L
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H02B 6/4201; G02B 6/4256; G02B
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G02B 6/428; G02B 6/4281; H05K 1/14;
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H05K 1/026

See application file for complete search history.

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(57) **CLAIM**

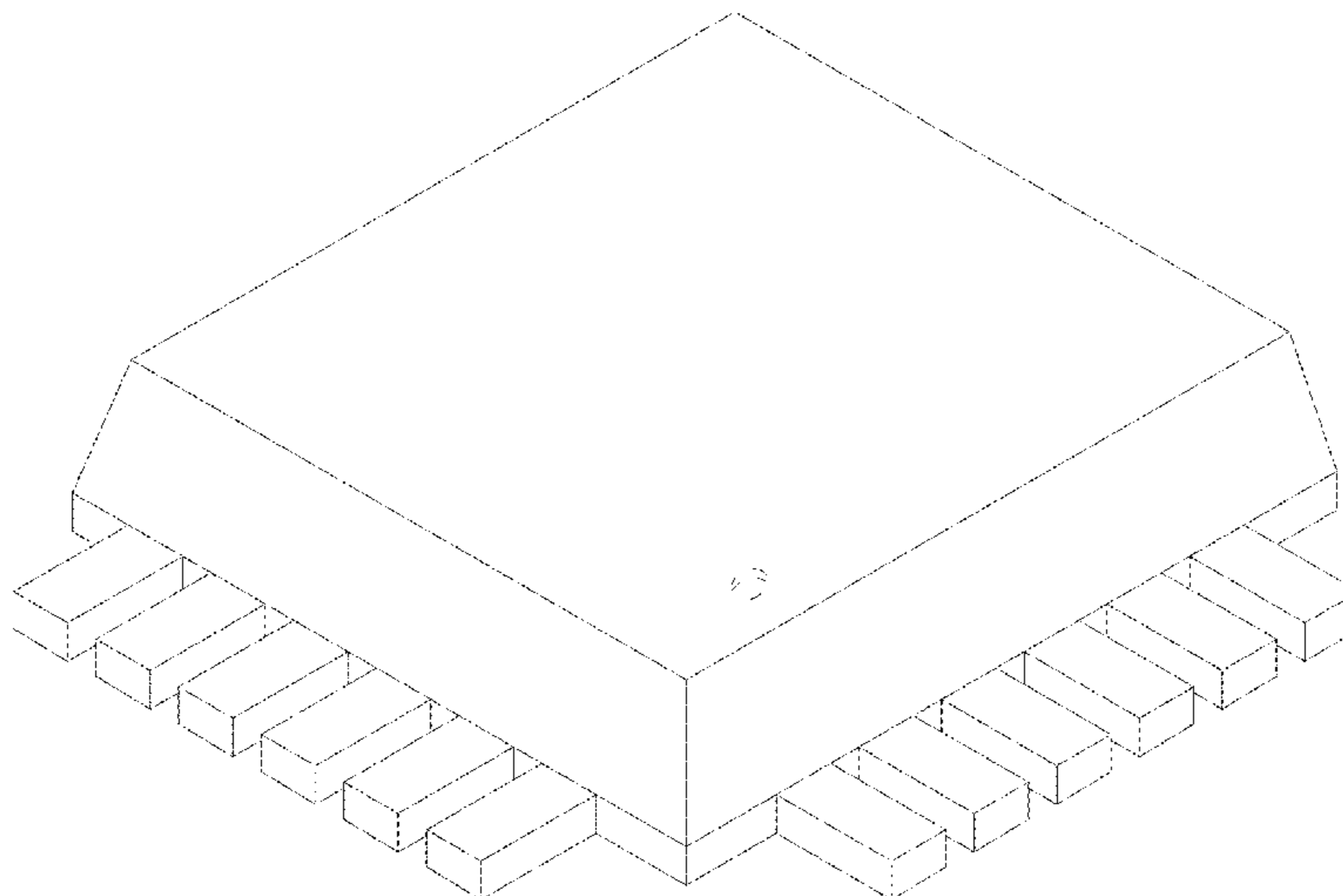
The ornamental design for an integrated circuit package, as shown and described.

DESCRIPTION

FIG. 1 is a front elevational view of an integrated circuit package showing my new design;
FIG. 2 is a rear elevational view thereof;
FIG. 3 is a left side elevational view thereof;
FIG. 4 is a right side elevational view thereof;
FIG. 5 is a top plan view thereof;
FIG. 6 is a bottom plan view thereof; and,
FIG. 7 is a perspective view thereof.

The broken lines shown on the integrated circuit package form no part of the claimed design.

1 Claim, 6 Drawing Sheets



(56)

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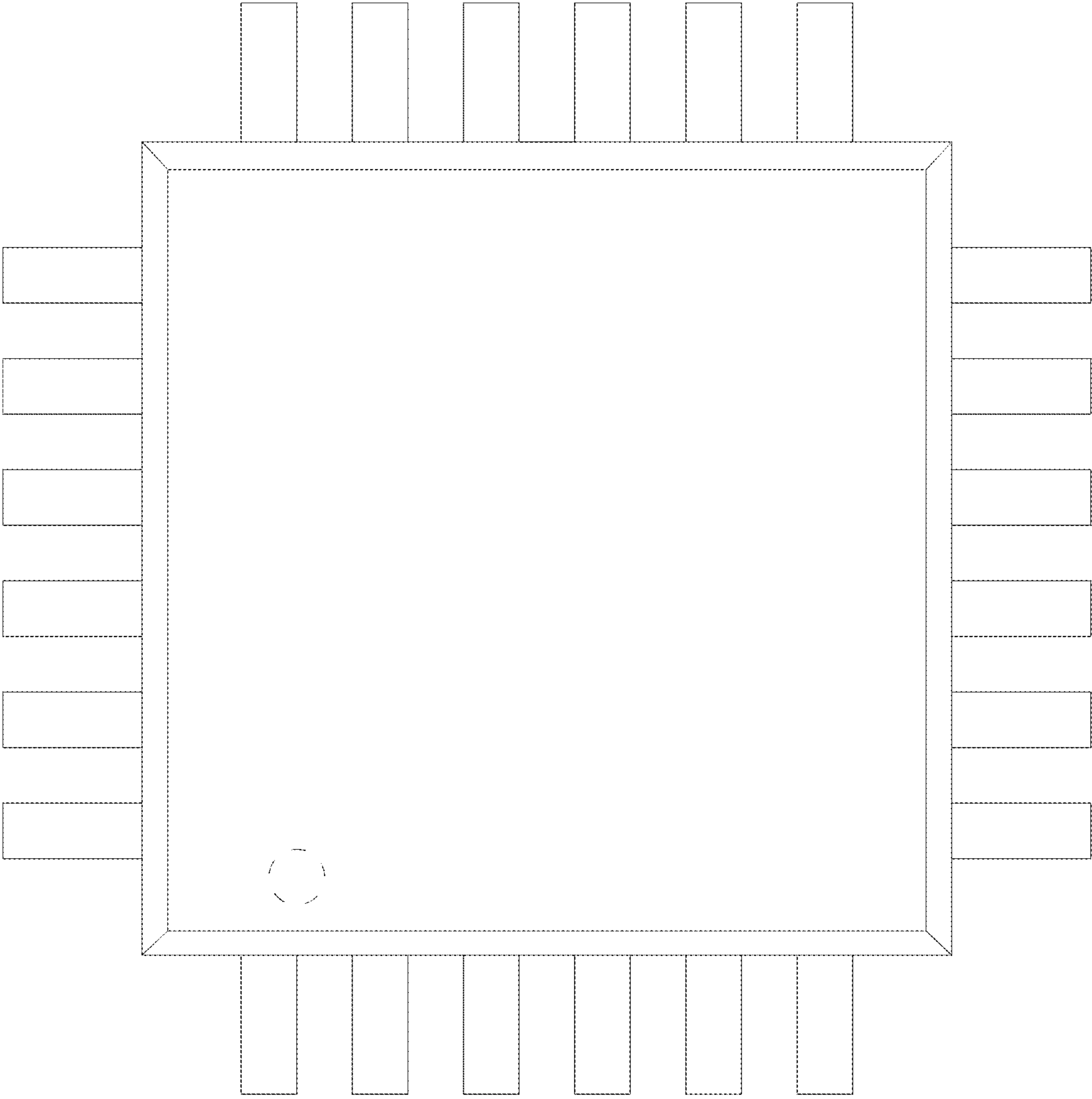


FIG. 1

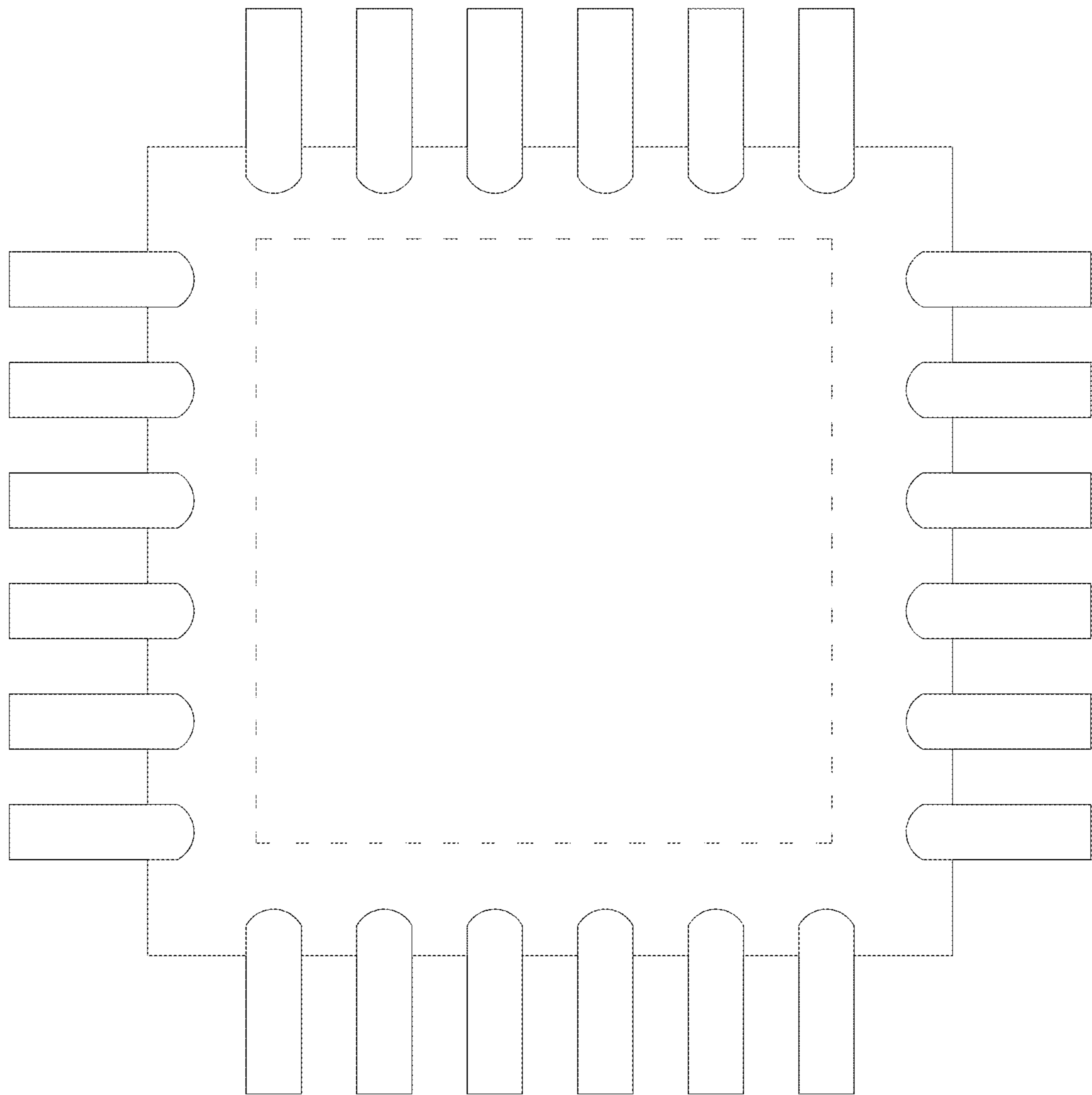


FIG. 2

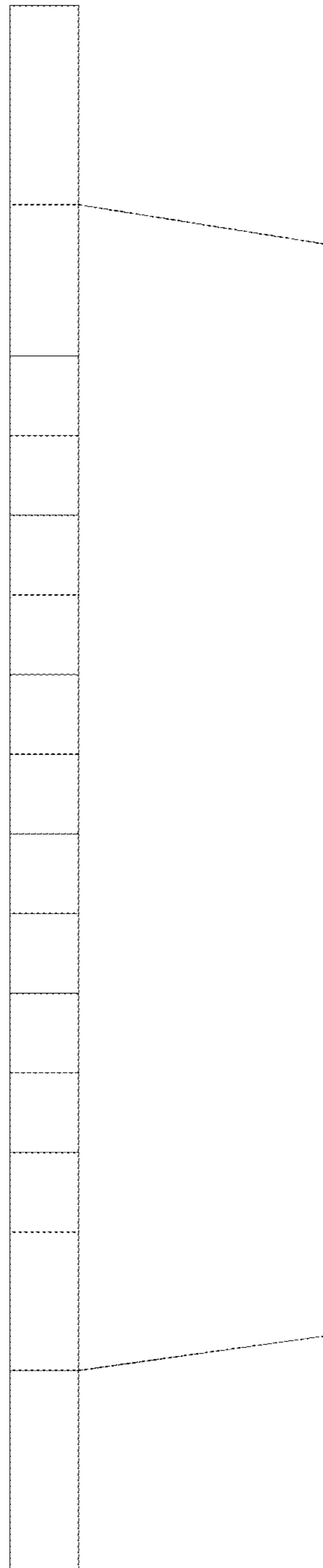


FIG. 3

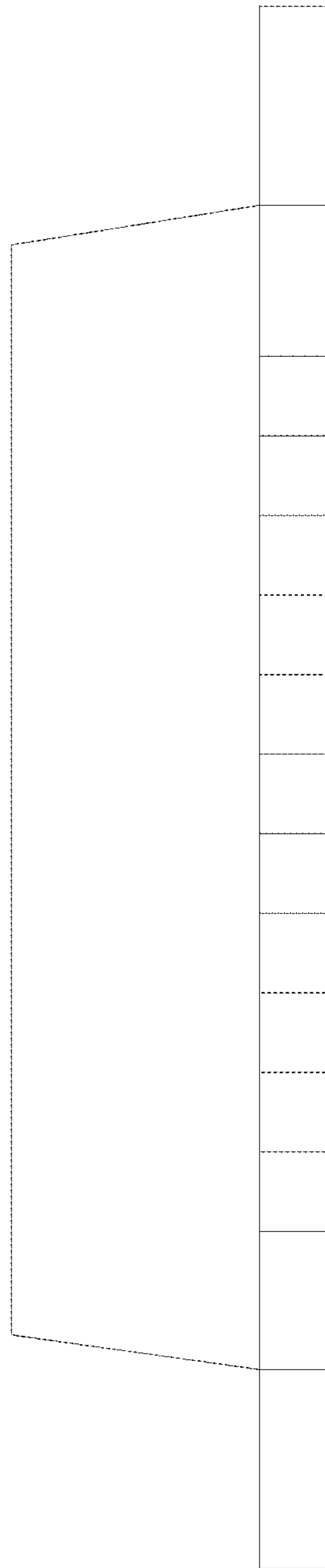


FIG. 4

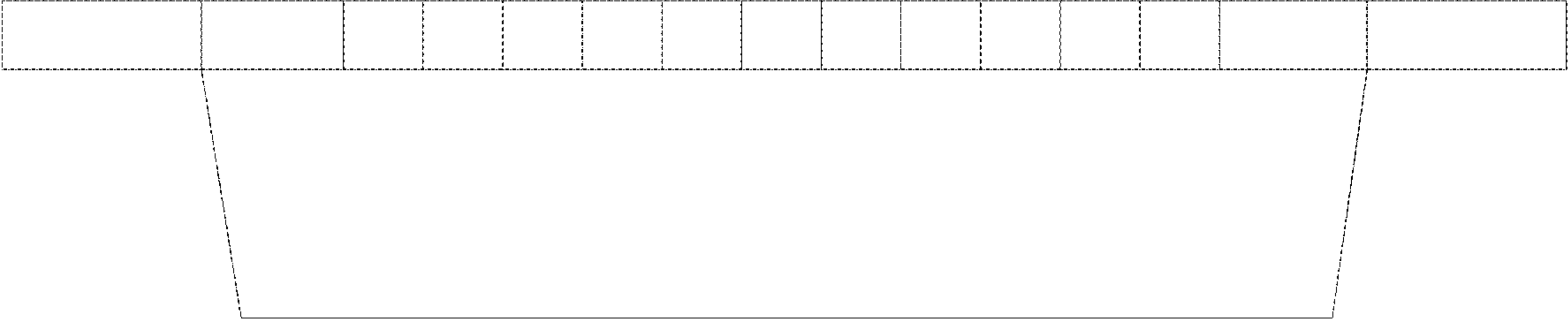


FIG. 5



FIG. 6

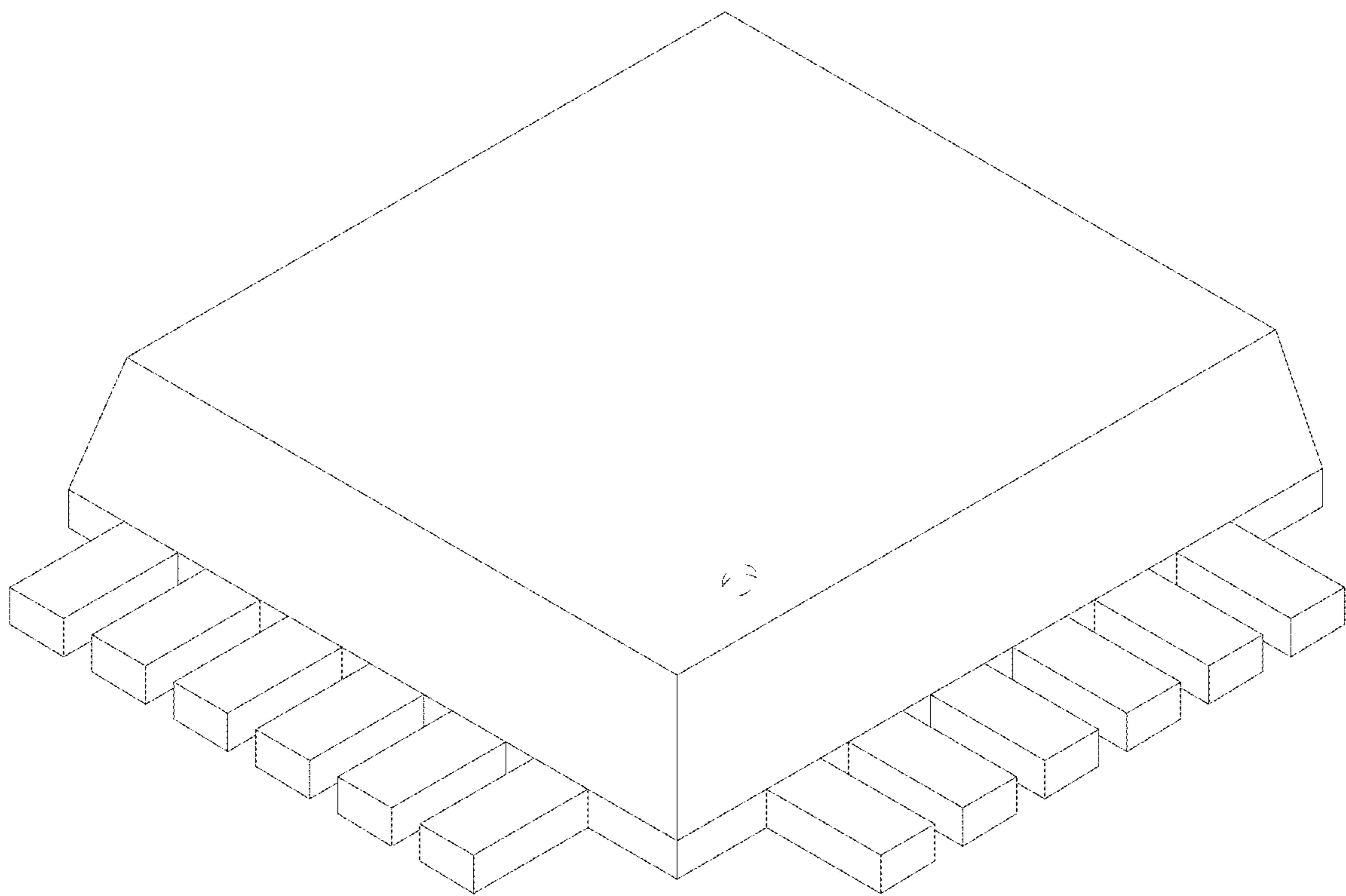


FIG. 7