



US00D928105S

(12) **United States Design Patent** (10) **Patent No.:** **US D928,105 S**
Saito (45) **Date of Patent:** **** Aug. 17, 2021**

(54) **SEMICONDUCTOR DEVICE**
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(73) Assignee: **ROHM CO., LTD.**, Kyoto (JP)
(**) Term: **15 Years**
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(52) **U.S. Cl.**
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H01L 21/4846; H01L 21/4871; H01L
21/67144; H01L 2224/42; H01L 2224/43;
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2924/1711; H01L 2924/1715; H01L
2924/181; H01L 2924/1811; H01L
2924/1815; H01L 2924/19042; H01L
2924/1905

See application file for complete search history.

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(57) **CLAIM**

The ornamental design for a semiconductor device, as shown and described.

DESCRIPTION

FIG. 1 is a perspective view of a semiconductor device showing my new design;

FIG. 2 is a front view thereof;

FIG. 3 is a top plan view thereof;

FIG. 4 is a bottom plan view thereof;

FIG. 5 is a left side view thereof;

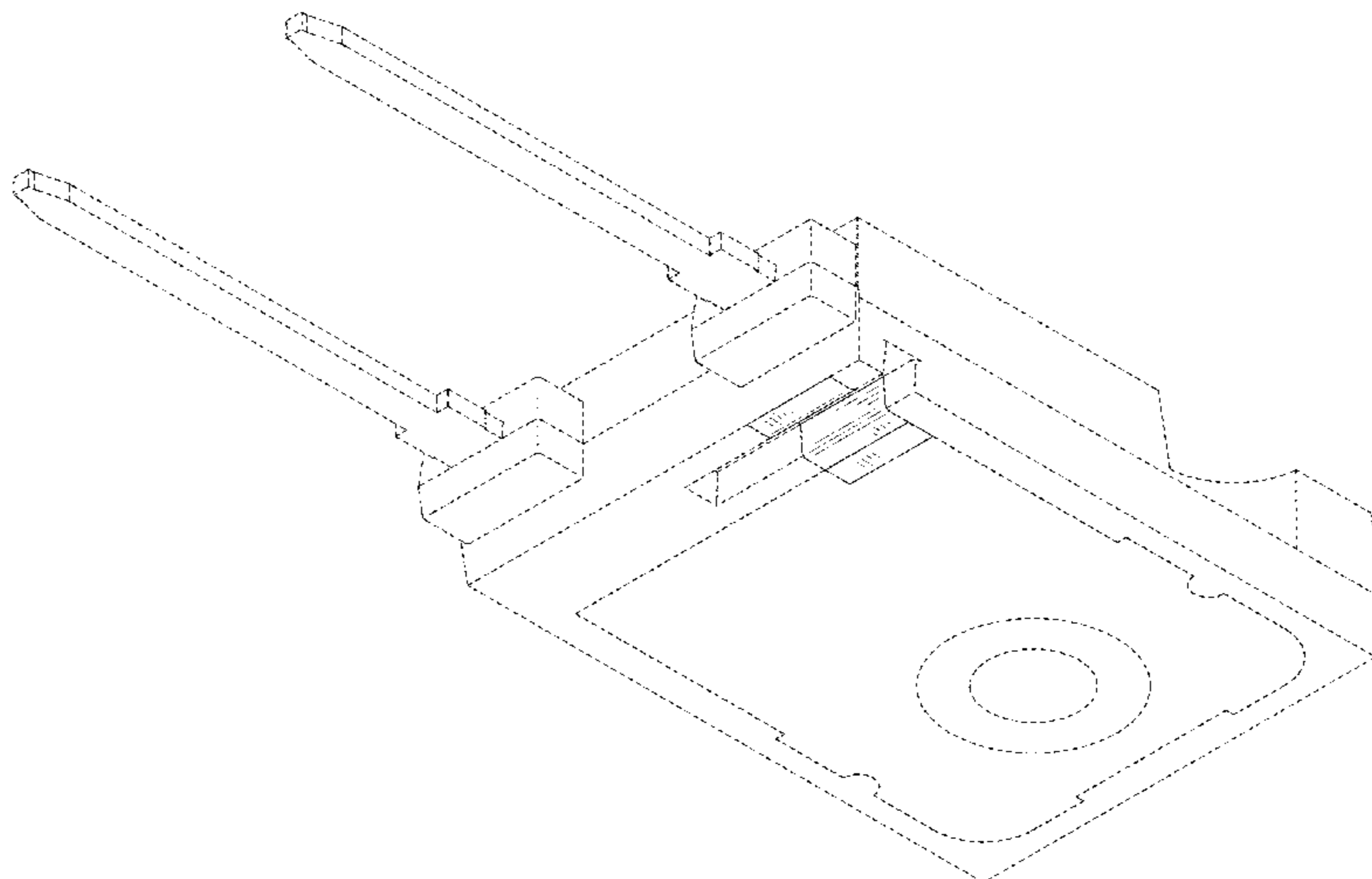
FIG. 6 is an enlarged cross-sectional view taken along line 6-6 in FIG. 4; and,

FIG. 7 is an enlarged cross-sectional view taken along line 7-7 in FIG. 4.

The even broken lines illustrate portions of the semiconductor device that form no part of the claimed design. The dash-dotted lines denote the boundary of the claim and form no part of the claimed design.

In FIGS. 1 and 4, the solid line extending in the vertical length direction, and which is co-linear with an even broken line at one end and a dash-dotted line at the other end, represents a claimed structure line of an electrode plate of the semiconductor device.

1 Claim, 7 Drawing Sheets



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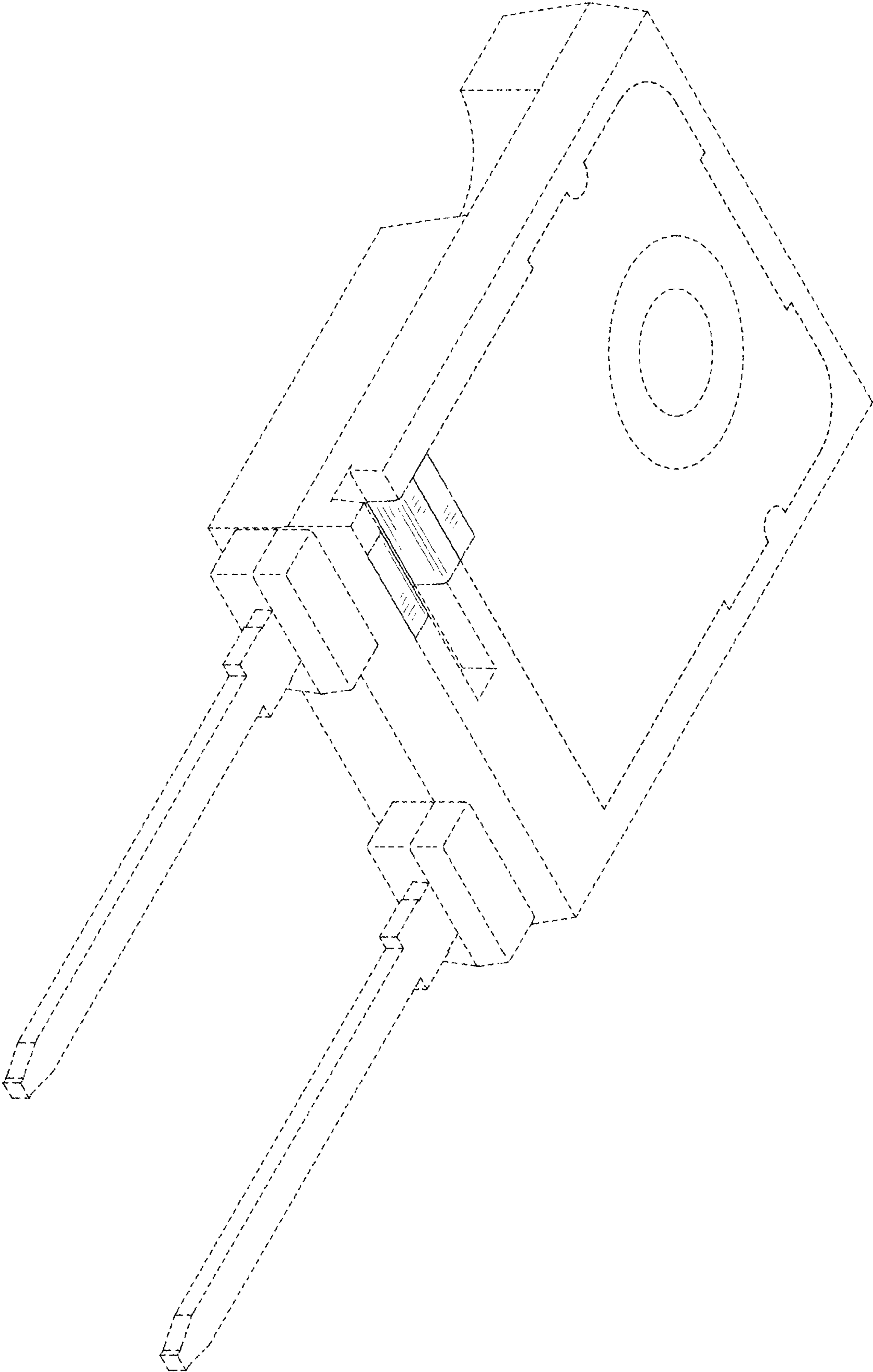


FIG.1

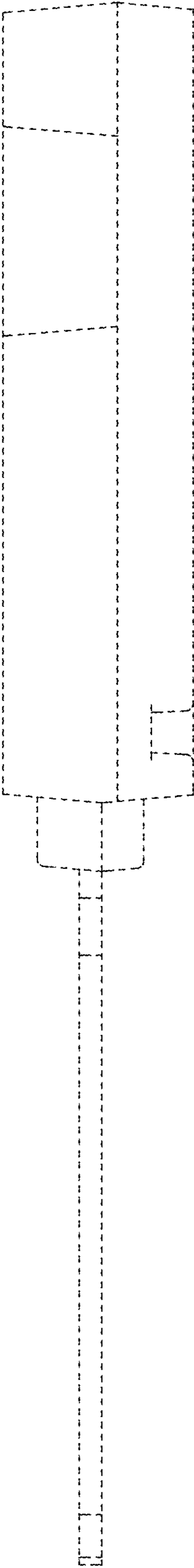


FIG.2

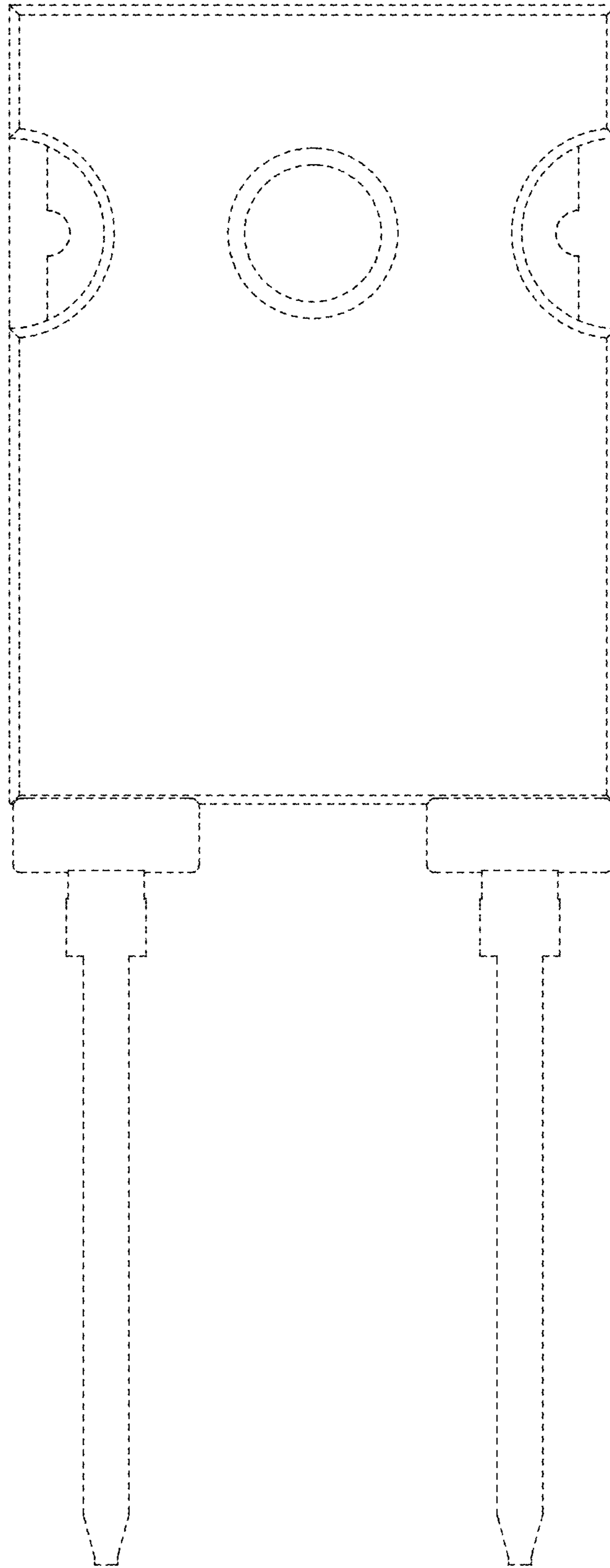


FIG. 3

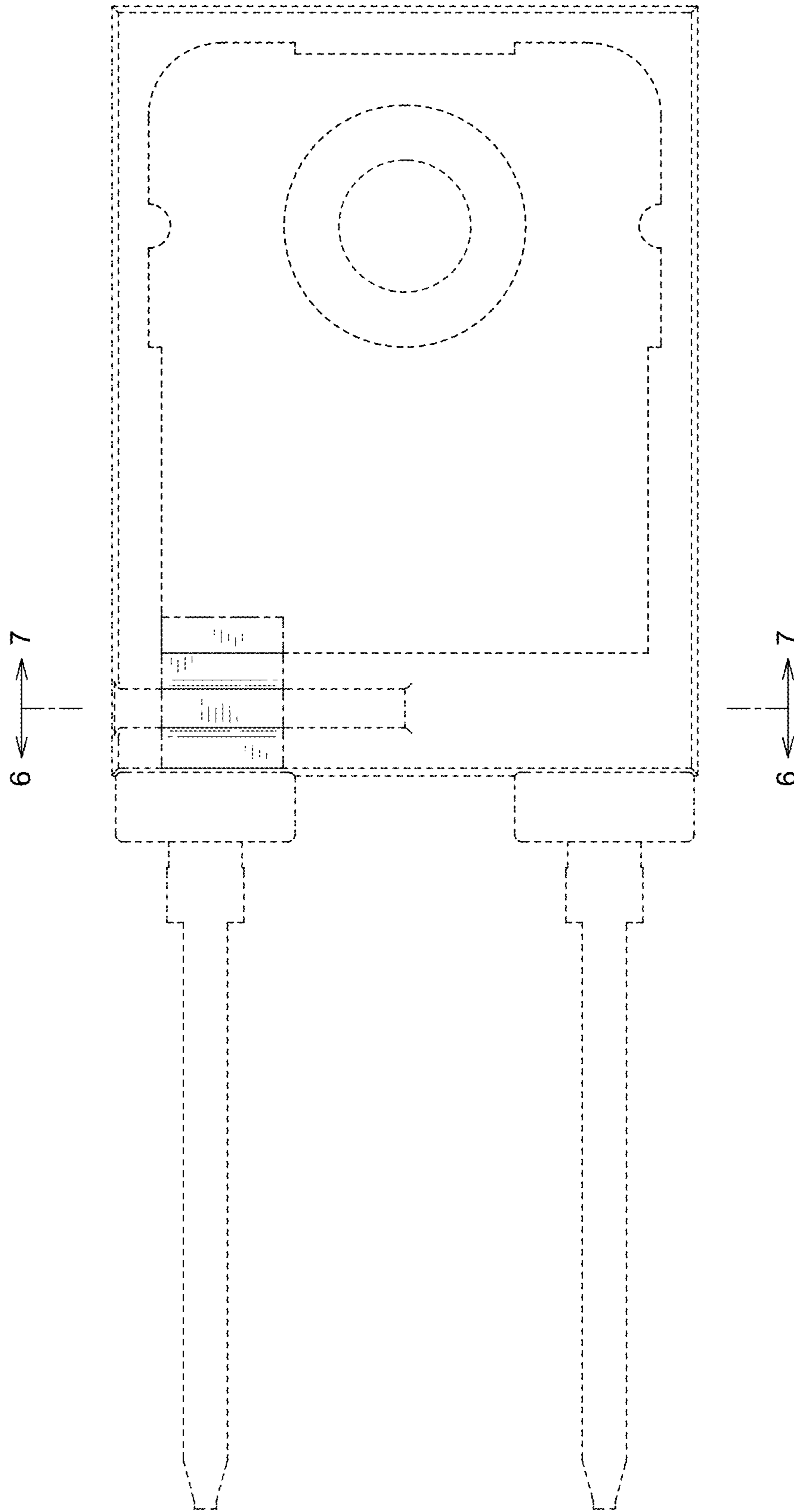


FIG. 4

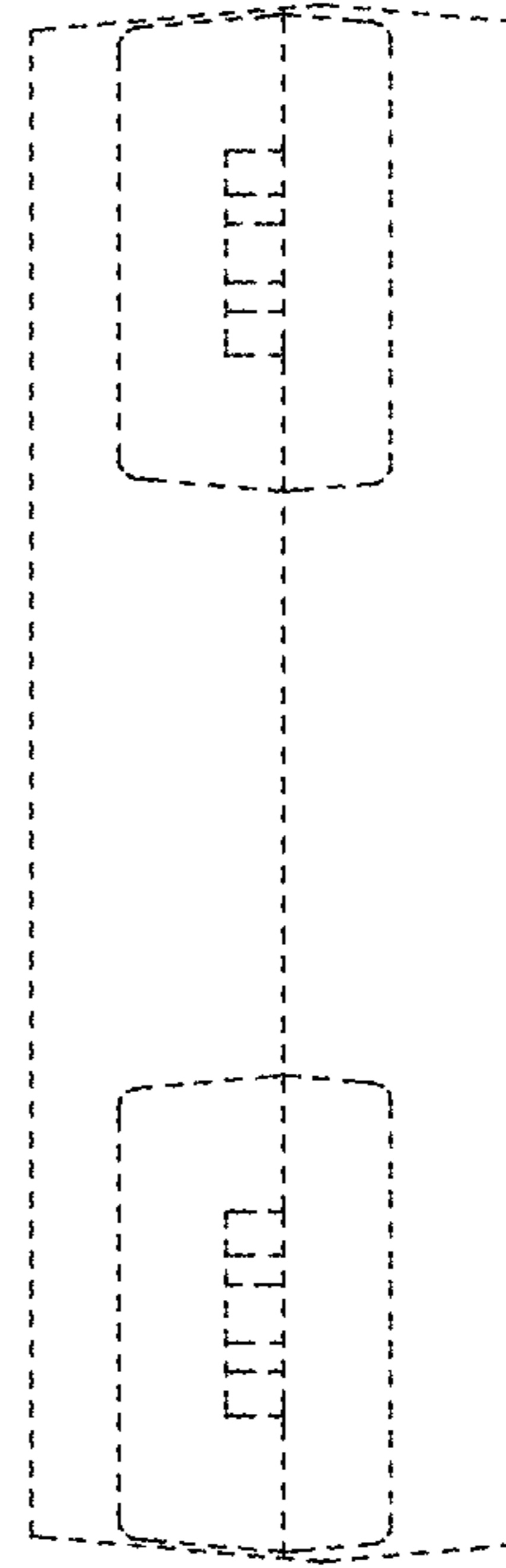


FIG. 5

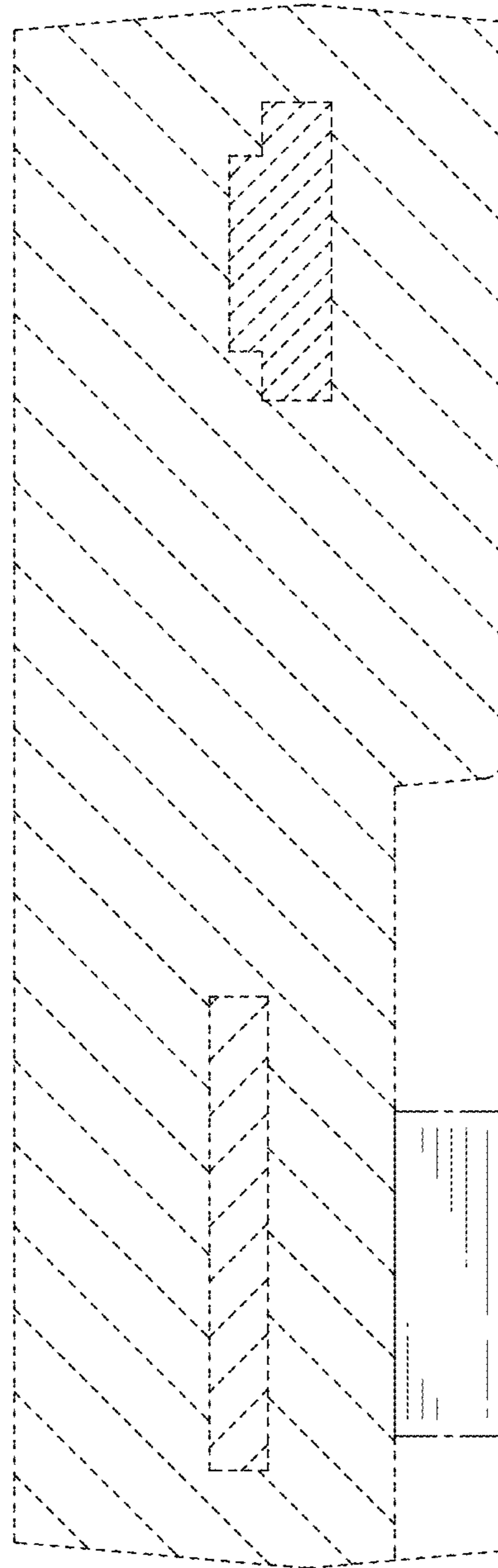


FIG.6

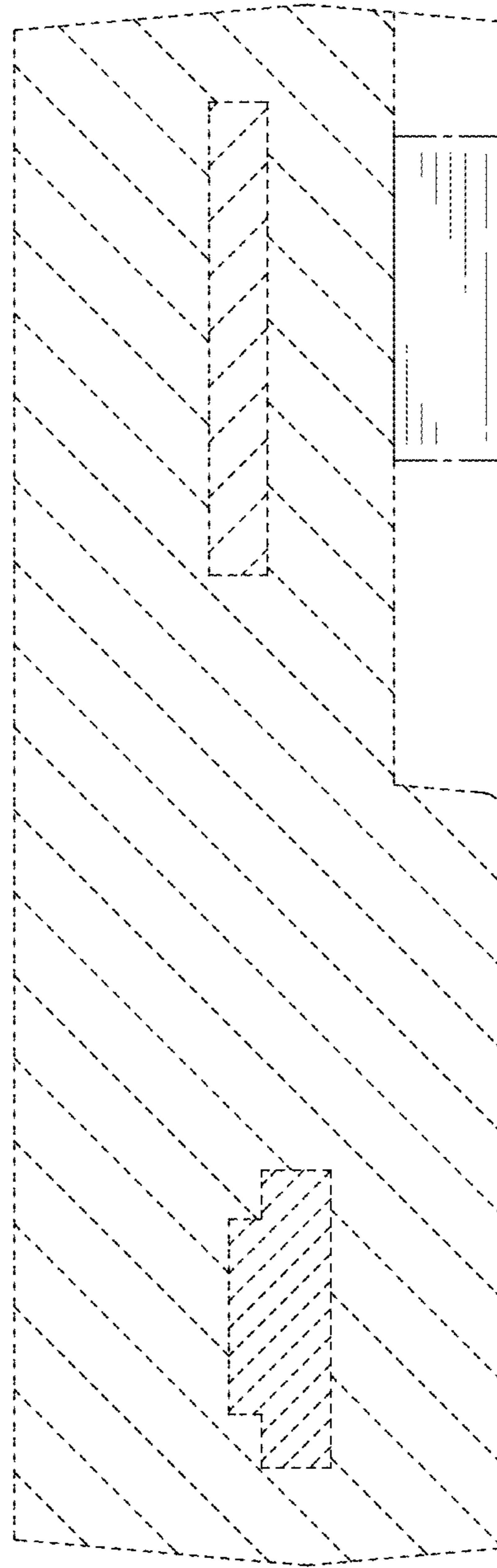


FIG.7