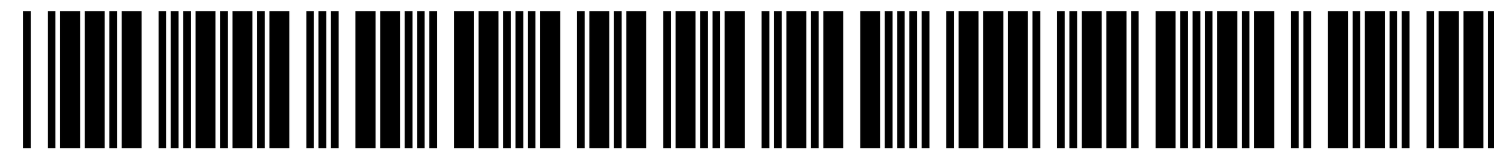


US00D926715S

(12) **United States Design Patent** (10) **Patent No.: US D926,715 S**

Okabe et al. (45) **Date of Patent: ** Aug. 3, 2021**

(54) **SUPPORT FOR A WAFER FOR FABRICATING A SEMICONDUCTOR**

(71) Applicant: **EPICREW CORPORATION**, Nagasaki (JP)

(72) Inventors: **Akira Okabe**, Nagasaki (JP); **Yukio Takenaga**, Nagasaki (JP)

(73) Assignee: **EPICREW CORPORATION**, Nagasaki (JP)

(**) Term: **15 Years**

(21) Appl. No.: **29/712,911**

(22) Filed: **Nov. 12, 2019**

(30) **Foreign Application Priority Data**

Jul. 29, 2019 (JP) 2019-016842

(51) **LOC (13) Cl.** **13-03**

(52) **U.S. Cl.**

USPC **D13/182**

(58) **Field of Classification Search**

USPC D13/182; D15/144, 144.1; 206/710, 206/711, 712; 118/728, 729, 730, 731, 118/732, 733; 211/41.18; 432/240, 241, 432/253, 258; 156/345.51–345.55

CPC H01L 21/68714; H01L 21/6875; H01L 21/68771; H01L 21/68735; H01L 21/673; H01L 21/67353; H01L 21/67383; C23C 16/458; C23C 16/4581; C23C 16/4582; C23C 16/4583; C23C 16/4584; C23C 16/4587; C23C 16/402; C23C 16/5096; C23C 16/00; C23C 14/50; C23C 14/505; C23C 14/52; C23C 14/54; C23C 14/541; C23C 14/542; C23C 14/548; H01J 27/20; H01J 27/32715; C23F 1/00

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,572,814	B2 *	6/2003	Shamoulian	H02N 13/00 264/605
D552,565	S *	10/2007	Nakamura	D13/182
D606,952	S *	12/2009	Lee	D13/182
D614,593	S *	4/2010	Lee	D13/182
D616,394	S *	5/2010	Sato	D13/182
D616,395	S *	5/2010	Sato	D13/182
D784,276	S *	4/2017	Tiner	D13/182
D819,580	S *	6/2018	Krishnan	D13/182
D830,981	S *	10/2018	Jeong	D13/182
D864,134	S *	10/2019	Watarai	D13/182
10,854,498	B2 *	12/2020	Shoji	C23C 16/402
2003/0029570	A1 *	2/2003	Kawamura	H01L 21/68735 156/345.51
2004/0124413	A1 *	7/2004	Arai	H01L 21/67259 257/48

FOREIGN PATENT DOCUMENTS

JP	D1399397	9/2010

* cited by examiner

Primary Examiner — Elizabeth J Oswecki

(74) *Attorney, Agent, or Firm* — Levine Bagade Han LLP

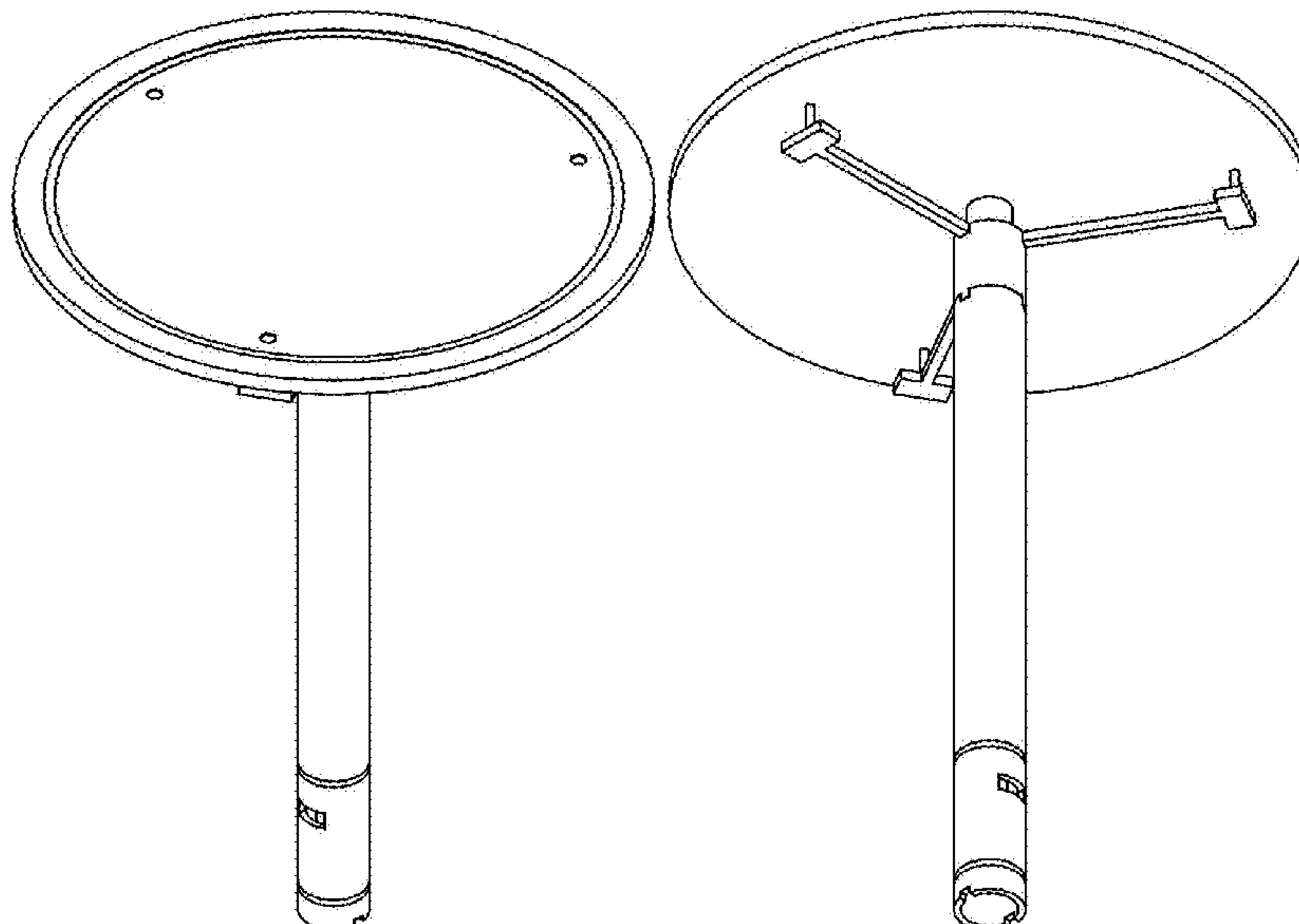
(57) **CLAIM**

The ornamental design for a support for a wafer for fabricating a semiconductor, as shown and described.

DESCRIPTION

FIG. **1** is a front view of a support for a wafer for fabricating a semiconductor showing our new design;
FIG. **2** is a rear view thereof;
FIG. **3** is a top plan view thereof;
FIG. **4** is a bottom plan view thereof;
FIG. **5** is a right side view thereof;
FIG. **6** is a left side view thereof;
FIG. **7** is a top perspective view thereof; and,
FIG. **8** is a bottom perspective view thereof.

1 Claim, 8 Drawing Sheets



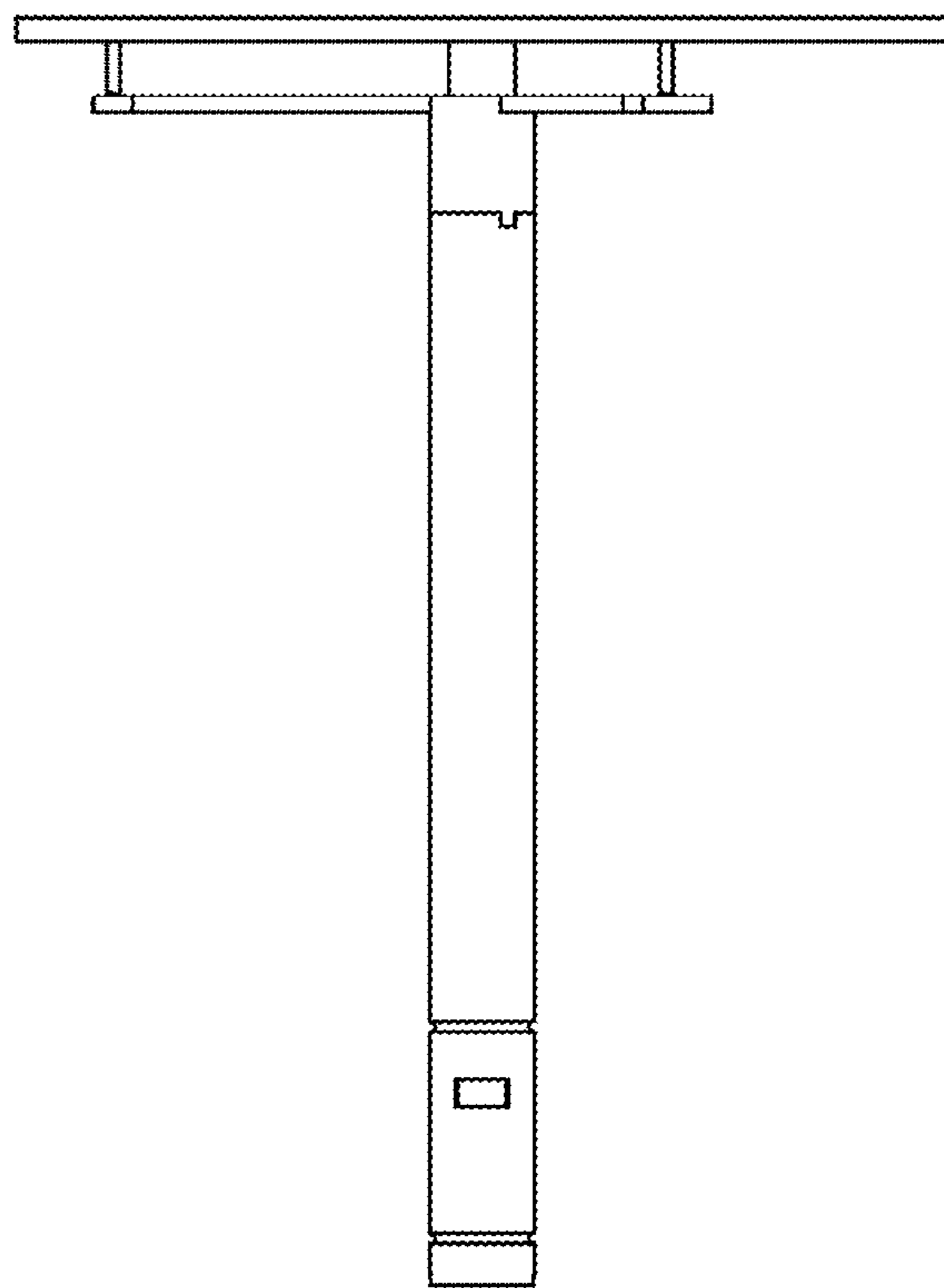


FIG. 1

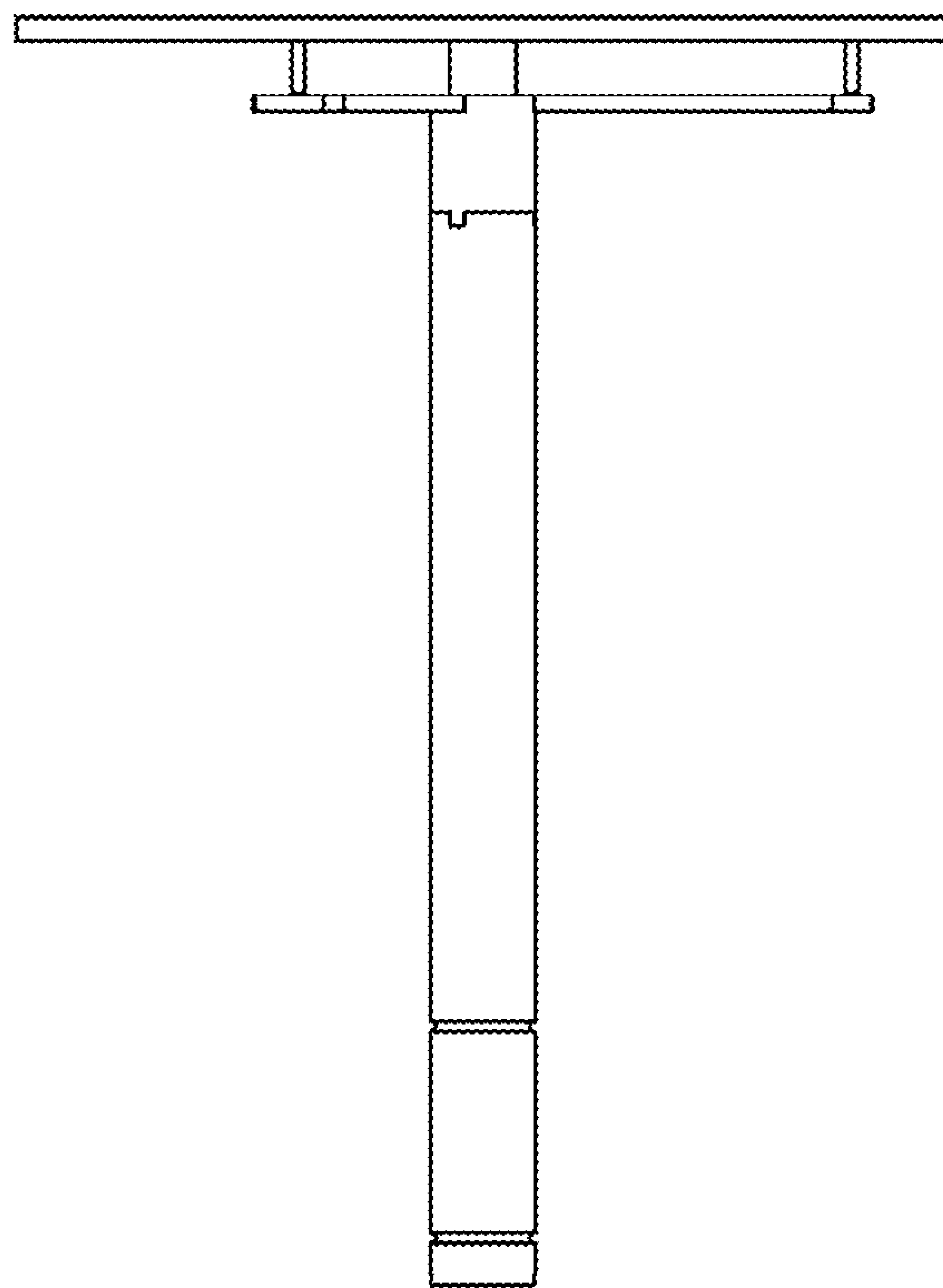


FIG. 2

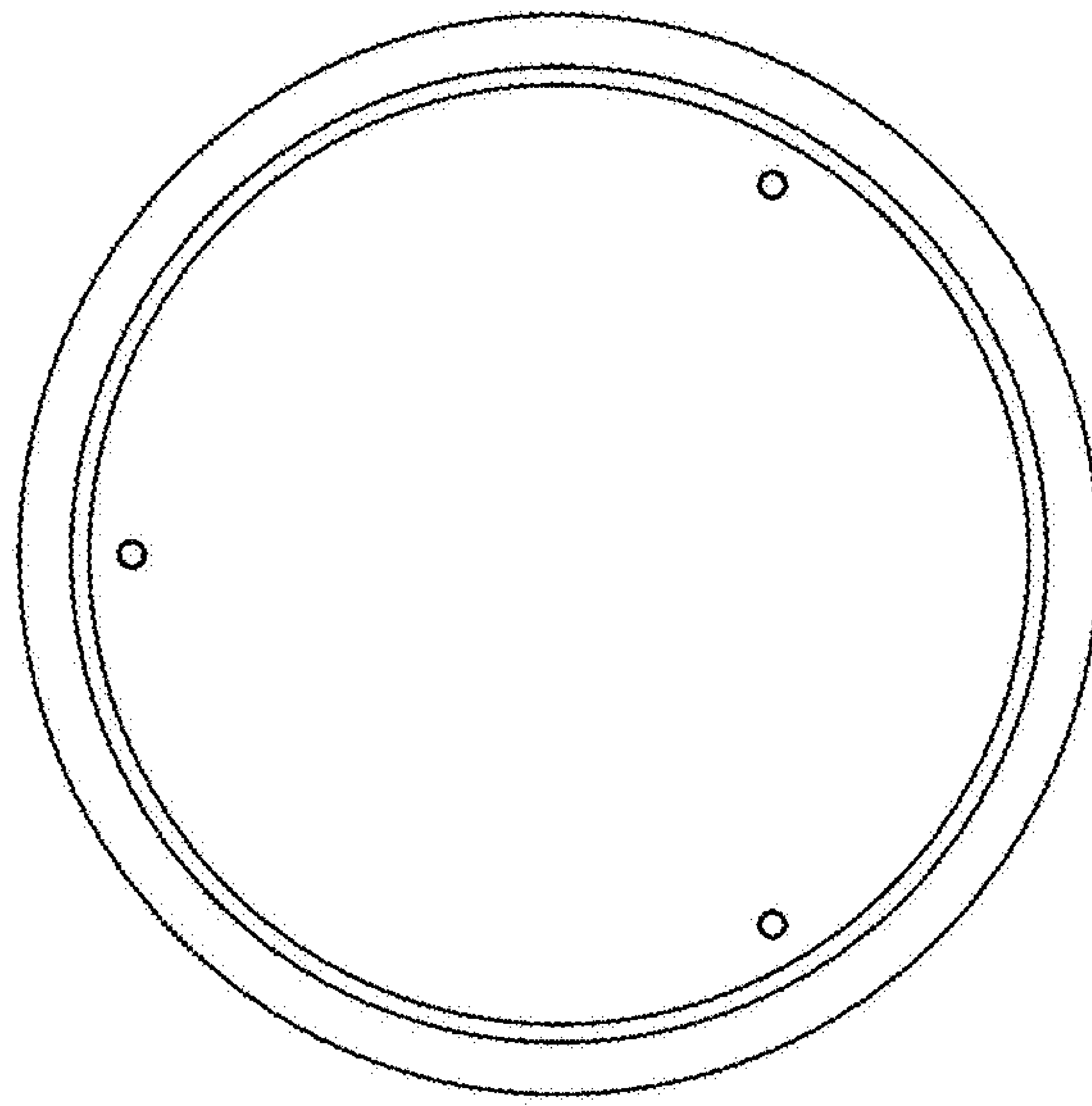


FIG. 3

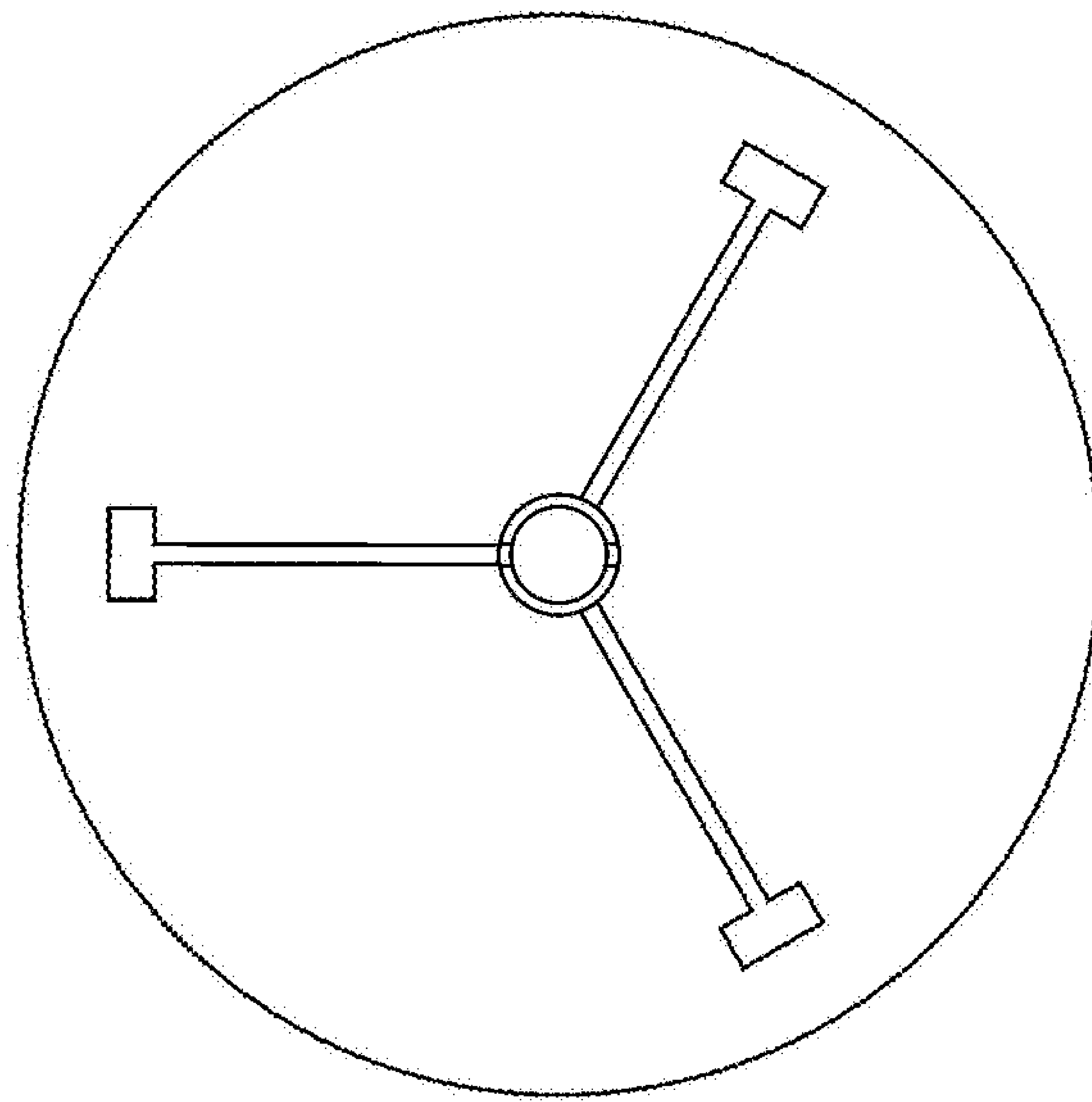


FIG. 4

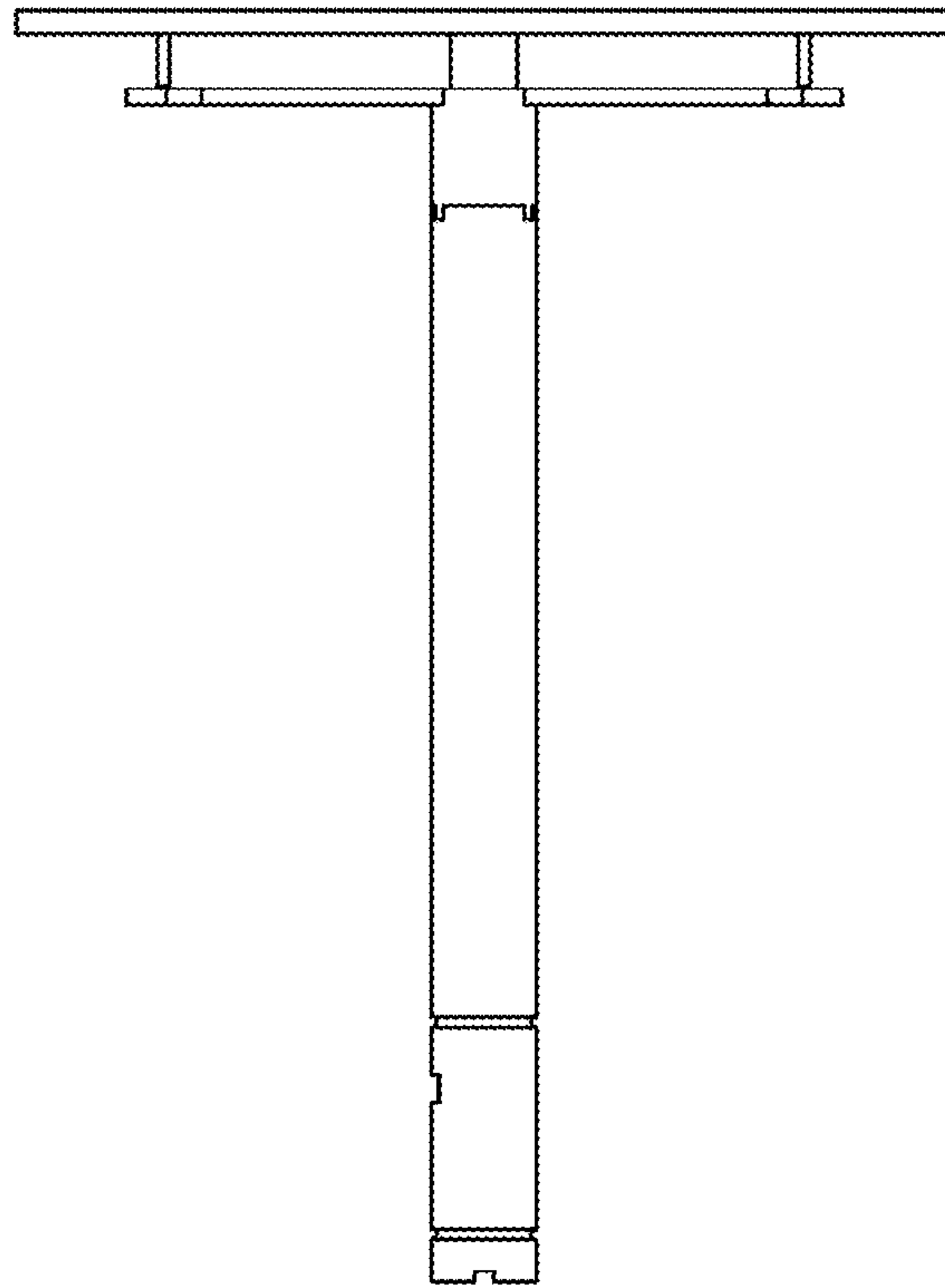


FIG. 5

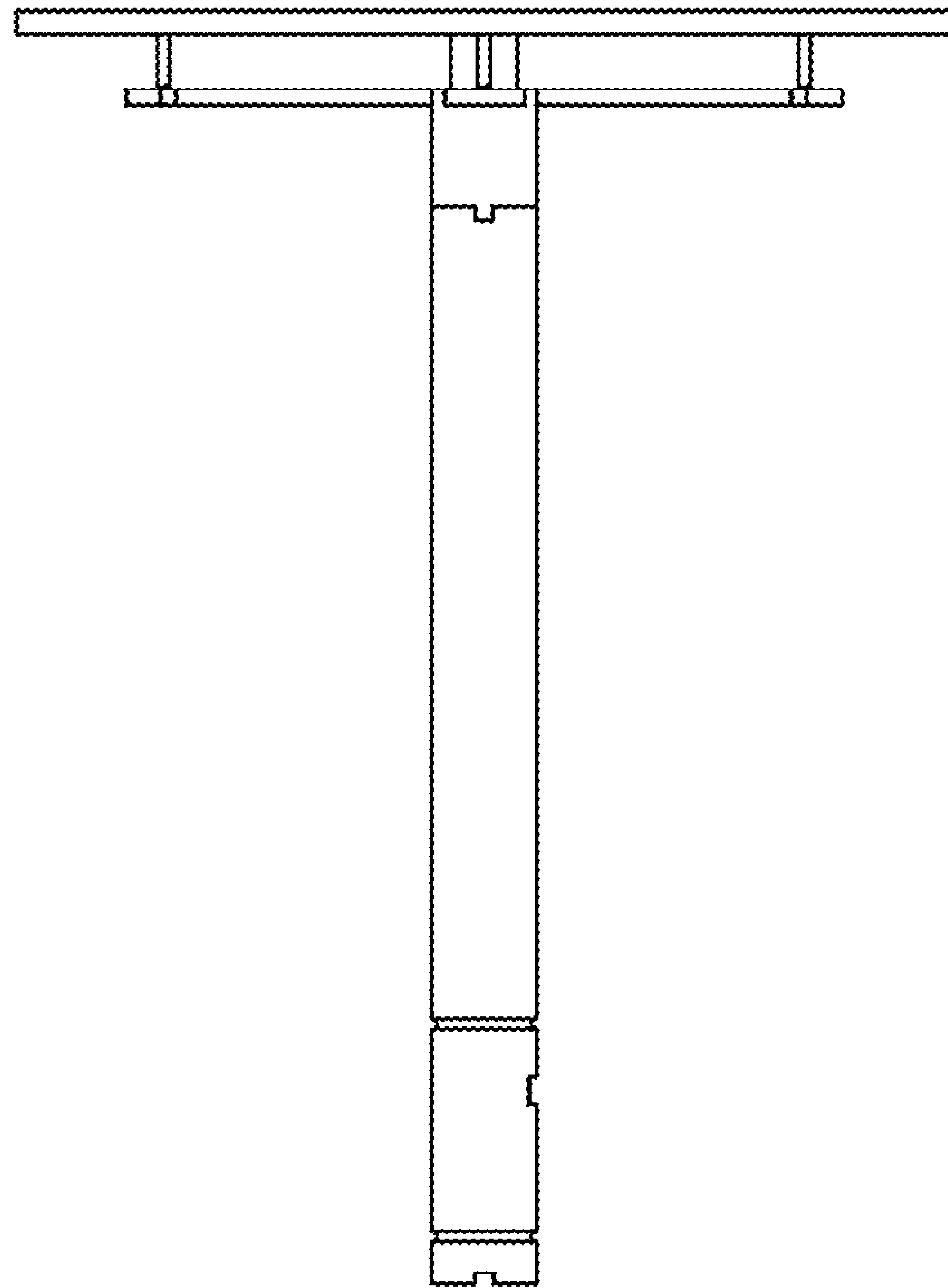


FIG. 6

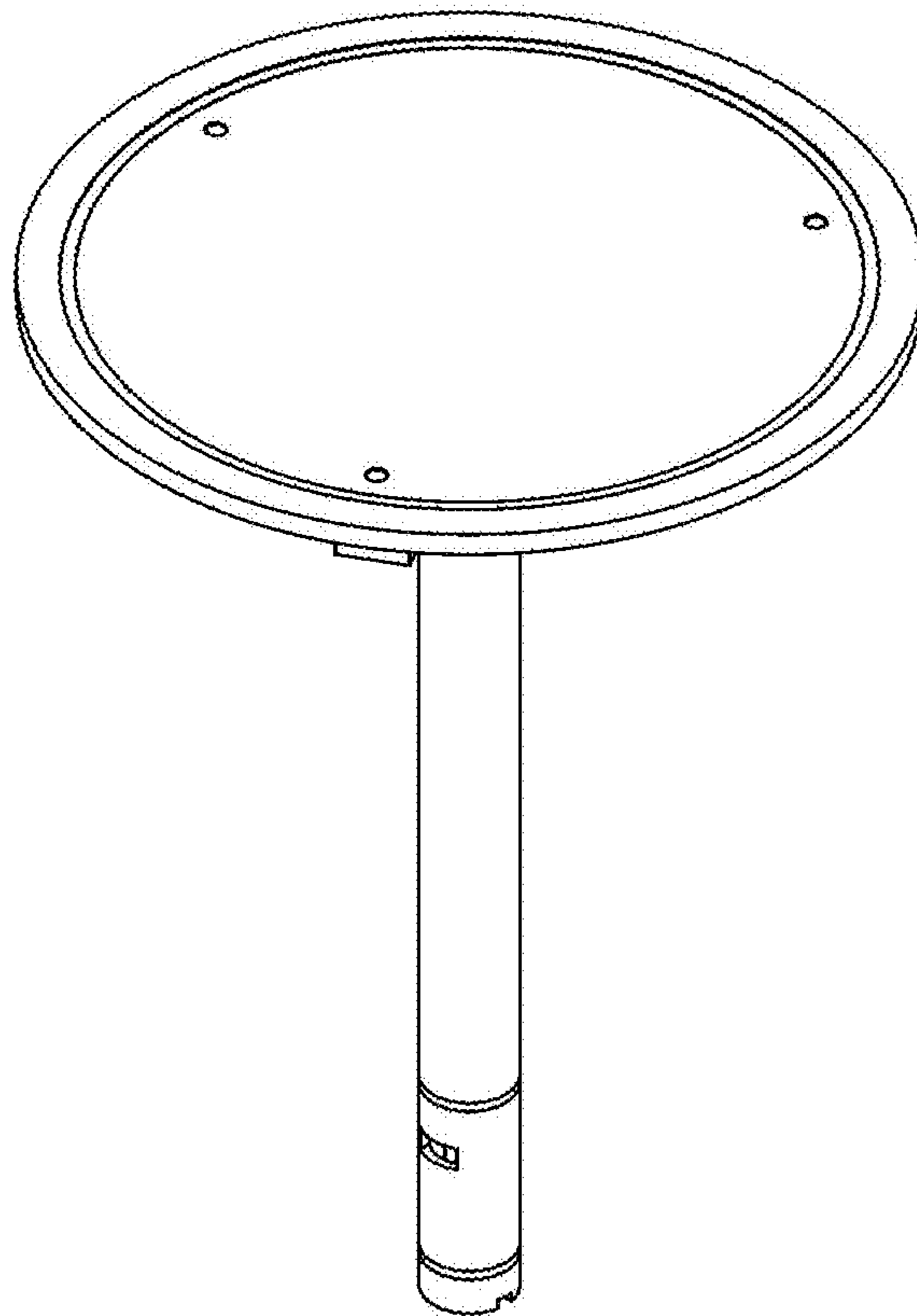


FIG. 7

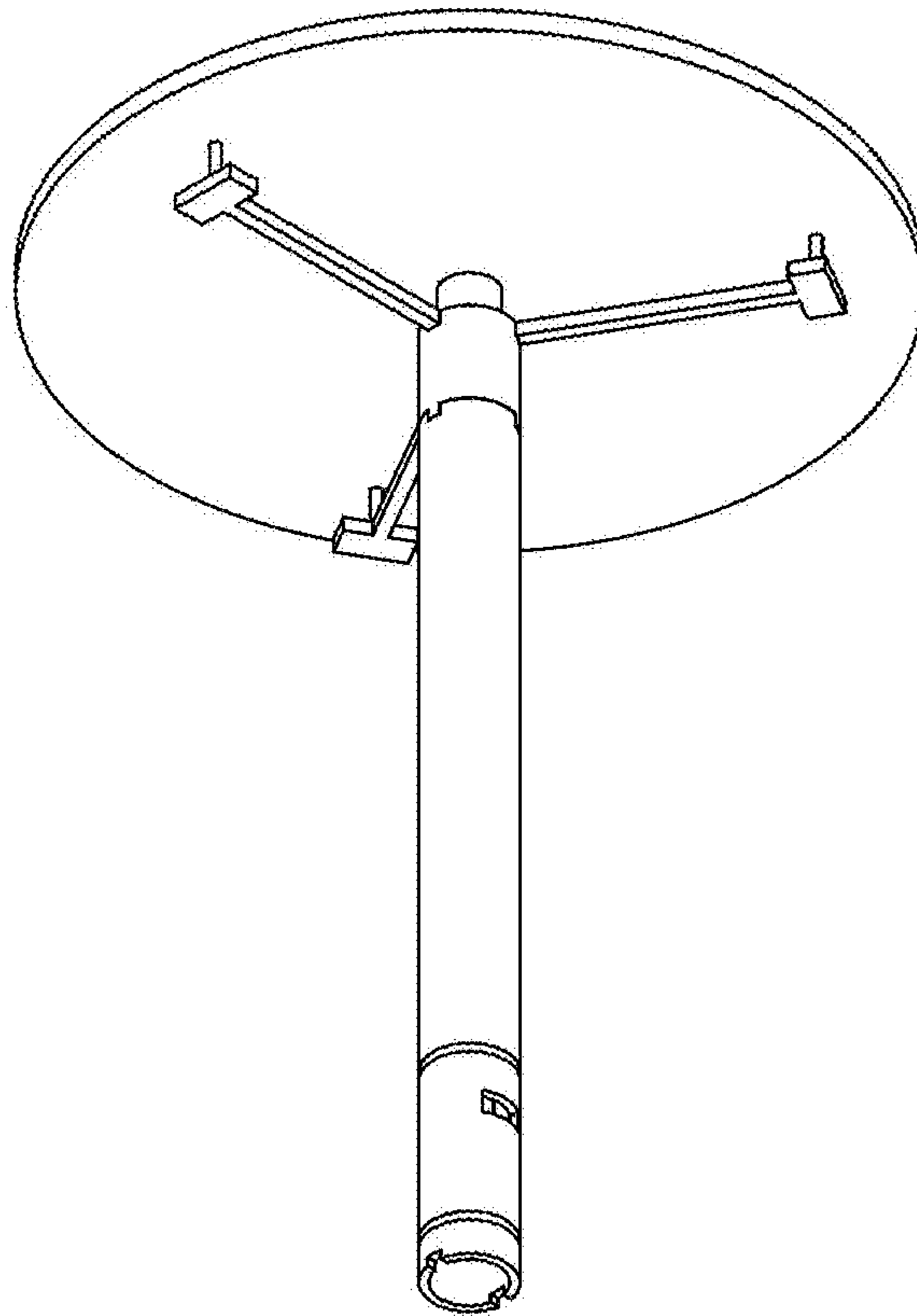


FIG. 8