US00D920265S

(12) United States Design Patent

Huang

(10) Patent No.: US D920,265 S
(45) Date of Patent: ** May 25, 2021

(54) **INTEGRATED CIRCUIT PACKAGE**

(71) Applicant: **China Chippacking Technology Co., Ltd.**, Guangdong (CN)

(72) Inventor: **YiWei Huang**, Guangdong (CN)

(**) Term: **15 Years**

(21) Appl. No.: **29/728,331**

(22) Filed: **Mar. 17, 2020**

(30) **Foreign Application Priority Data**

Sep. 29, 2019 (CN) 201930539500.6

(51) **LOC (13) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182, 110; 174/16.3; 257/666, 678, 257/679, 680, 681, 682, 683, 684, 685, 257/686, 687, 688, 689, 690, 691, 692, 257/693, 694, 695, 696, 697, 700, 730; 361/773, 792, 813; 439/68, 70, 607.22
CPC H01L 27/00; H01L 27/01; H01L 27/013; H01L 27/016; H01L 27/02; H01L 27/0203; H01L 27/0207; H01L 27/04; H01L 27/06; H01L 27/0605; H01L 27/07; H01L 27/08; H01L 27/14618; H01L 21/4846; H01L 21/4853; H01L 21/4857; H01L 21/56; H01L 21/561; H01L 21/563; H01L 21/565; H01L 21/566; H01L 21/568; H01L 23/498; H01L 23/49805; H01L 23/3114; H01L 23/3121; H01L 23/3107; H01L 23/481; H01L 23/5384; H01L 23/528; H01L 33/48; H01L 33/52; H01L 33/54; H01L 33/62; H01L 24/02; H01L 24/97; H01L 31/0203; H01L 25/105
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,220,298	A *	6/1993	Nagase	H01L 23/552 257/E23.114
D355,411	S *	2/1995	Sadigh-Behzadi	D13/182
D396,211	S *	7/1998	Enomoto	D13/182
D396,212	S *	7/1998	Enomoto	D13/182
D396,213	S *	7/1998	Enomoto	D13/182
D397,092	S *	8/1998	Sano	D13/182
D416,236	S *	11/1999	Kobayashi	D13/182
D489,338	S *	5/2004	Seddon	D13/182
D510,728	S *	10/2005	Celaya	D13/182
9,142,531	B1 *	9/2015	Camacho	H01L 24/97
9,184,122	B2 *	11/2015	Jin	H01L 23/49811
9,299,661	B2 *	3/2016	Kapusta	H01L 21/561
9,355,962	B2 *	5/2016	Lee	H01L 25/105

(Continued)

OTHER PUBLICATIONS

What is µMAX IC package? https://electronics.stackexchange.com/questions/15839/what-is-%c2%b5max-ic-package, Jun. 23, 2011. (Year: 2011).*

Primary Examiner — Elizabeth J Oswecki
(74) *Attorney, Agent, or Firm* — Prakash Nama; Global IP Services, PLLC

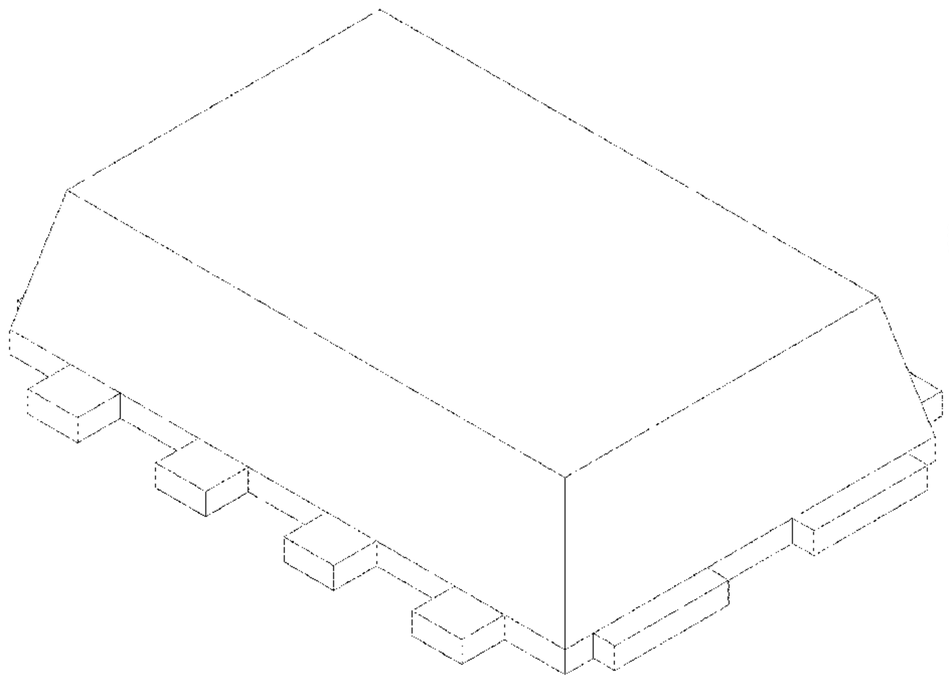
(57) **CLAIM**

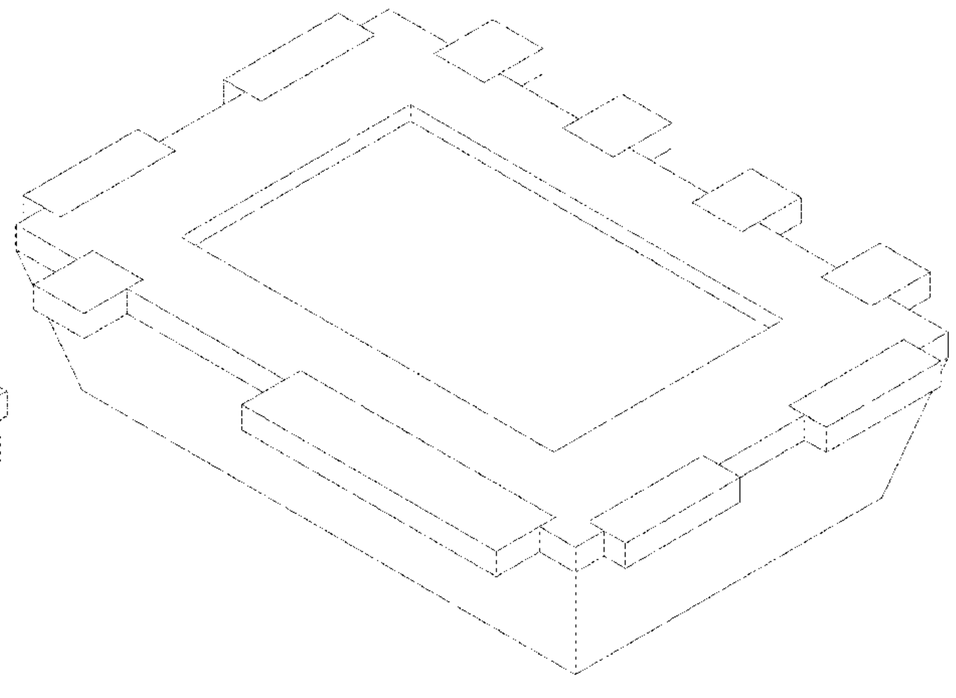
The ornamental design for an integrated circuit package, as shown.

DESCRIPTION

FIG. **1** is a front elevational view of an integrated circuit package showing my new design;
FIG. **2** is a rear elevational view thereof;
FIG. **3** is a left side elevational view thereof;
FIG. **4** is a right side elevational view thereof;
FIG. **5** is a top plan view thereof;
FIG. **6** is a bottom plan view thereof;
FIG. **7** is a front perspective view thereof; and,
FIG. **8** is a rear perspective view thereof.

1 Claim, 8 Drawing Sheets





(56) **References Cited**

U.S. PATENT DOCUMENTS

9,437,512	B2 *	9/2016	Gregorich	H01L 23/49838
9,530,945	B2 *	12/2016	Badehi	H01L 31/125
9,653,442	B2 *	5/2017	Yu	H01L 24/17
D796,459	S *	9/2017	Iwai	D13/182
9,859,253	B1 *	1/2018	Jayaraman	H01L 25/50
10,134,685	B1 *	11/2018	Chen	H01L 24/19
10,615,151	B2 *	4/2020	Hu	H01L 24/32
10,636,757	B2 *	4/2020	Yang	H01L 24/20
10,685,896	B2 *	6/2020	Liu	H01L 23/3128
10,790,162	B2 *	9/2020	Tsai	H01L 23/5226
D902,164	S *	11/2020	Kondo	D13/182
10,867,879	B2 *	12/2020	Yu	H01L 23/5226

* cited by examiner

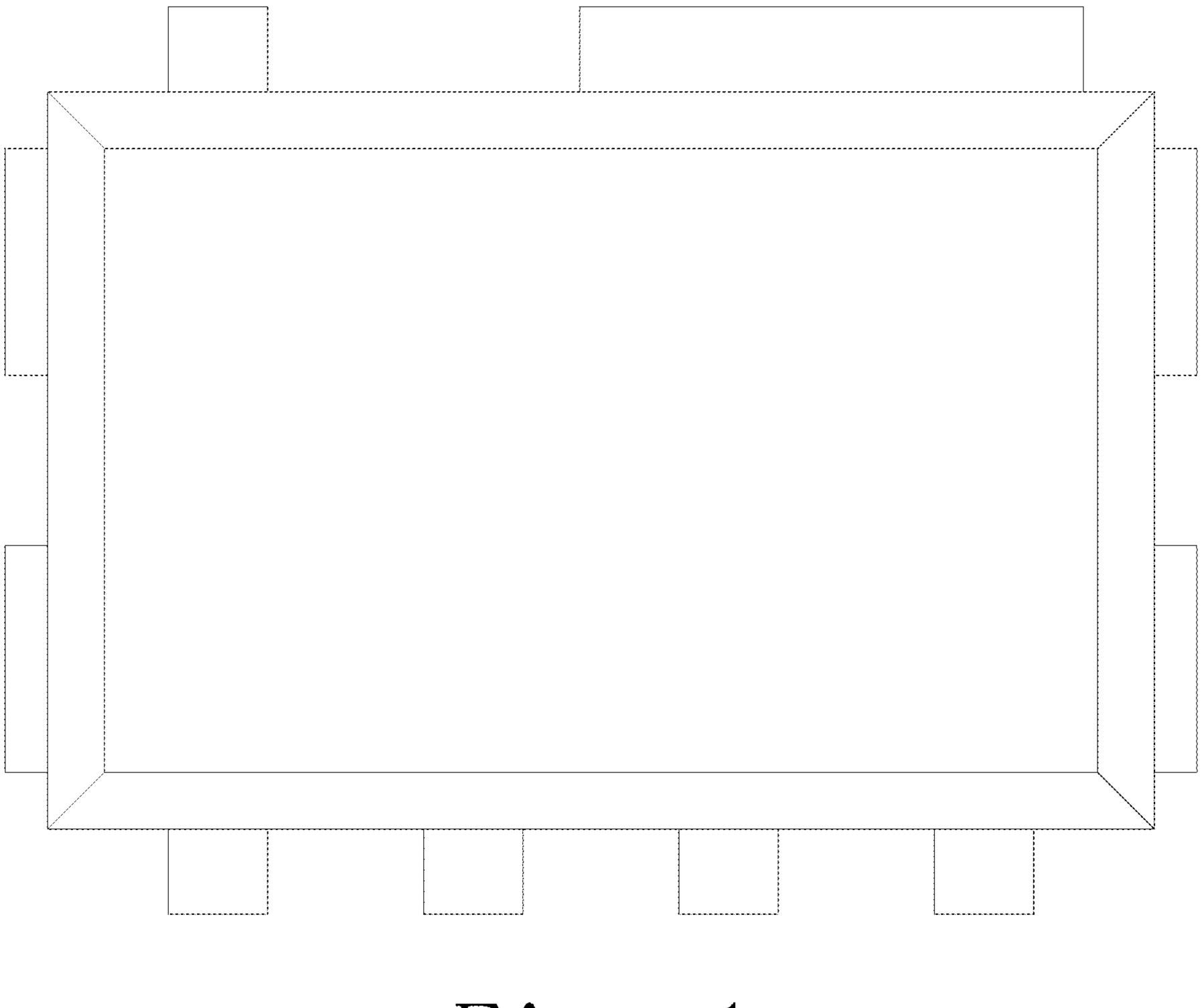


Fig. 1

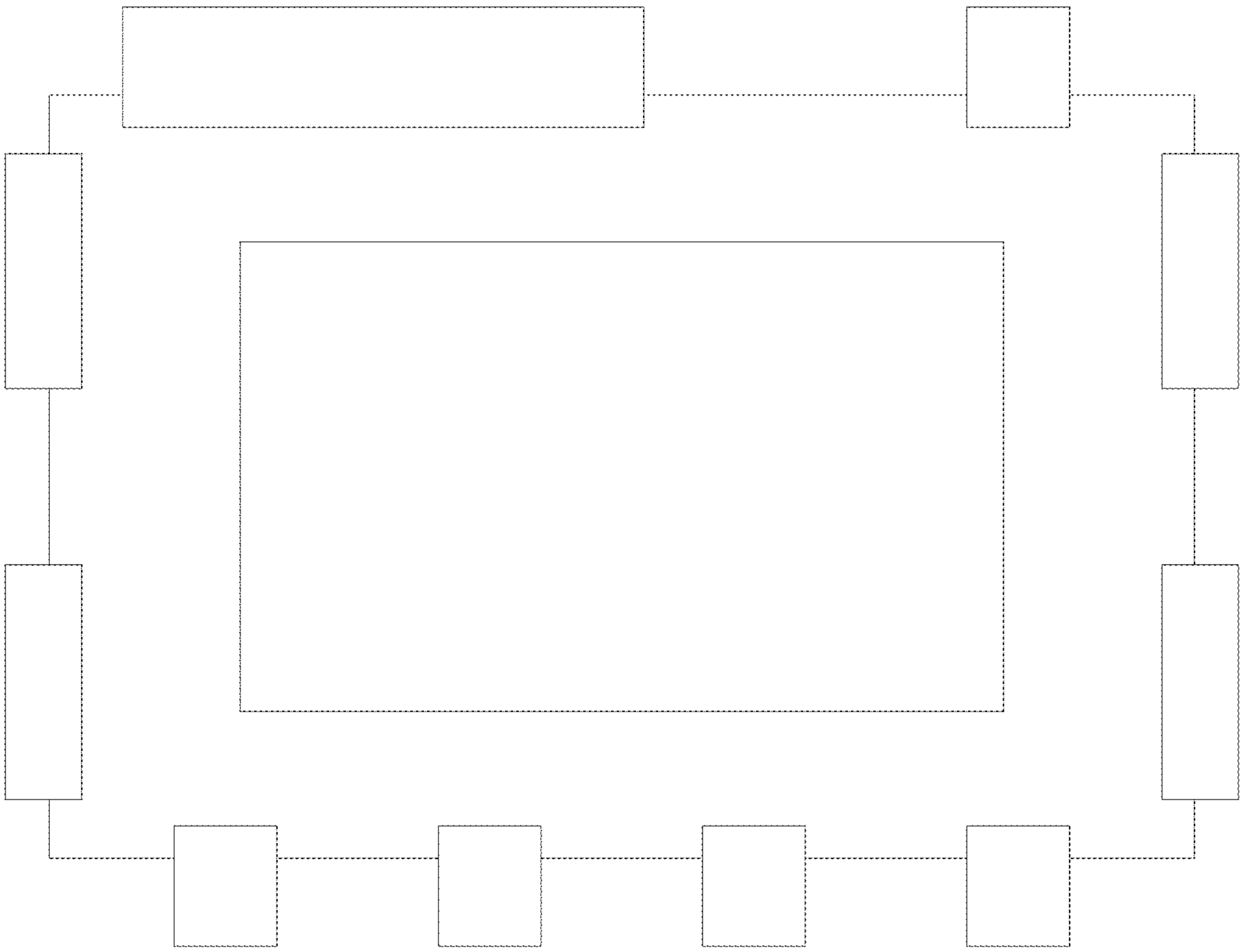


Fig. 2

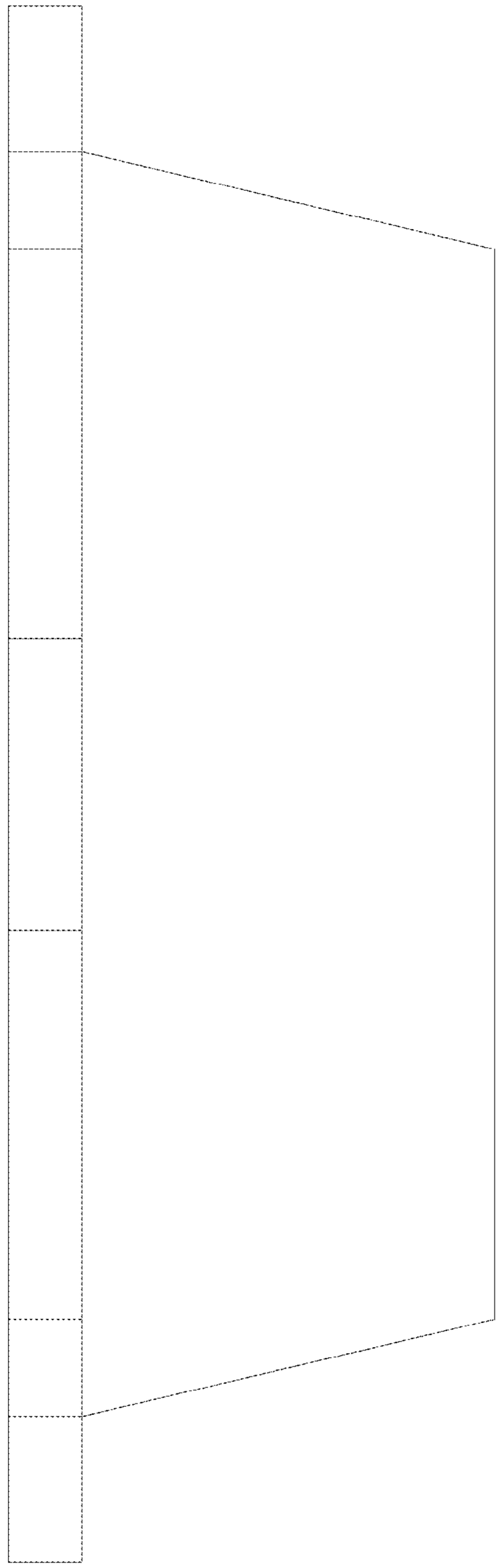


Fig. 3

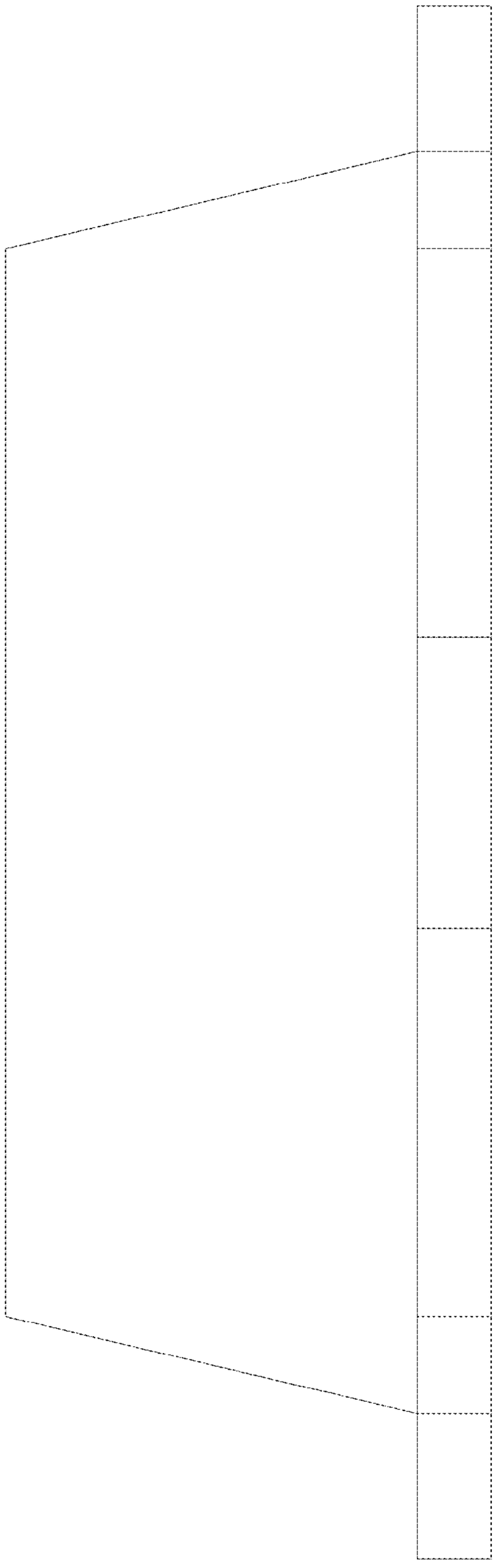


Fig. 4

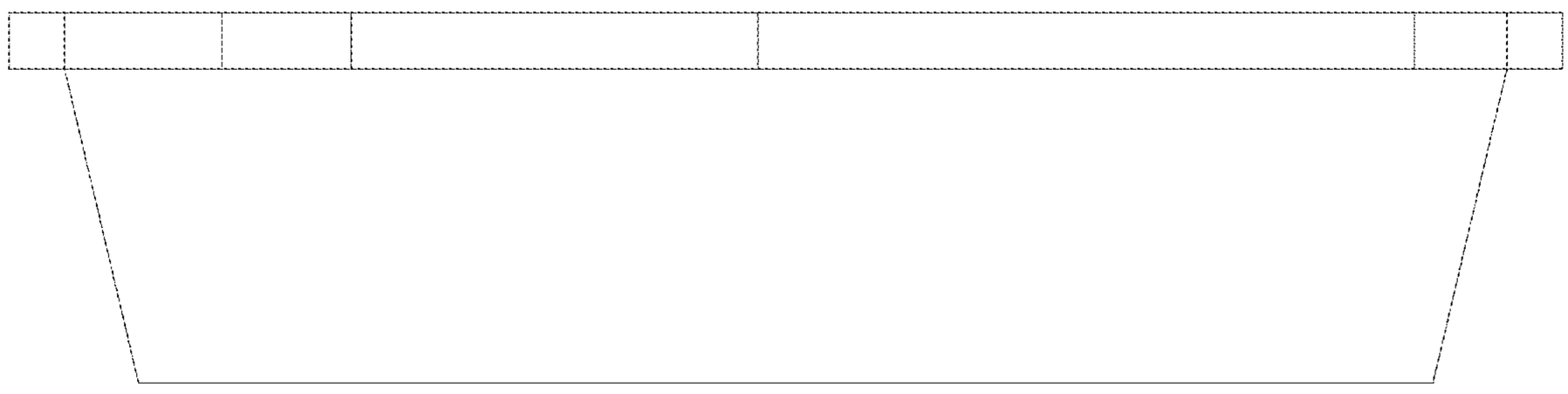


Fig. 5

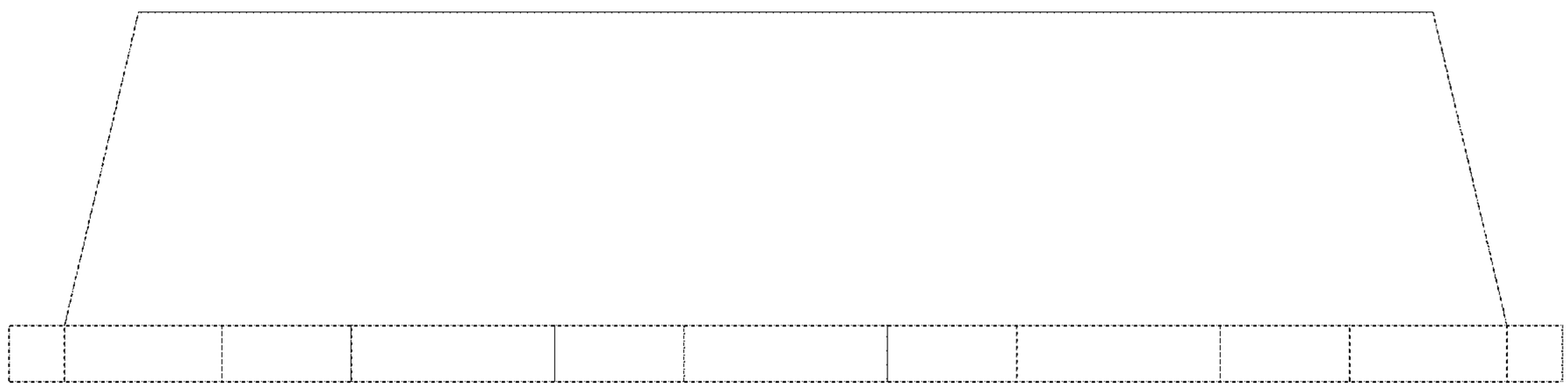


Fig. 6

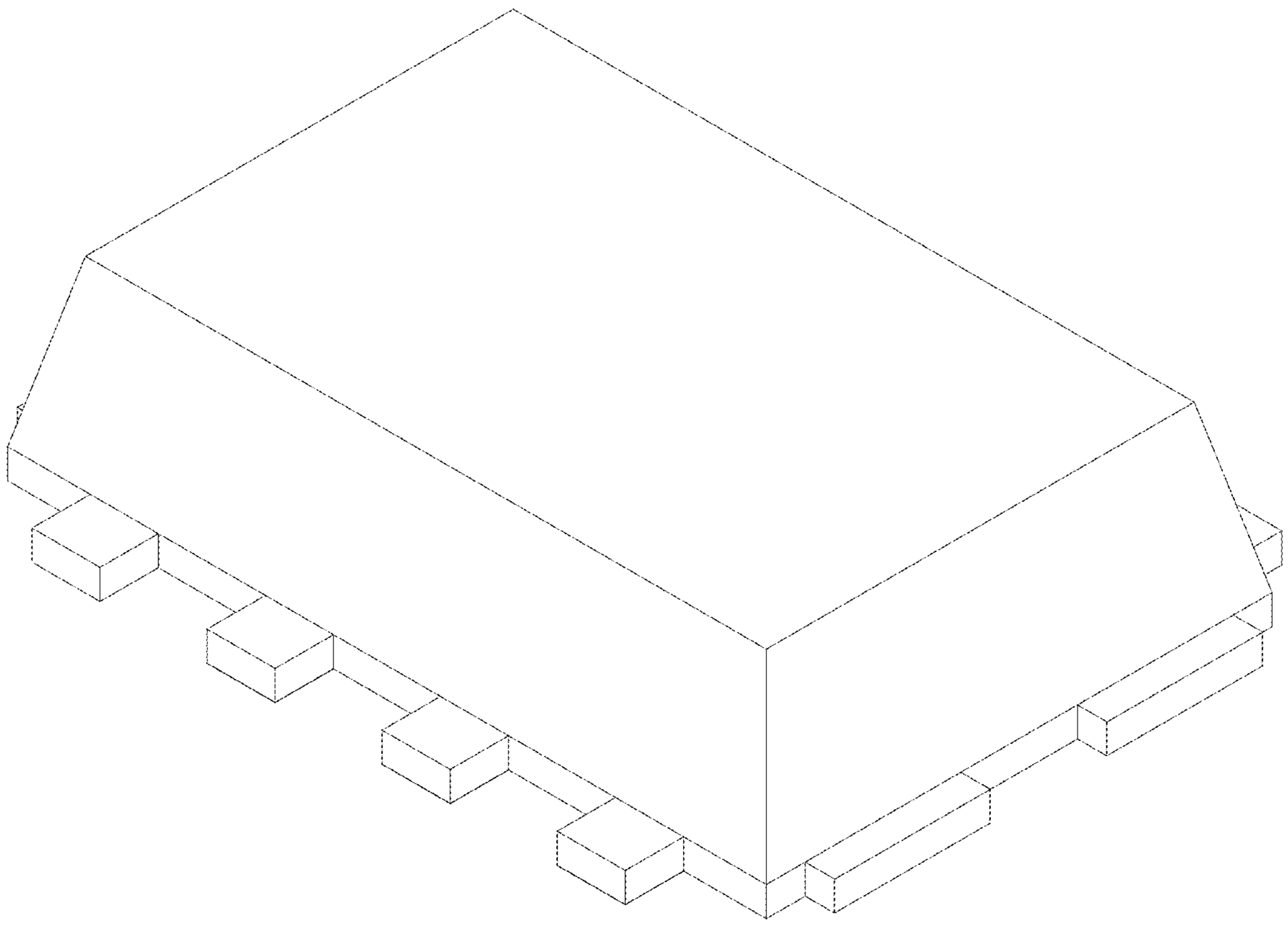


Fig. 7

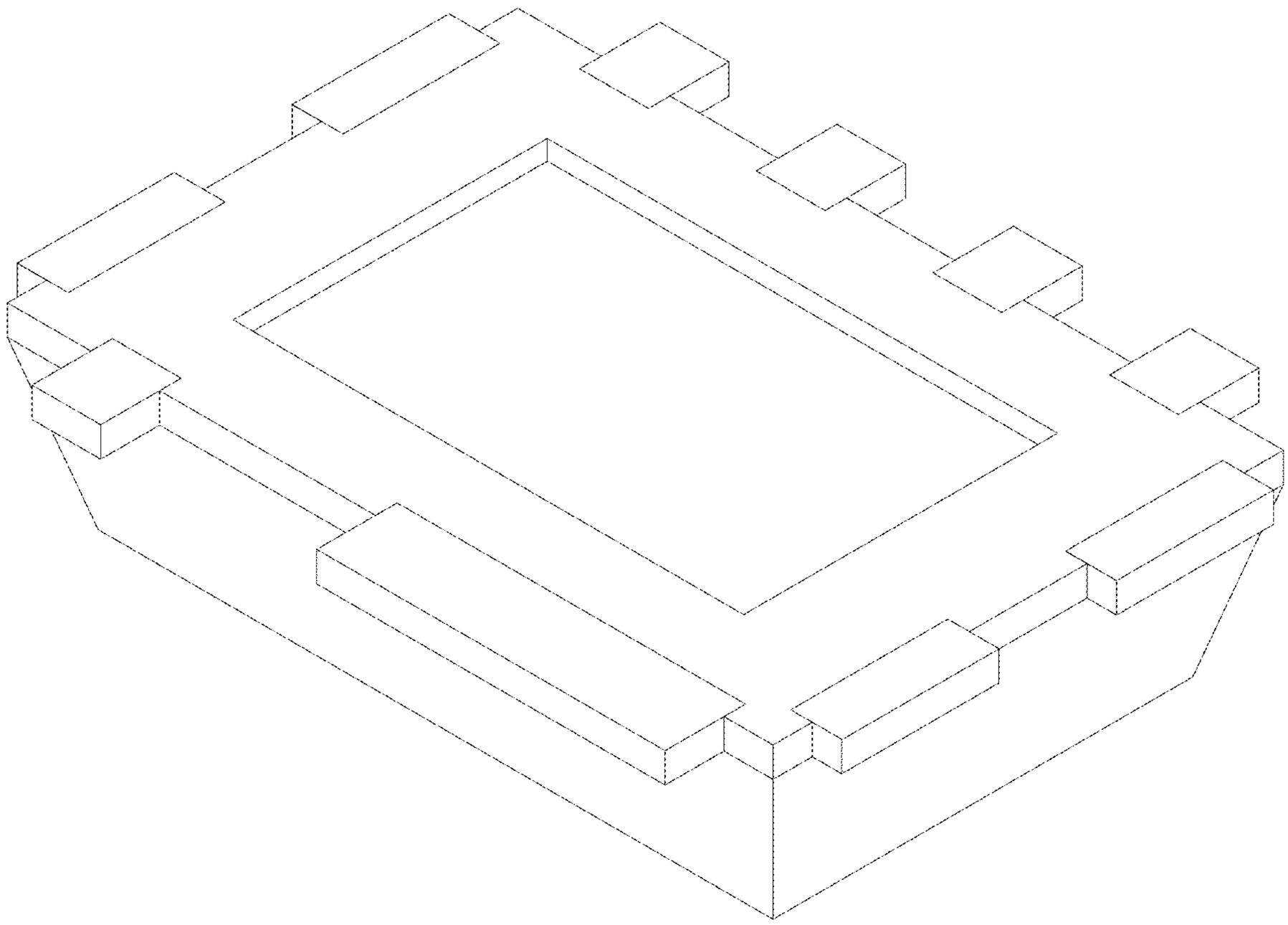


Fig. 8