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(12) United States Design Patent

Yamanaka et al.

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(54) **SEMICONDUCTOR DEVICE**

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(73) Assignee: **SANSHA ELECTRIC MANUFACTURING CO., LTD.**, Osaka (JP)

(**) Term: **15 Years**

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(51) **LOC (13) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182
CPC H01L 21/00; H01L 21/02; H01L 21/4814; H01L 21/4846; H01L 21/4871; H01L 21/67144; H01L 2224/42; H01L 2224/43; H01L 2224/01; H01L 2224/08055; H01L 2224/08054; H01L 23/12; H01L 23/13; H01L 23/14; H01L 23/147; H01L 23/00; H01L 23/48; H01L 23/4926; H01L 23/495; H01L 23/49517; H01L 23/498; H01L 23/49805; H01L 23/49811; H01L 23/49861; H01L 23/49866; H01L 23/49872; H01L 23/49575; H01L 23/49579; H01L 2924/171; H01L 2924/1711; H01L 2924/1715; H01L 2924/181; H01L 2924/1811; H01L 2924/1815; H01L 2924/19042; H01L 2924/1905
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,408,128	A *	4/1995	Furnival	H01L 23/49811	257/690
D364,383	S *	11/1995	Yamada	D13/146	
D364,384	S *	11/1995	Shimizu	D13/146	
D364,385	S *	11/1995	Shimizu	D13/146	
D441,726	S *	5/2001	Sofue	D13/182	
D464,618	S *	10/2002	Ando	D13/110	
7,425,757	B2 *	9/2008	Takubo	H01L 25/072	257/678
8,526,199	B2 *	9/2013	Matsumoto	H01L 23/3735	361/820
D703,625	S *	4/2014	Lim	D13/182	
D704,670	S *	5/2014	Chen	D13/182	
D704,671	S *	5/2014	Chen	D13/182	
D710,317	S *	8/2014	Chen	D13/182	
D710,318	S *	8/2014	Chen	D13/182	
D710,319	S *	8/2014	Chen	D13/182	
D748,595	S *	2/2016	Bertalan	D13/182	
D761,746	S *	7/2016	Toyoshima	D13/182	

(Continued)

Primary Examiner — Elizabeth J Oswecki
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(57) **CLAIM**

The ornamental design for a semiconductor device, as shown and described.

DESCRIPTION

FIG. **1** is a front view of a semiconductor device, showing our new design;
FIG. **2** is a rear view thereof;
FIG. **3** is a top view thereof;
FIG. **4** is a bottom view thereof;
FIG. **5** is a left-side view thereof;
FIG. **6** is a right-side view thereof;
(Continued)

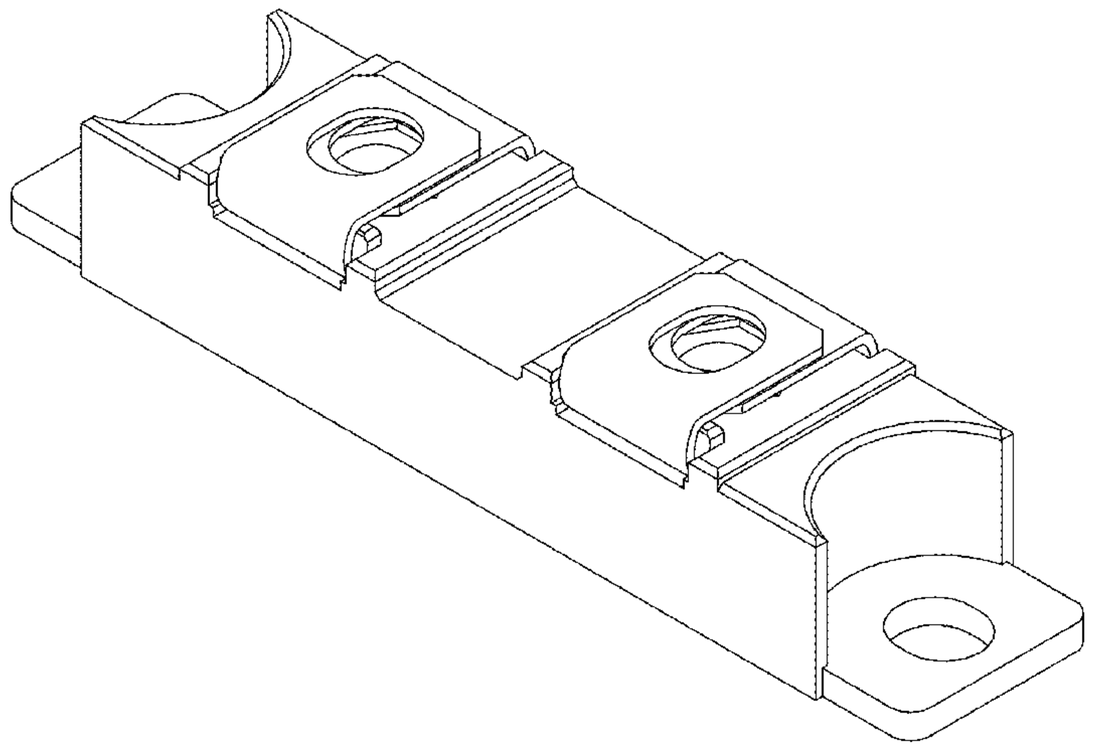

FIG. **7** is a front top perspective view thereof;
FIG. **8** is a rear top perspective view thereof; and,
FIG. **9** is a rear side perspective view thereof.

1 Claim, 9 Drawing Sheets

(56) **References Cited**

U.S. PATENT DOCUMENTS

D762,185	S *	7/2016	Muehlensiep	D13/182
D762,597	S *	8/2016	Bertalan	D13/182
9,418,975	B1 *	8/2016	Yoneyama	H01L 23/5386
D766,851	S *	9/2016	Yoneyama	D13/182
D773,412	S *	12/2016	Yoneyama	D13/182
9,660,356	B1 *	5/2017	Nakamura	H05K 7/1432
D790,491	S *	6/2017	Hayashida	D13/182
D798,832	S *	10/2017	Hayashida	D13/182
D827,591	S *	9/2018	Ikeda	D13/182
D884,662	S *	5/2020	Itoh	D13/182
2001/0038143	A1 *	11/2001	Sonobe	H01L 24/49 257/690
2004/0227231	A1 *	11/2004	Maly	H01L 25/072 257/724
2008/0142948	A1 *	6/2008	Matsumoto	H01R 12/52 257/690
2016/0190915	A1 *	6/2016	Horiuchi	H01L 25/072 363/132
2016/0284618	A1 *	9/2016	Tsukamoto	H01L 23/645

* cited by examiner

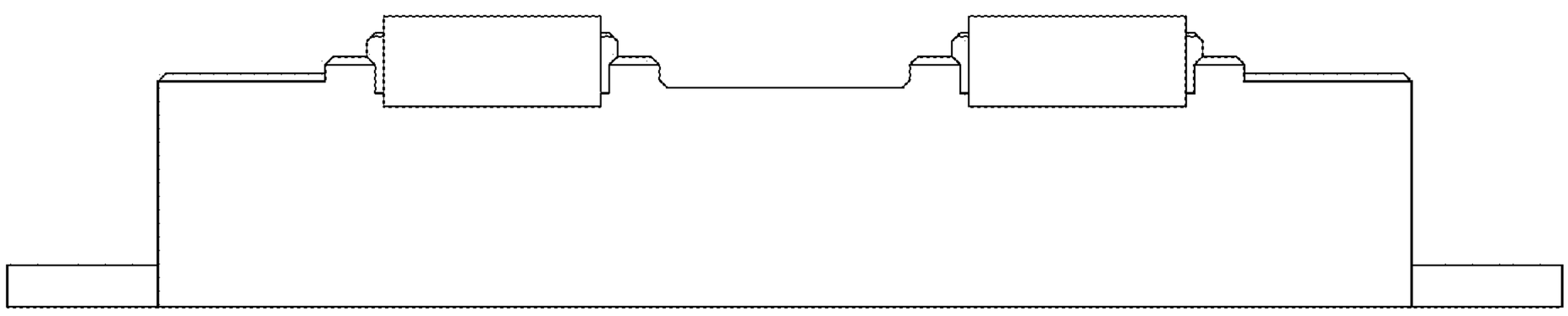

FIG. 1

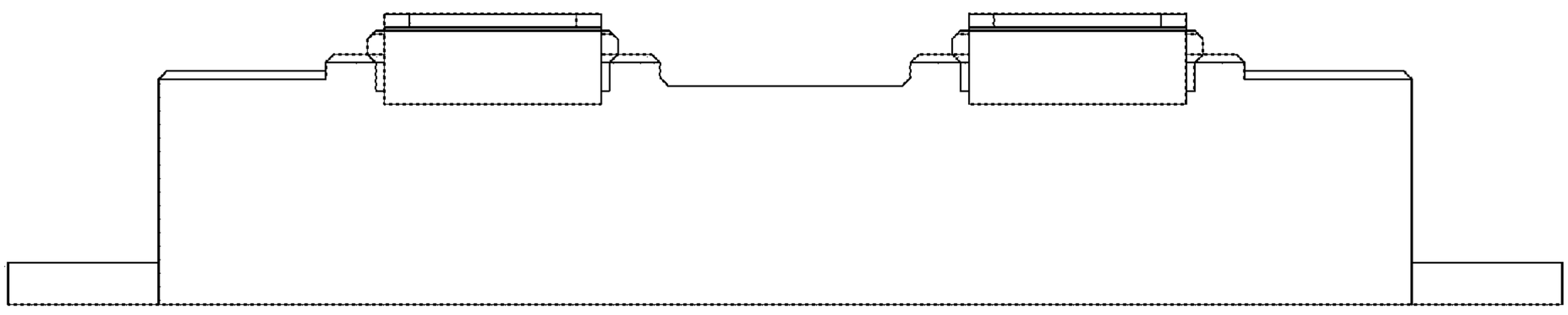

FIG. 2

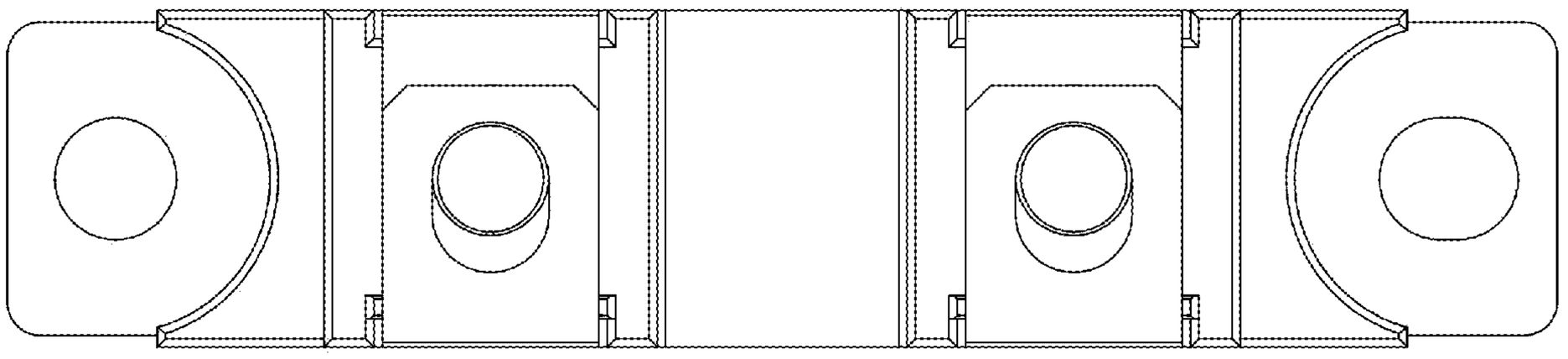

FIG. 3

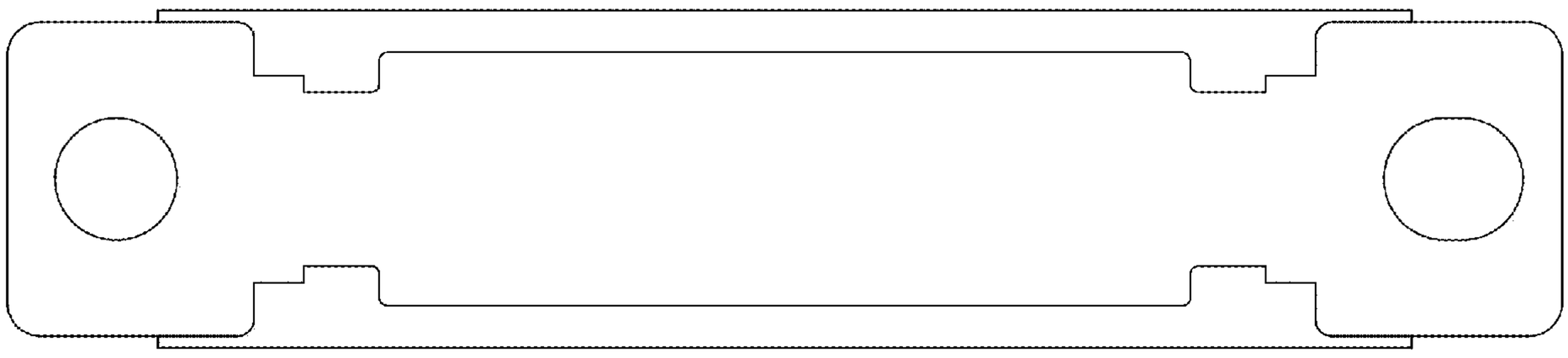

FIG. 4

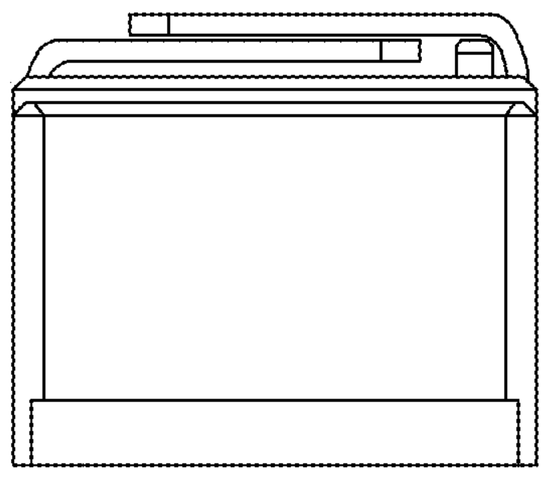

FIG. 5

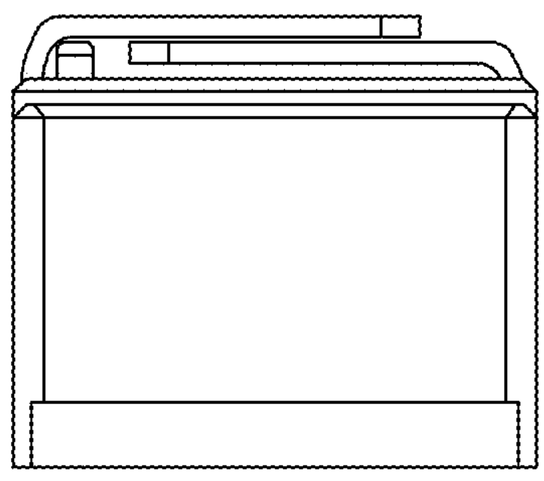

FIG. 6

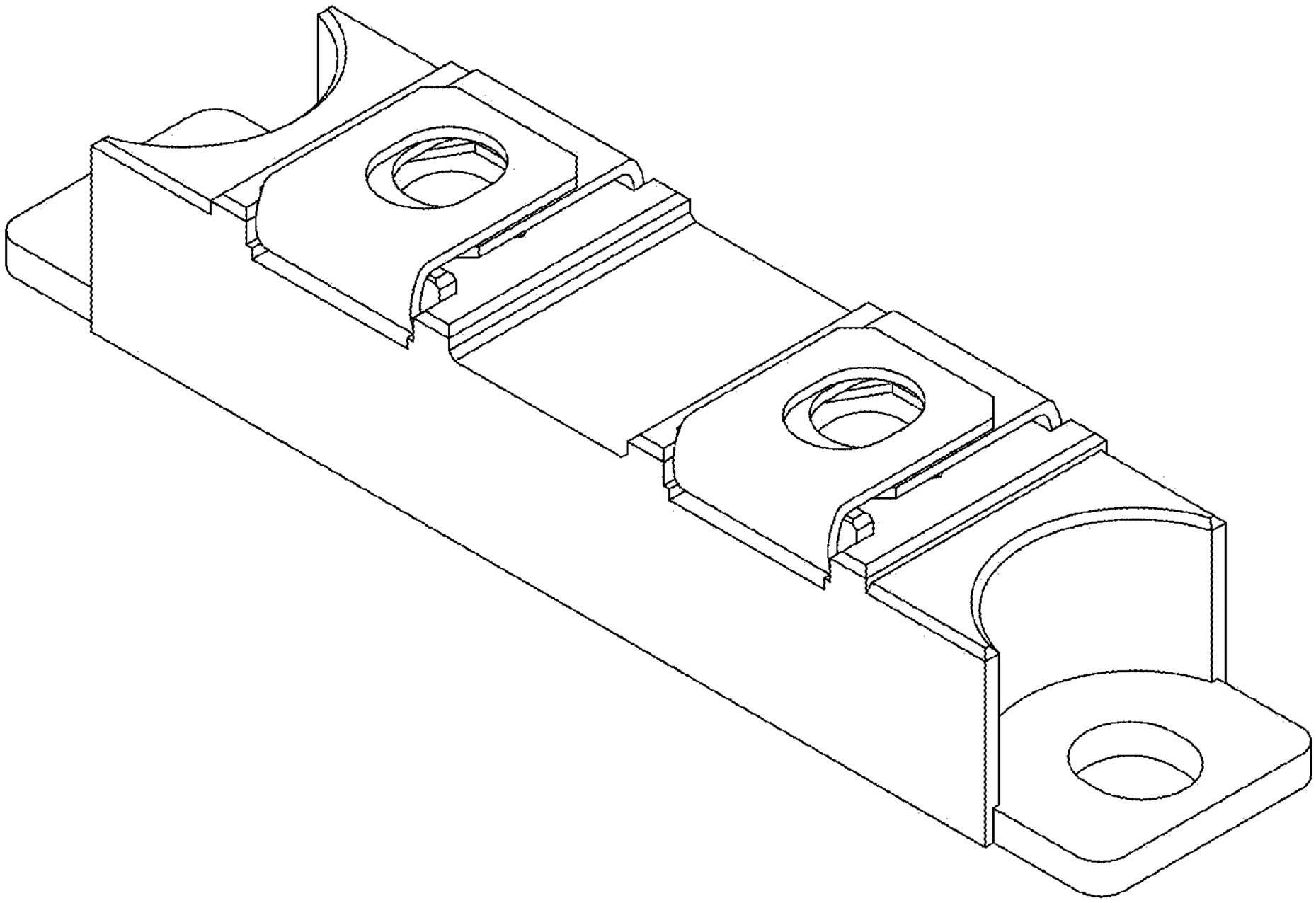

FIG. 7

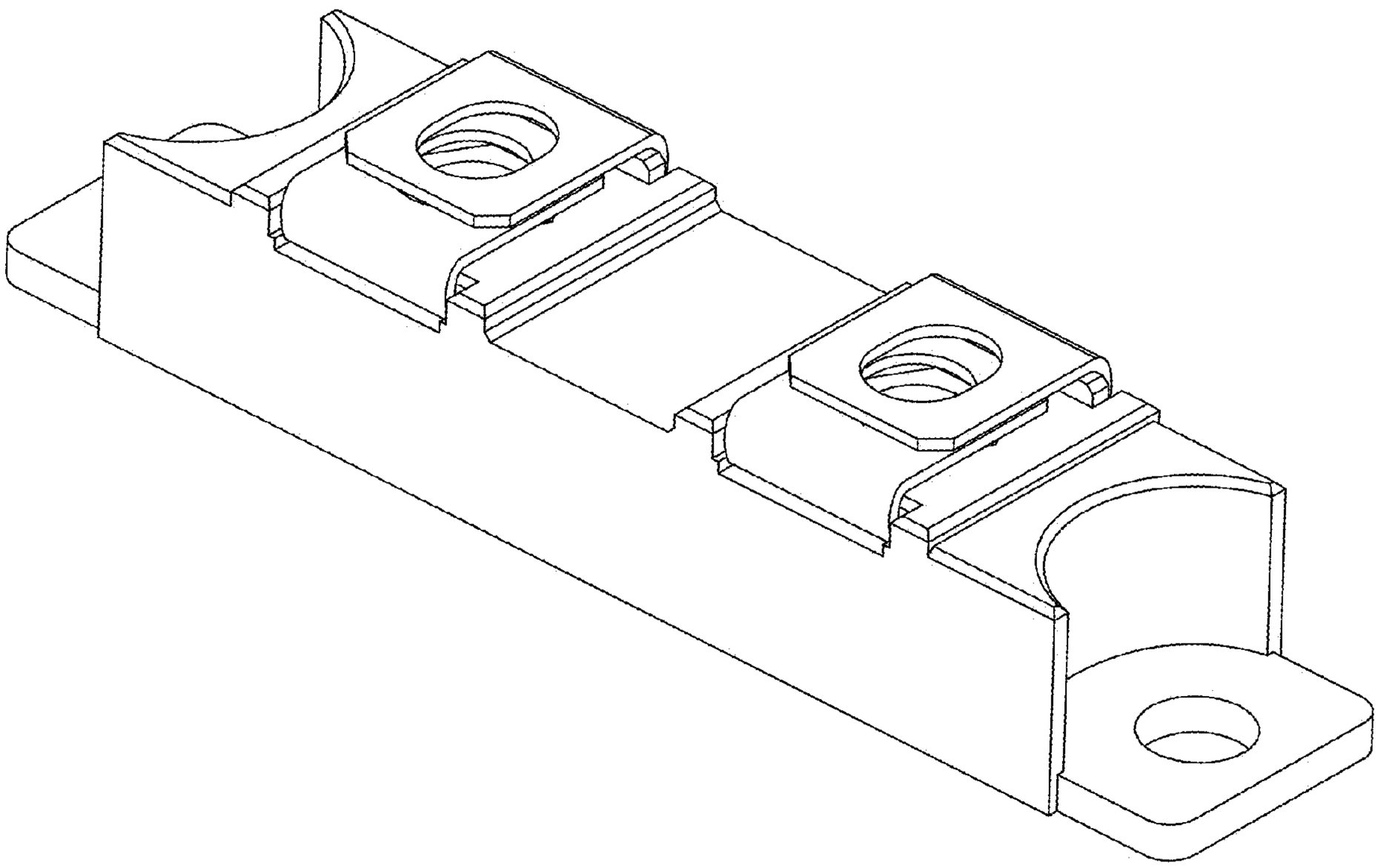

FIG. 8

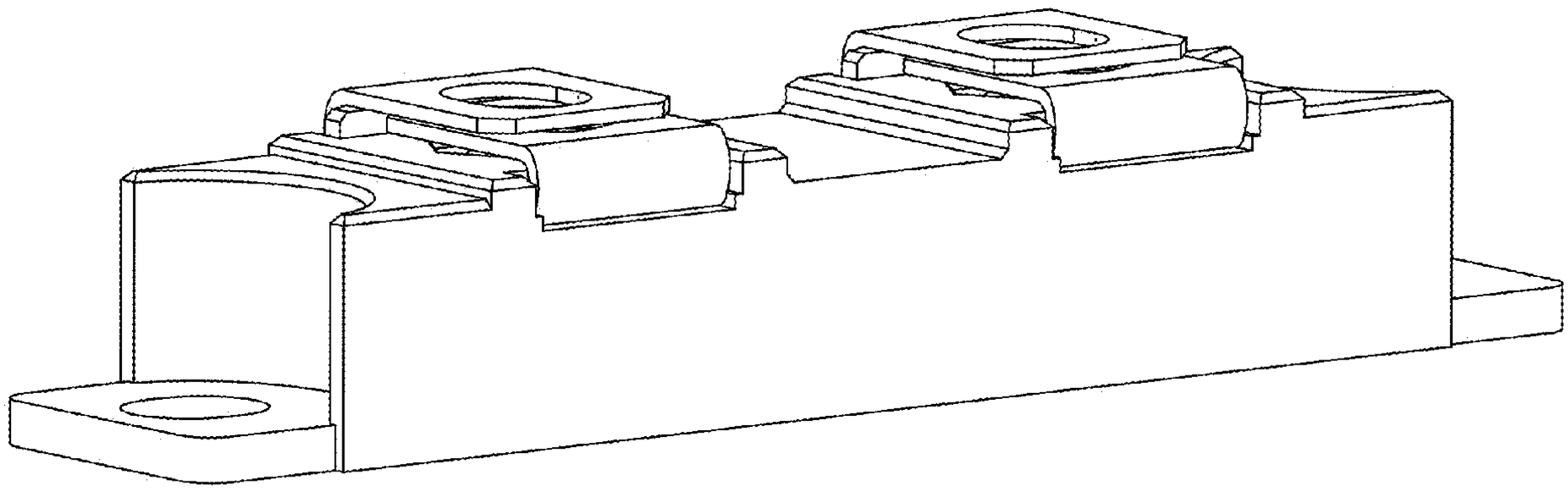

FIG. 9