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(12) **United States Design Patent**  
**Yamaki et al.**

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- (54) **ELASTIC MEMBRANE FOR SEMICONDUCTOR WAFER POLISHING**
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- (73) Assignee: **EBARA CORPORATION**, Tokyo (JP)
- (\*\*) Term: **15 Years**
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- (22) Filed: **Dec. 10, 2018**

**Related U.S. Application Data**

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**Foreign Application Priority Data**

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- (52) **U.S. Cl.**  
USPC ..... **D13/182**
- (58) **Field of Classification Search**  
USPC ..... D13/182; 451/66, 288, 289  
CPC ..... B24B 37/30; B24B 41/061; B24B 49/16  
See application file for complete search history.

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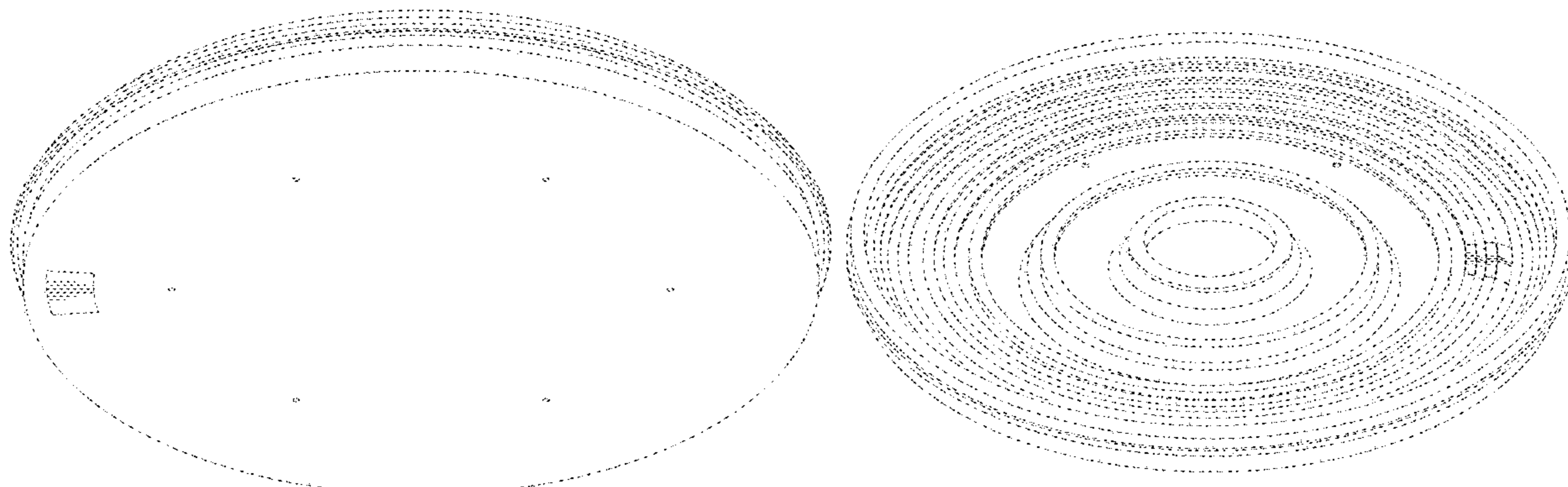
(57) **CLAIM**

The ornamental design for an elastic membrane for semiconductor wafer polishing, as shown and described.

**DESCRIPTION**

FIG. 1 is a bottom perspective view of an elastic membrane for semiconductor wafer polishing showing our new design; FIG. 2 is a top perspective view thereof; FIG. 3 is a bottom view thereof; FIG. 4 is a top view thereof; FIG. 5 is a front view thereof, rear view being identical; FIG. 6 is a right-side view thereof, left-side view being identical; FIG. 7 is a cross-sectional view taken along line 7-7 of FIG. 4; and, FIG. 8 is an enlarged portion view labeled FIG. 8 in FIG. 7. The portions of the elastic membrane shown in even broken lines form no part of the claimed design. The dashed-dot lines in the drawings represent the boundary lines of the claimed design. The box labeled FIG. 8 shown in even broken lines in FIG. 7 defines the enlarged portion view of FIG. 8.

**1 Claim, 6 Drawing Sheets**



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FIG.1

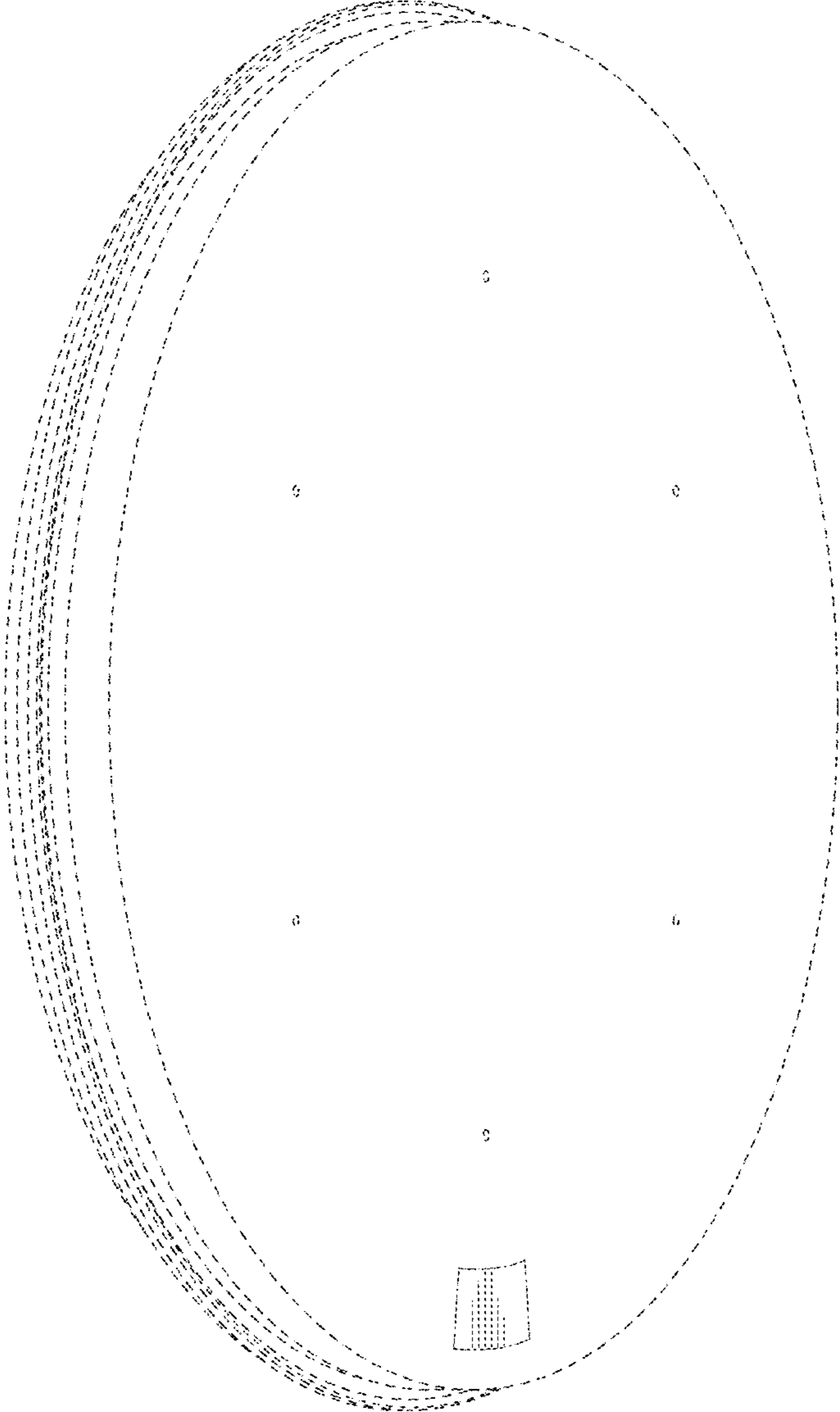


FIG.2

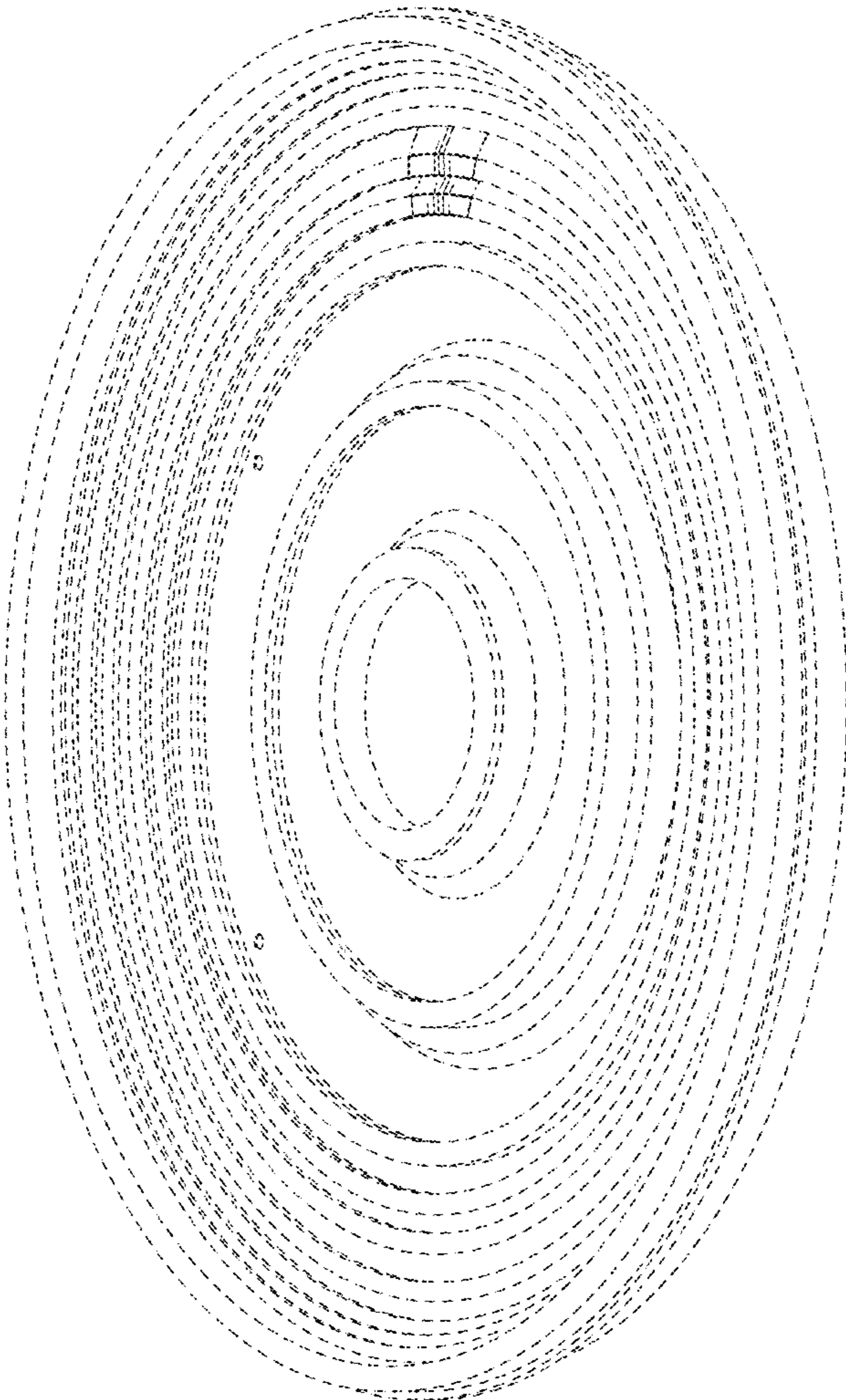


FIG.3

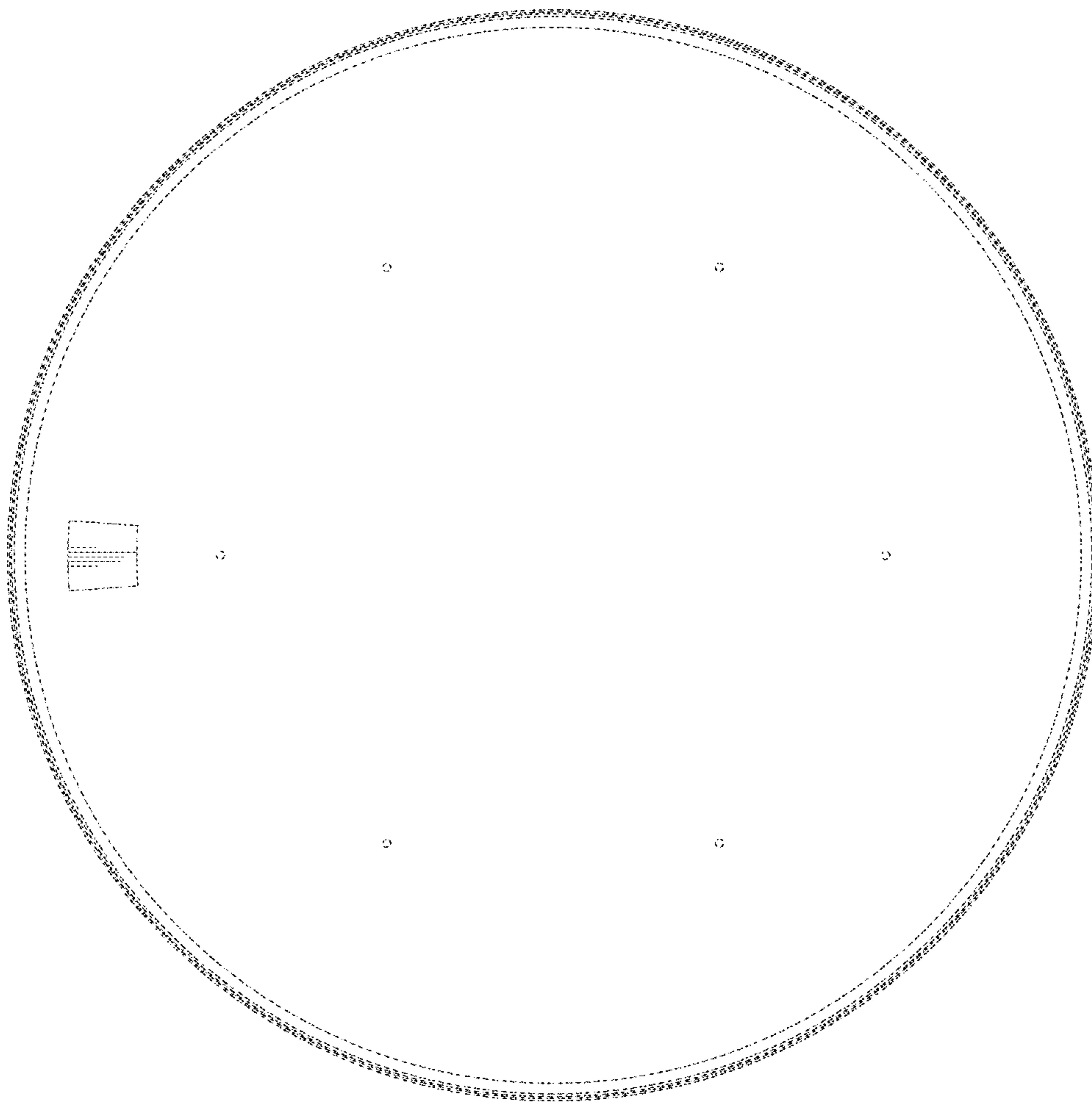
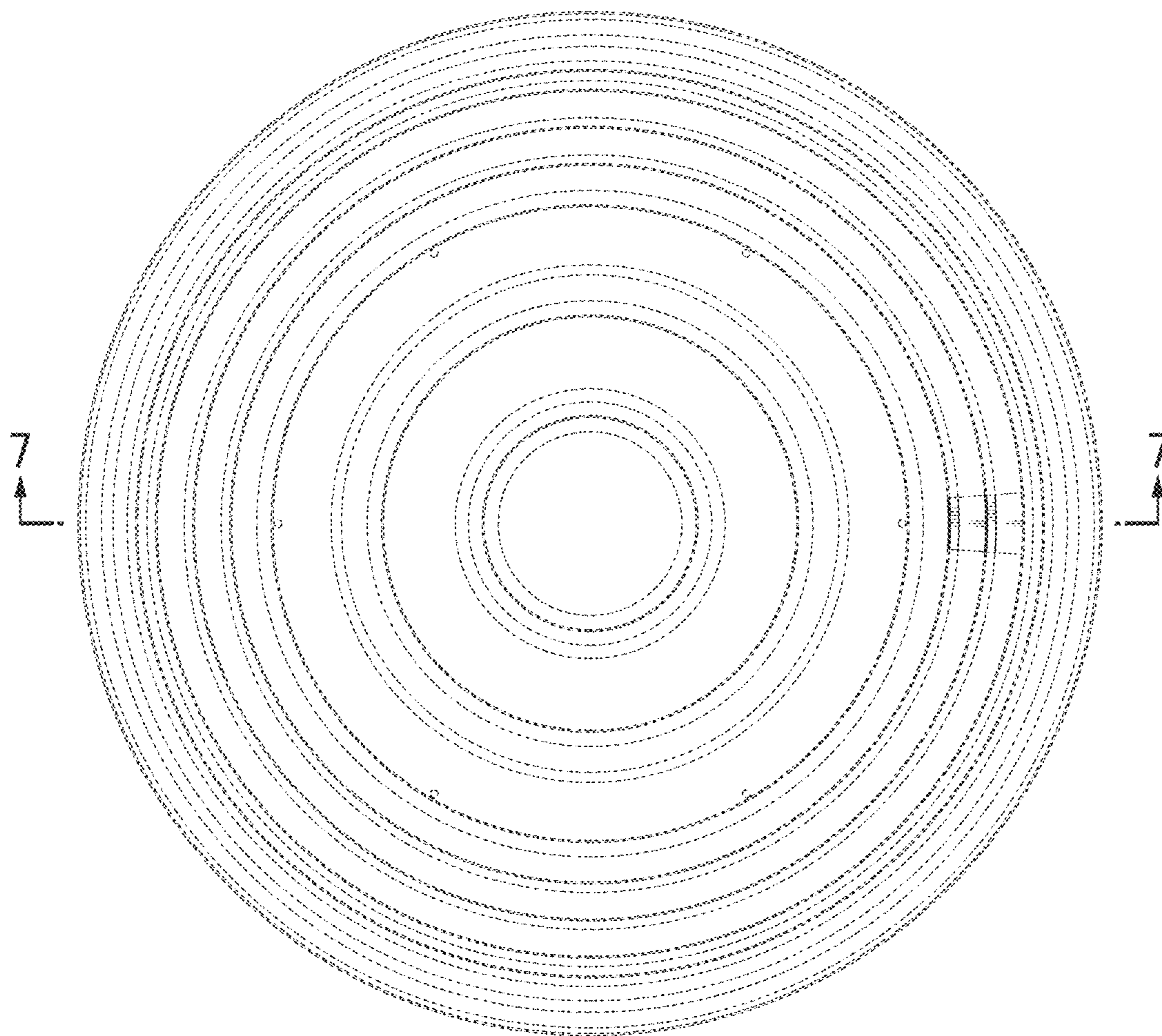
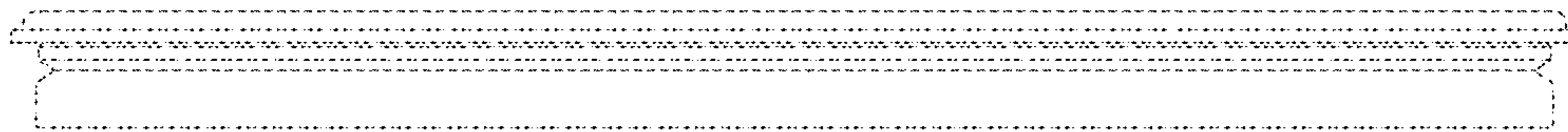


FIG.4



**FIG.5**



**FIG.6**

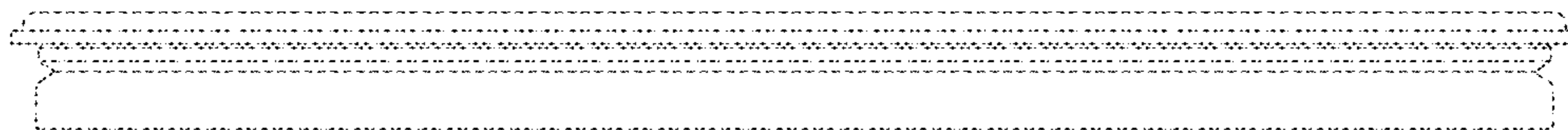


FIG.7

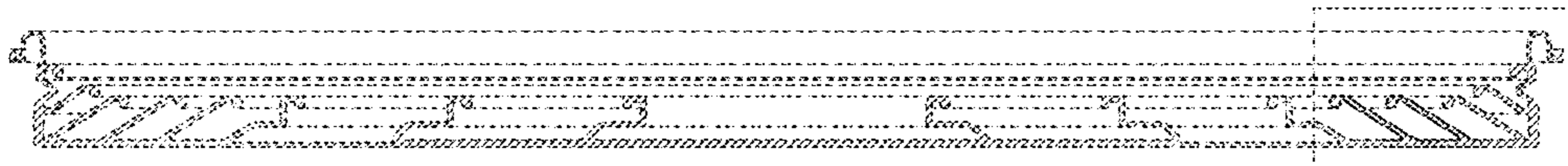


FIG.8

FIG.8

