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Pacier et al.

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(54) **TRANSPORTABLE SEMICONDUCTOR WAFER RACK**

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(**) Term: **15 Years**

(21) Appl. No.: **29/680,874**

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(51) **LOC (13) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182; D15/144, 144.1, 199; 118/715, 500, 728, 729; 211/41.18; 432/253, 258; 156/345.51, 345.52, 156/345.53, 345.55; 414/217, 220.01, 414/935–941
CPC C23C 16/458; C23C 16/4581; C23C 16/4582; C23C 16/4583; C23C 16/4584; C23C 16/4587; C23C 16/4588; C30B 3/14; H01L 21/673; H01L 21/67303; H01L 21/67306; H01L 21/67309; H01L 21/67313; H01L 21/67316; H01L 21/67323; H01L 21/67326; H01L 21/6733
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

D361,752	S	*	8/1995	Yamaga	D13/182
D366,868	S	*	2/1996	Ohsawa	D13/182
D378,675	S	*	4/1997	Iwai	D13/182
D378,823	S	*	4/1997	Watanabe	D13/182
D380,454	S	*	7/1997	Iwai	D13/182
5,752,609	A	*	5/1998	Kato	H01L 21/67309 211/41.18
D404,015	S	*	1/1999	Honma	D13/182
D404,371	S	*	1/1999	Shimazu	D13/182
D409,158	S	*	5/1999	Shimazu	206/832
D411,176	S	*	6/1999	Shimazu	D13/182

(Continued)

FOREIGN PATENT DOCUMENTS

CN	110246791 A	9/2019

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(74) *Attorney, Agent, or Firm* — Downs Rachlin Martin PLLC

(57) **CLAIM**

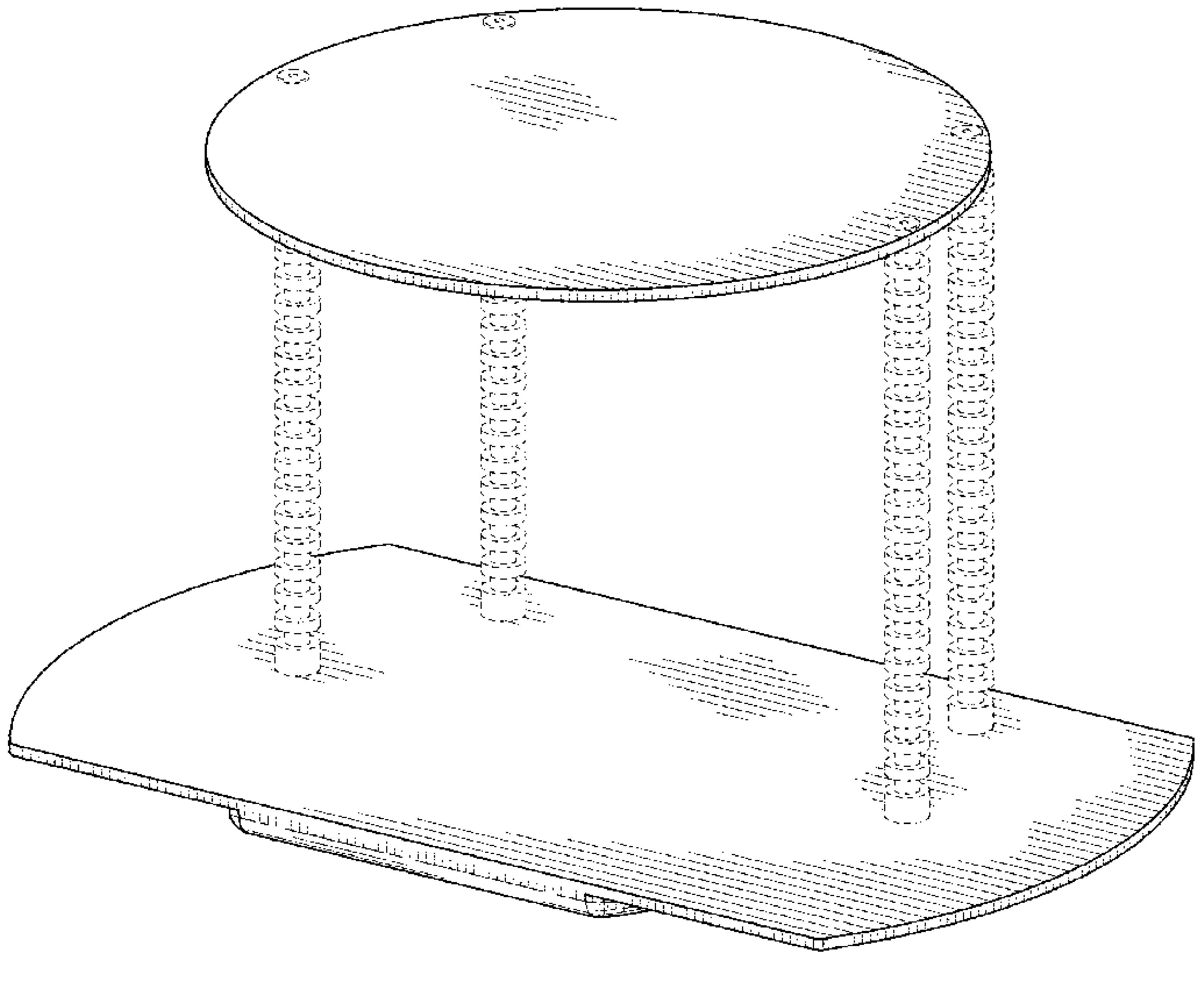
The ornamental design for a transportable semiconductor wafer rack, as shown and described.

DESCRIPTION

FIG. **1** is a perspective view of a transportable semiconductor wafer rack showing our new design;
FIG. **2** is a front view thereof;
FIG. **3** is a rear view thereof;
FIG. **4** is a first side view thereof;
FIG. **5** is a second side view thereof;
FIG. **6** is a top view thereof;
FIG. **7** is a bottom view thereof;
FIG. **8** is a cross-section view taken along line **8**-**8** of FIG. **7**; and,
FIG. **9** is another cross-section view taken along line **9**-**9** of FIG. **7**.

The broken lines in the Figures are for the purpose of illustrating unclaimed portions of the transportable semiconductor wafer rack and form no part of the claimed design. The shade lines in the Figures show contour and not surface ornamentation.

1 Claim, 9 Drawing Sheets



(56) References Cited

U.S. PATENT DOCUMENTS

6,062,853	A	*	5/2000	Shimazu	H01L 21/6875 432/258
6,065,615	A	*	5/2000	Uchiyama	H01L 21/67306 211/41.18
6,099,302	A	*	8/2000	Hong	C30B 31/14 211/41.18
6,099,645	A	*	8/2000	Easley	H01L 21/67309 118/500
6,287,112	B1	*	9/2001	Van Voorst Vader	C30B 31/14 118/728
6,341,935	B1	*	1/2002	Tseng	H01L 21/67303 118/500
D570,308	S	*	6/2008	Sato	D13/182
D570,309	S	*	6/2008	Sato	D13/182
D580,894	S	*	11/2008	Sato	D13/182
7,484,958	B2	*	2/2009	Kobayashi	H01L 21/67309 211/41.18
D600,221	S	*	9/2009	Sato	D13/182
D600,222	S	*	9/2009	Sato	D13/182
D616,396	S	*	5/2010	Sato	D13/182
7,857,140	B2	*	12/2010	Shinjo	H01L 21/6732 206/445
D655,255	S	*	3/2012	Takebayashi	D13/182
D655,682	S	*	3/2012	Takebayashi	D13/182
D734,730	S	*	7/2015	Yoshida	D13/182
D737,785	S	*	9/2015	Yoshida	D13/182
D738,329	S	*	9/2015	Yoshida	D13/182
D747,279	S	*	1/2016	Yoshida	D13/182
D839,219	S	*	1/2019	Yoshida	D13/182
10,224,185	B2		3/2019	Noh et al.	
D846,514	S	*	4/2019	Yoshida	D13/182
2002/0092815	A1	*	7/2002	Kim	H01L 21/67303 211/41.18
2002/0113027	A1	*	8/2002	Minami	H01L 21/67309 211/41.18
2002/0130061	A1	*	9/2002	Hengst	C23C 16/325 206/710
2002/0187023	A1	*	12/2002	Araki	H01L 21/67309 414/160
2003/0024888	A1	*	2/2003	Payne	H01L 21/67303 211/41.18
2005/0145584	A1	*	7/2005	Buckley	H01L 21/67306 211/41.18
2018/0019144	A1		1/2018	Ogitsu	
2019/0279891	A1		9/2019	Domsa et al.	

* cited by examiner

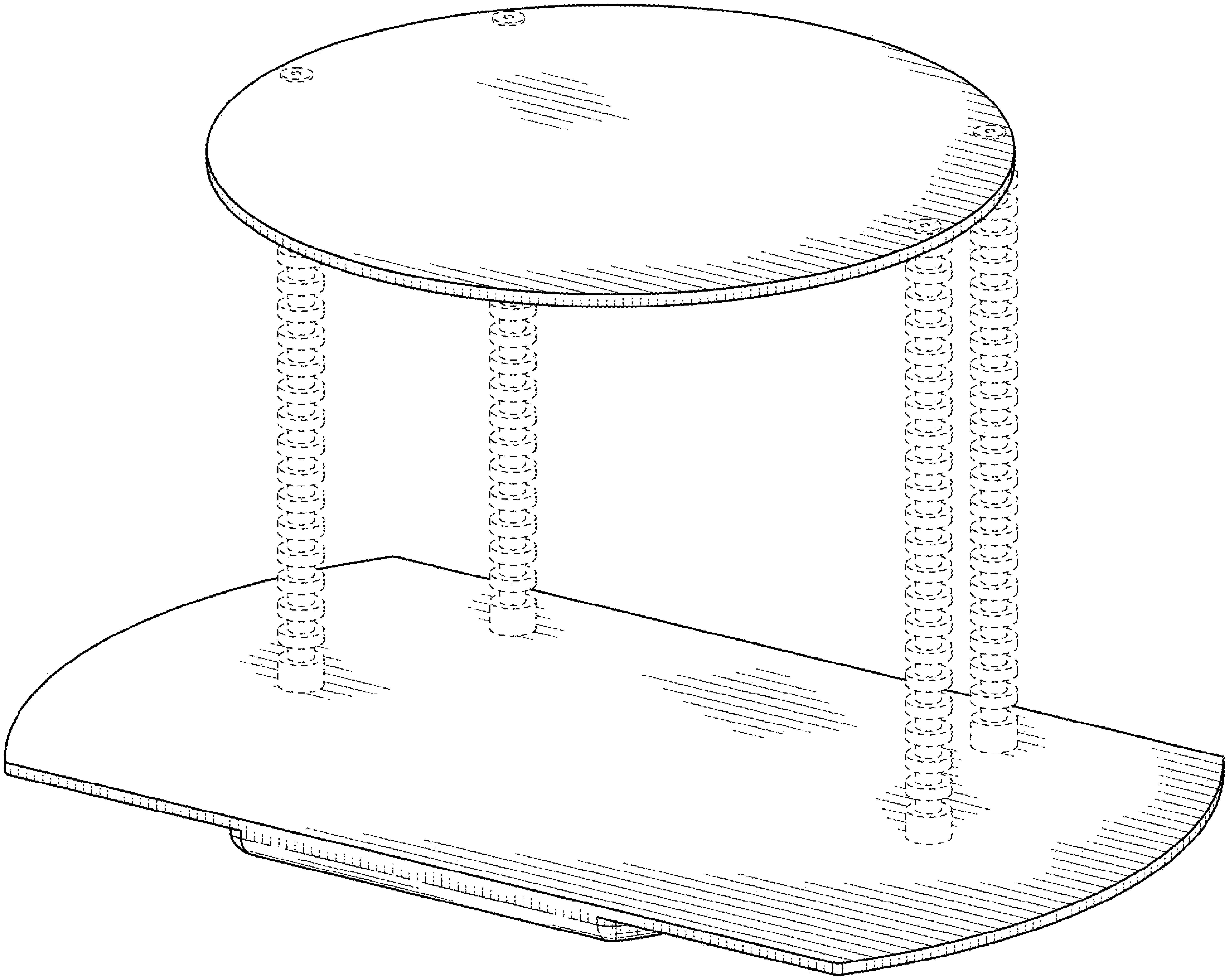


FIG. 1

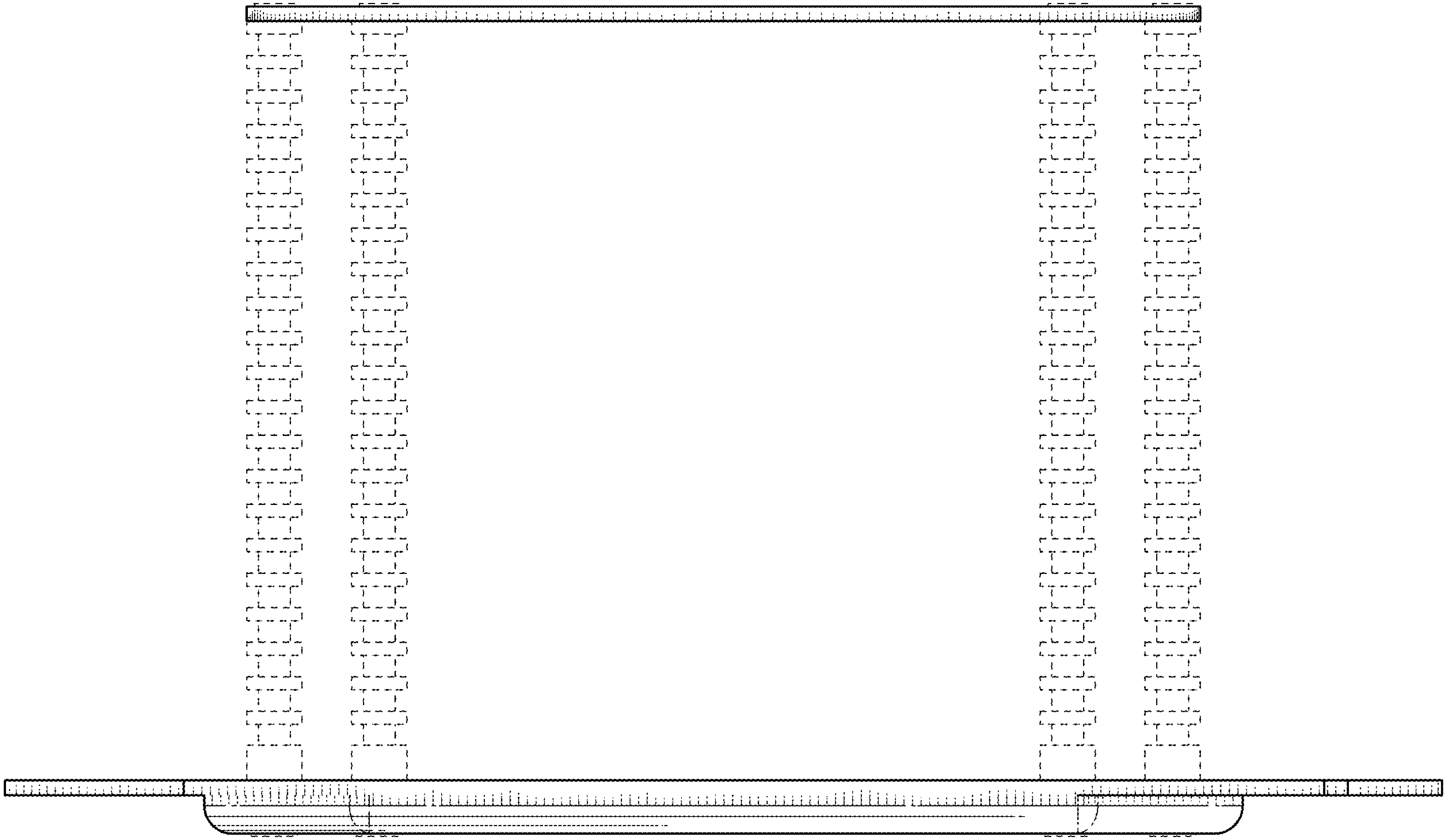


FIG. 2

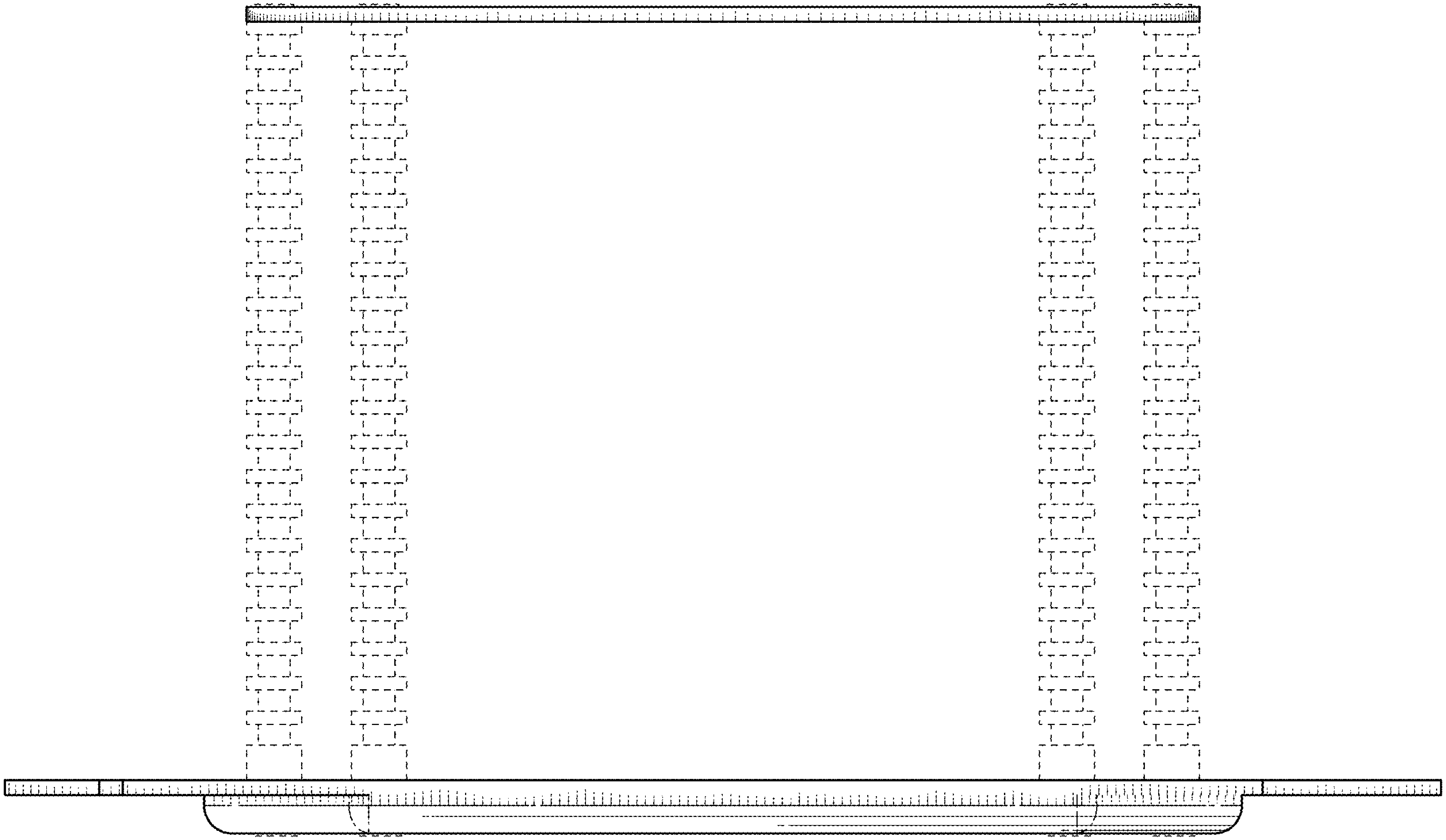


FIG. 3

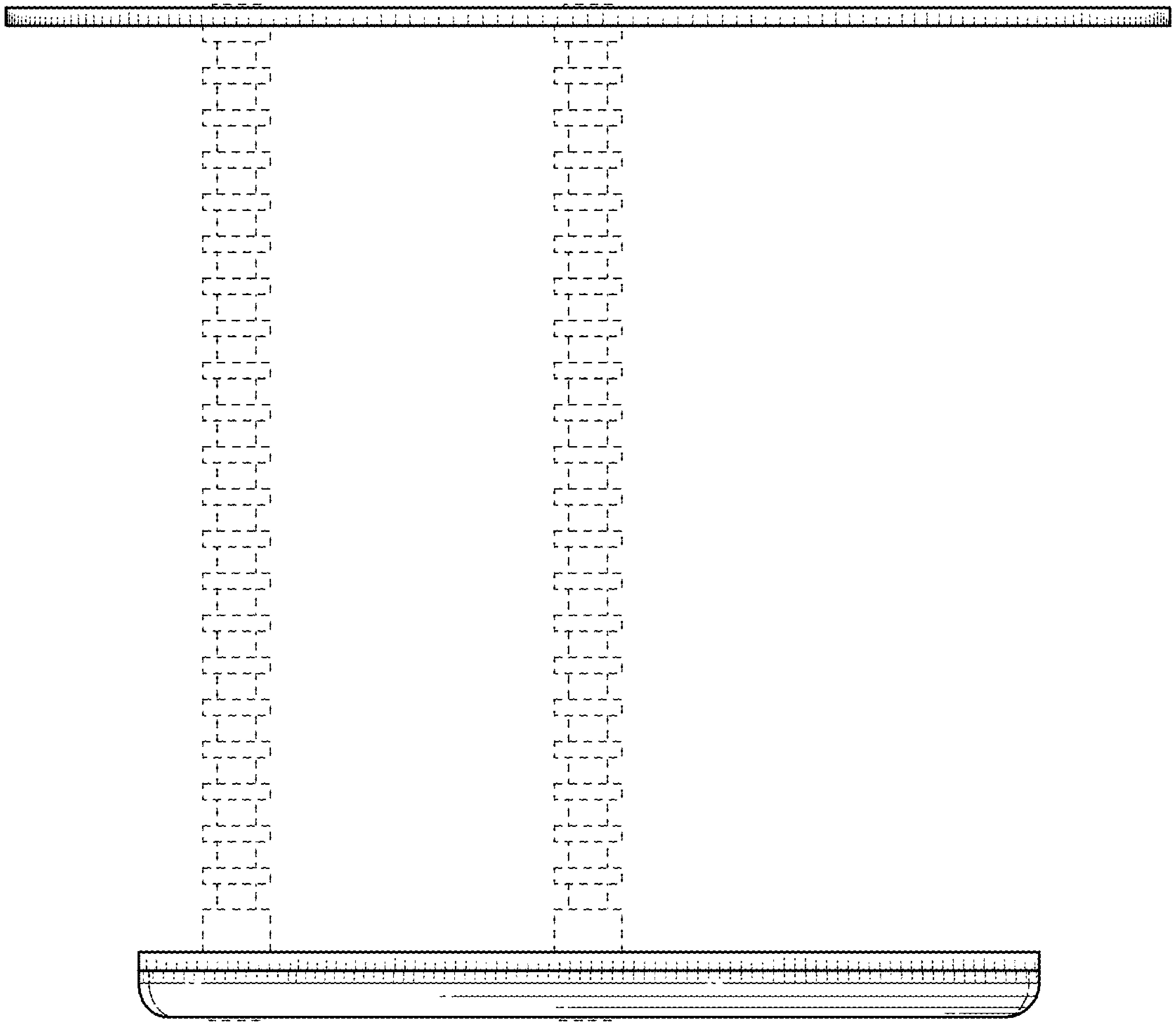


FIG. 4

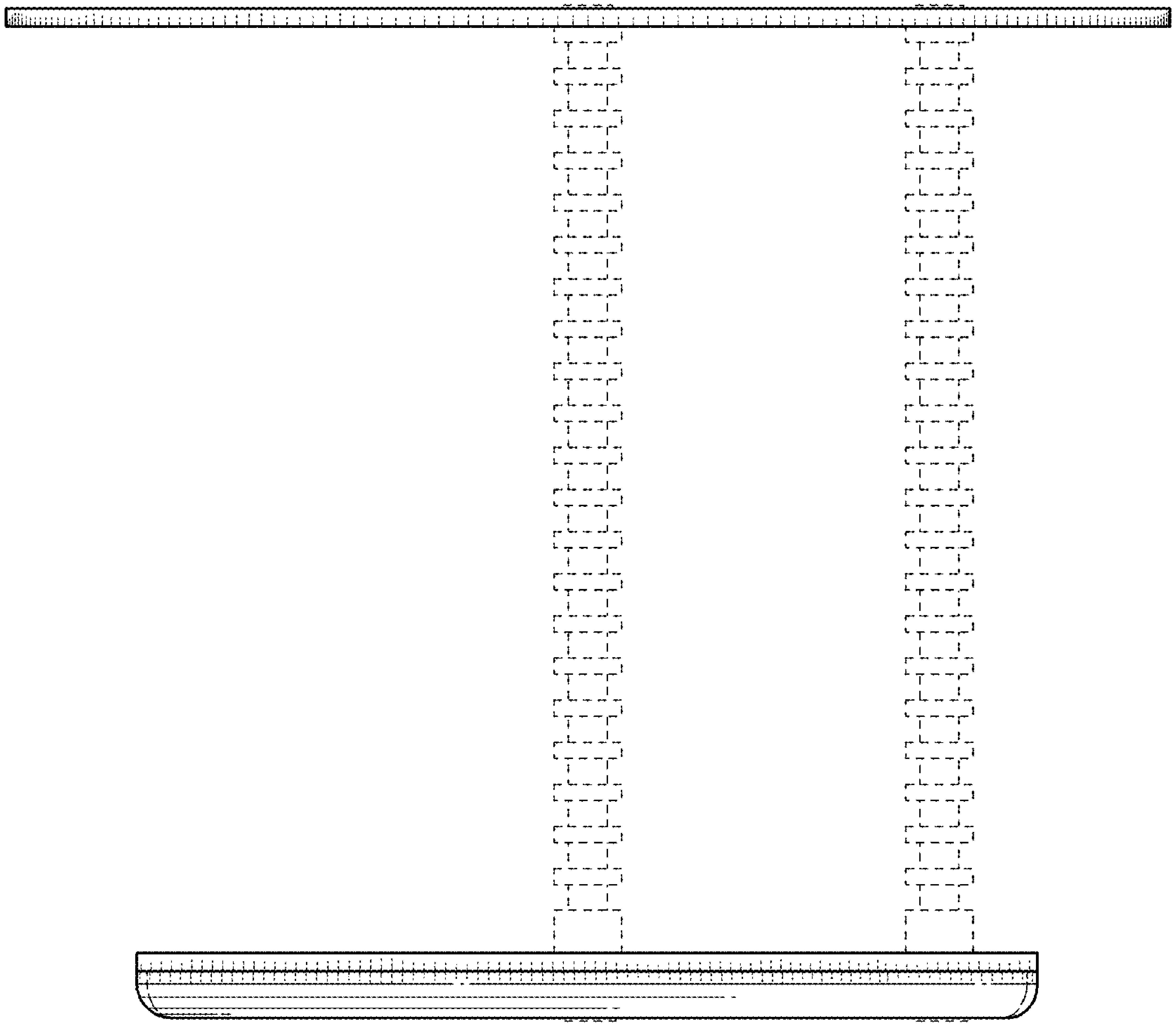


FIG. 5

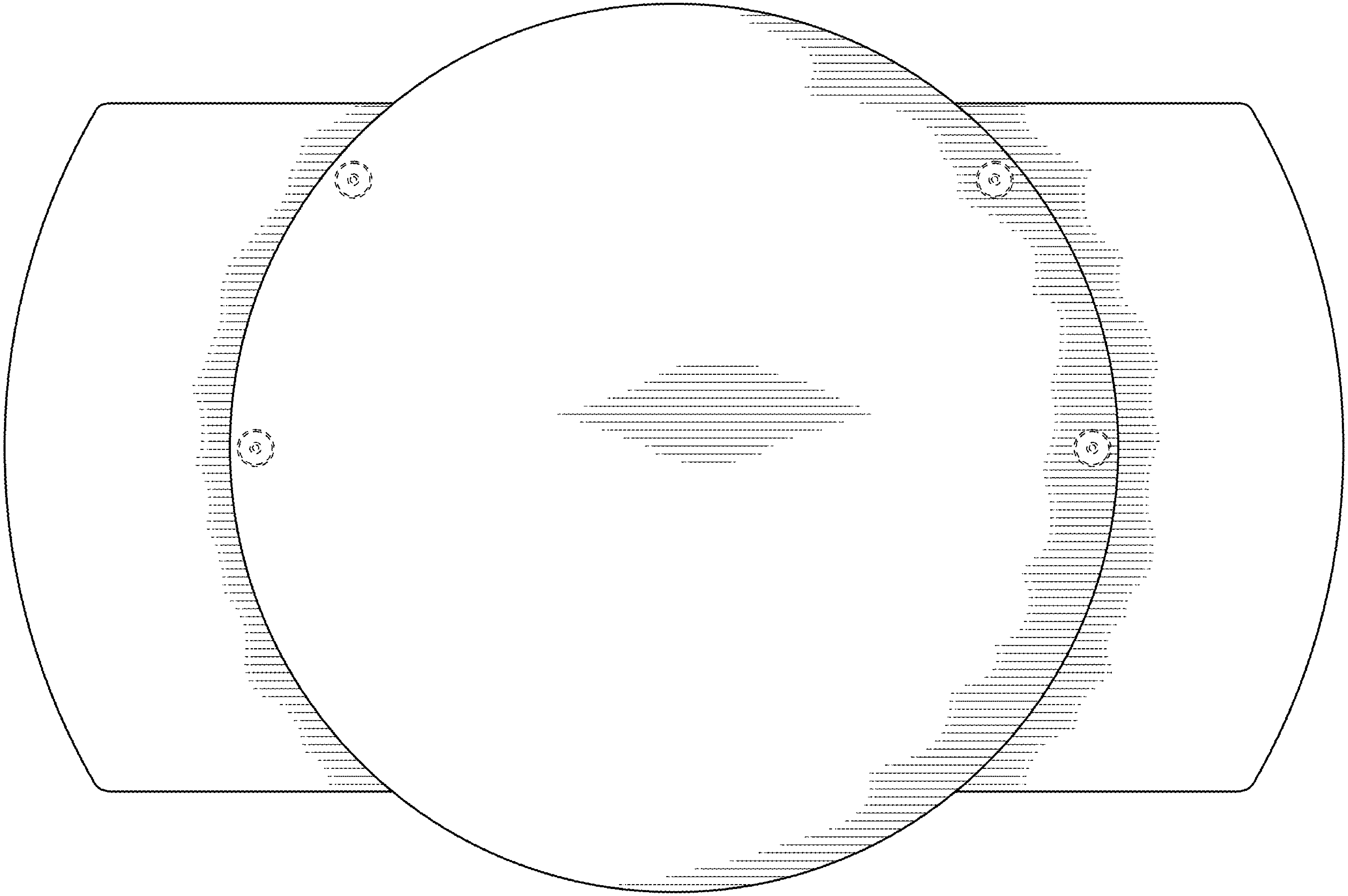


FIG. 6

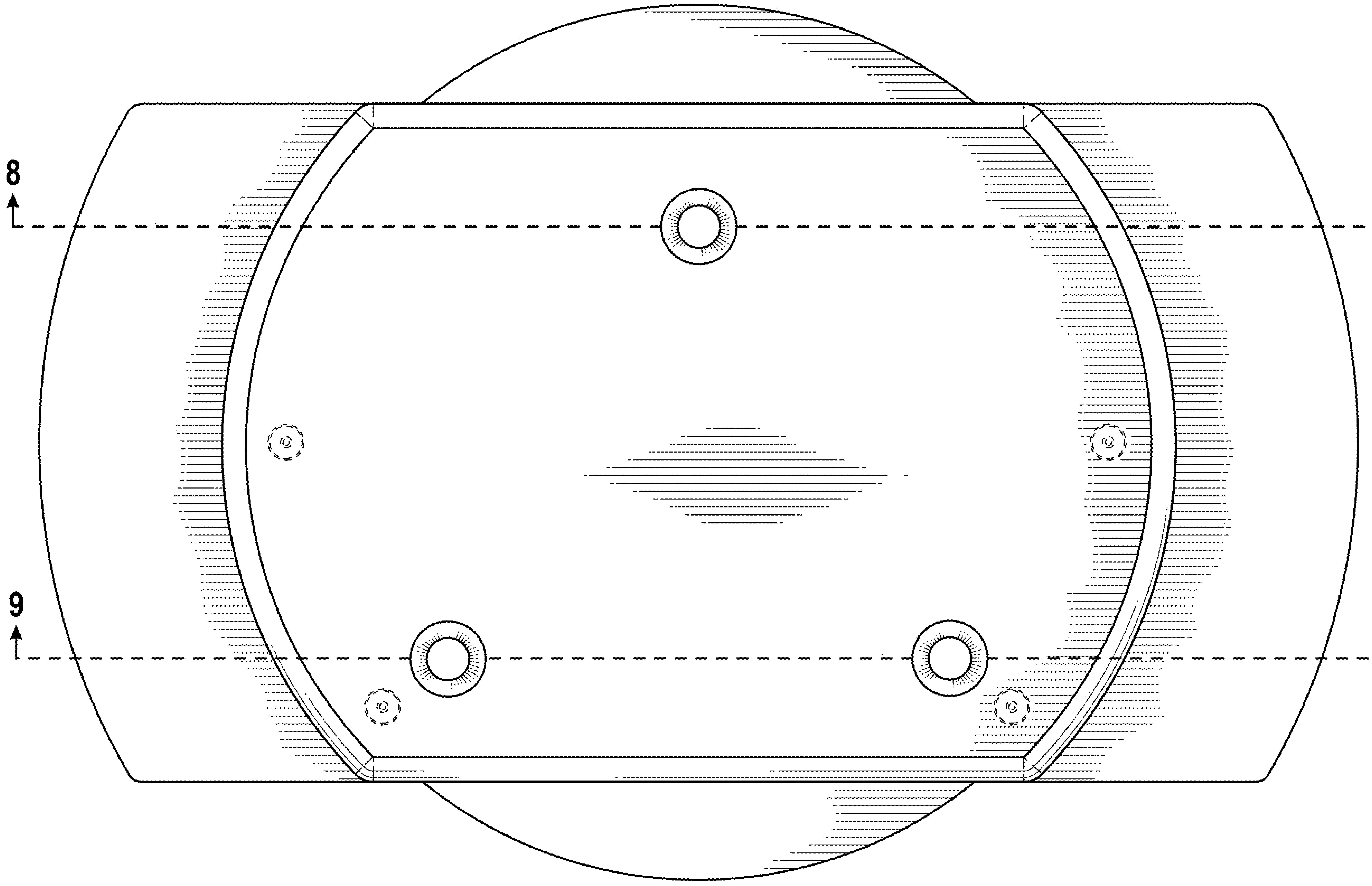


FIG. 7

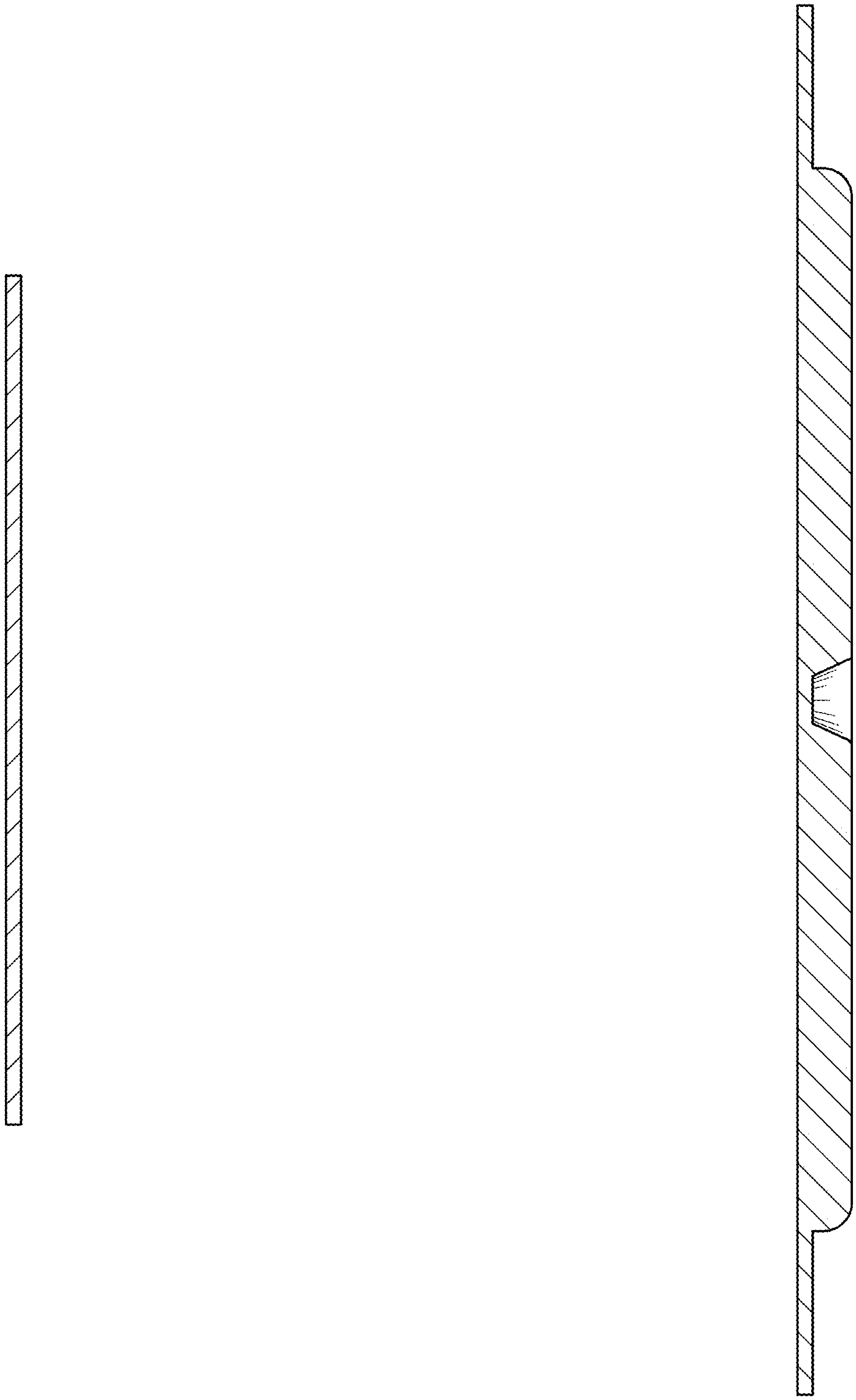


FIG. 8

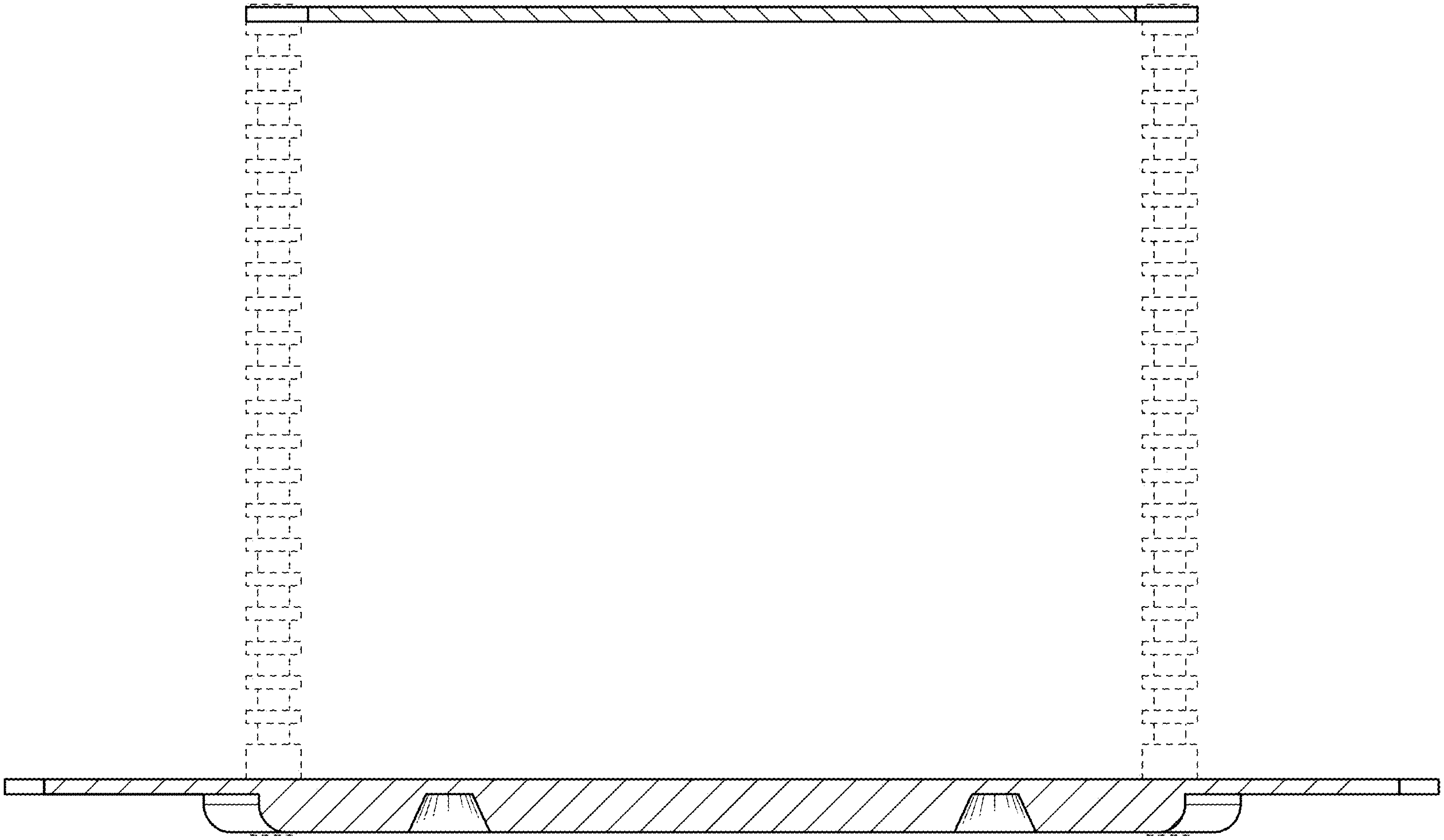


FIG. 9