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(12) **United States Design Patent** (10) **Patent No.:** **US D908,102 S**  
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(54) **TRANSPORTABLE SEMICONDUCTOR  
WAFER RACK**

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(US)

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(\*\*) Term: **15 Years**

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(52) **U.S. Cl.**  
USPC ..... **D13/182**

(58) **Field of Classification Search**  
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118/715, 500, 728, 729; 211/41.18;  
432/253, 258; 156/345.51, 345.52,  
156/345.53, 345.55; 414/217, 220.01,  
414/935-941  
CPC ..... C23C 16/458; C23C 16/4581; C23C  
16/4582; C23C 16/4583; C23C 16/4584;  
C23C 16/4587; C23C 16/4588; C30B  
3/14; H01L 21/673; H01L 21/67303;  
H01L 21/67306; H01L 21/67309; H01L  
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See application file for complete search history.

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(57) **CLAIM**

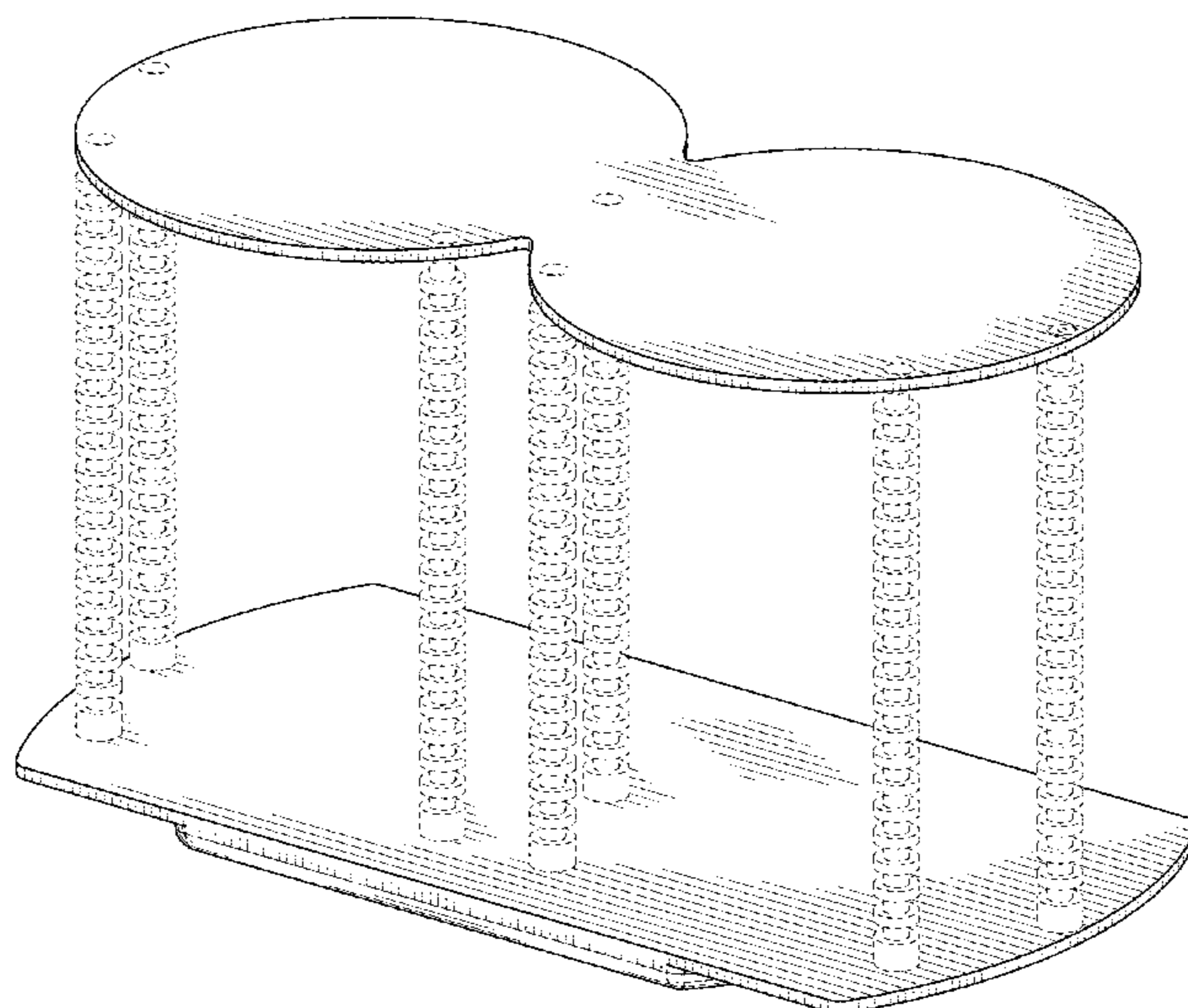
The ornamental design for a transportable semiconductor wafer rack, as shown and described.

**DESCRIPTION**

FIG. 1 is a perspective view of a transportable semiconductor wafer rack showing our new design;  
FIG. 2 is a front view thereof;  
FIG. 3 is a rear view thereof;  
FIG. 4 is a first side view thereof;  
FIG. 5 is a second side view thereof;  
FIG. 6 is a top view thereof;  
FIG. 7 is a bottom view thereof;  
FIG. 8 is a cross-section view taken along line 8-8 of FIG. 7; and,  
FIG. 9 is another cross-section view taken along line 9-9 of FIG. 7.

The broken lines in the Figures are for the purpose of illustrating unclaimed portions of the transportable semiconductor wafer rack and form no part of the claimed design. The shade lines in the Figures show contour and not surface ornamentation.

**1 Claim, 9 Drawing Sheets**



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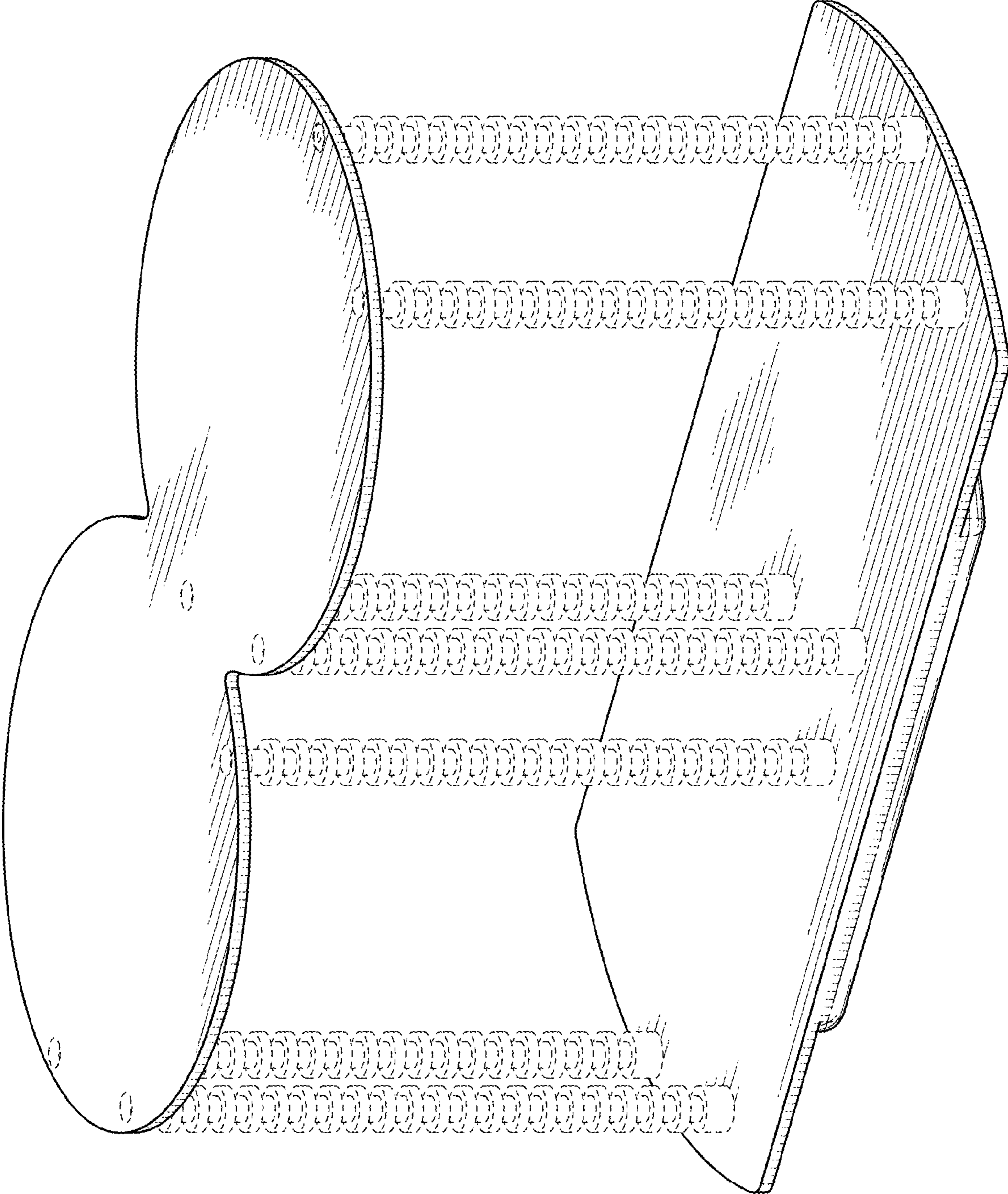


FIG. 1

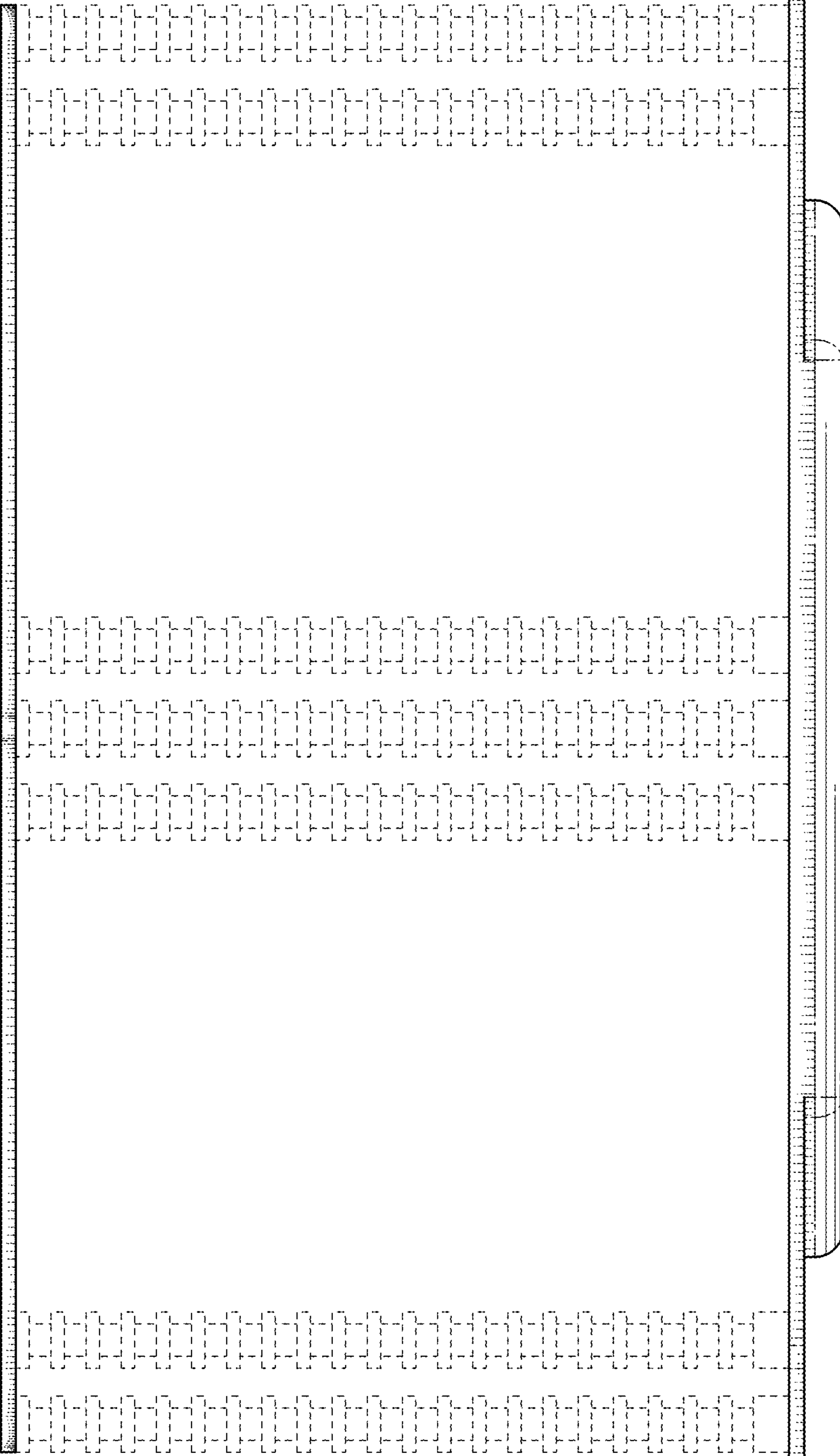


FIG. 2

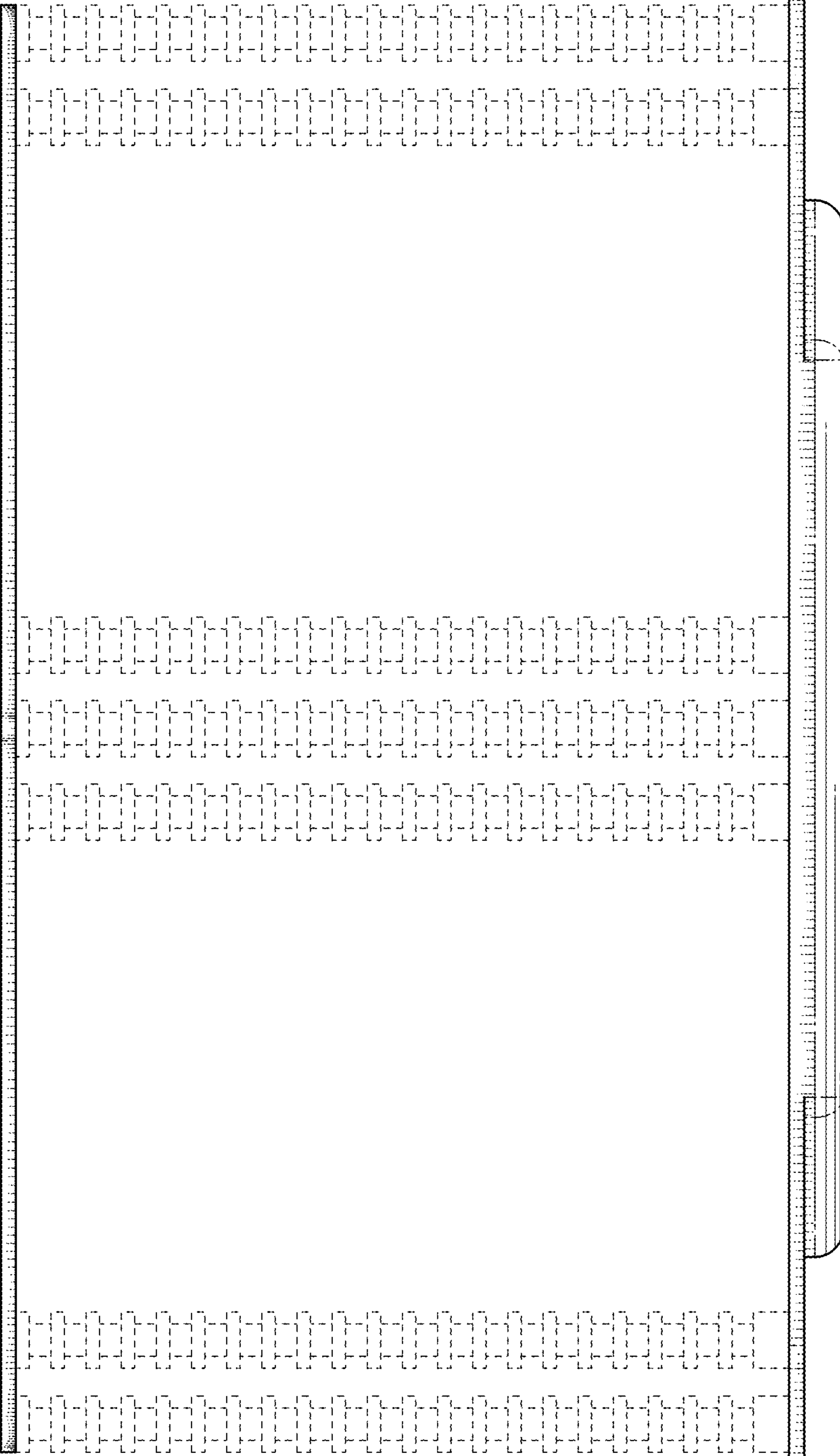


FIG. 3

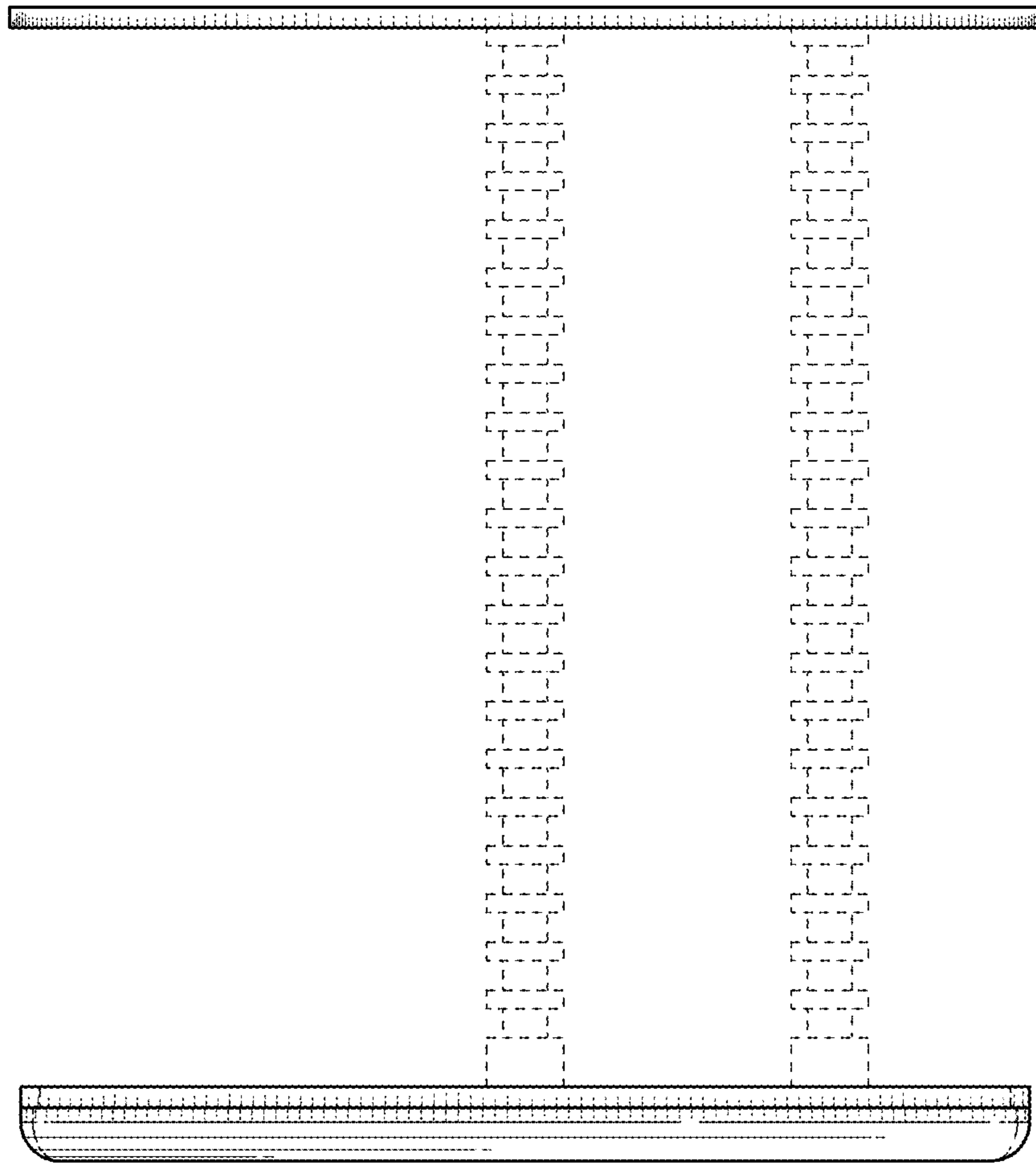


FIG. 4

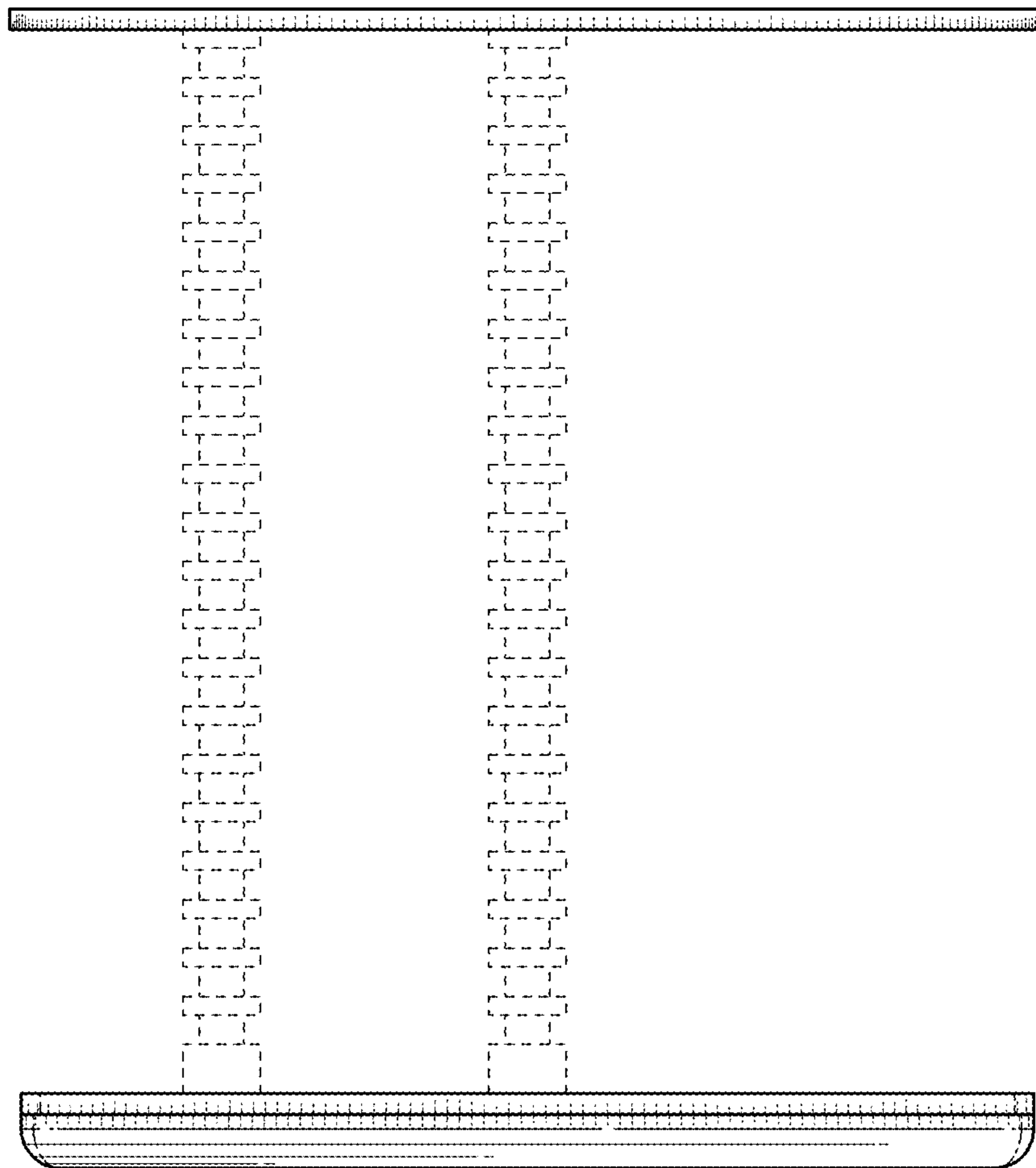


FIG. 5

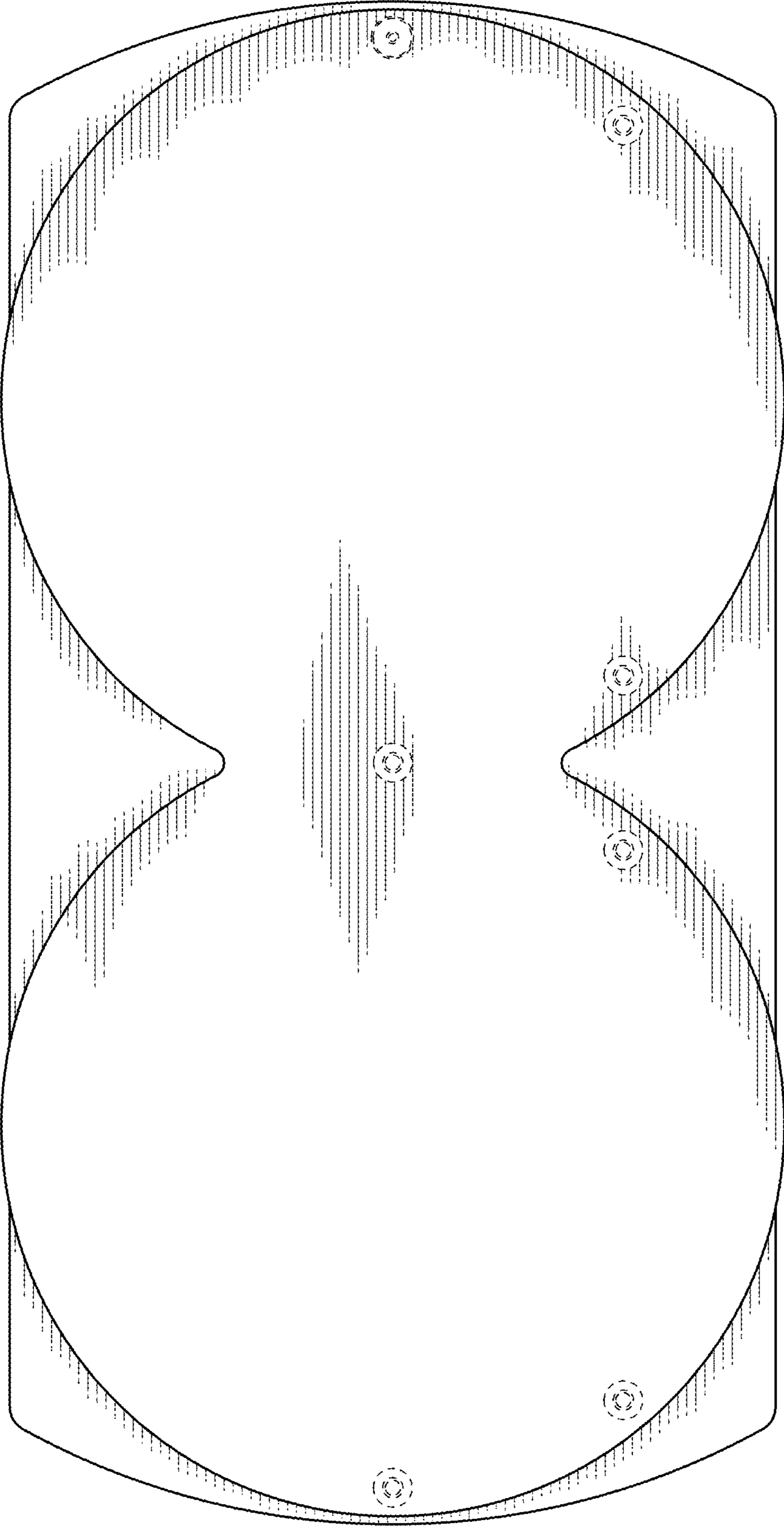


FIG. 6



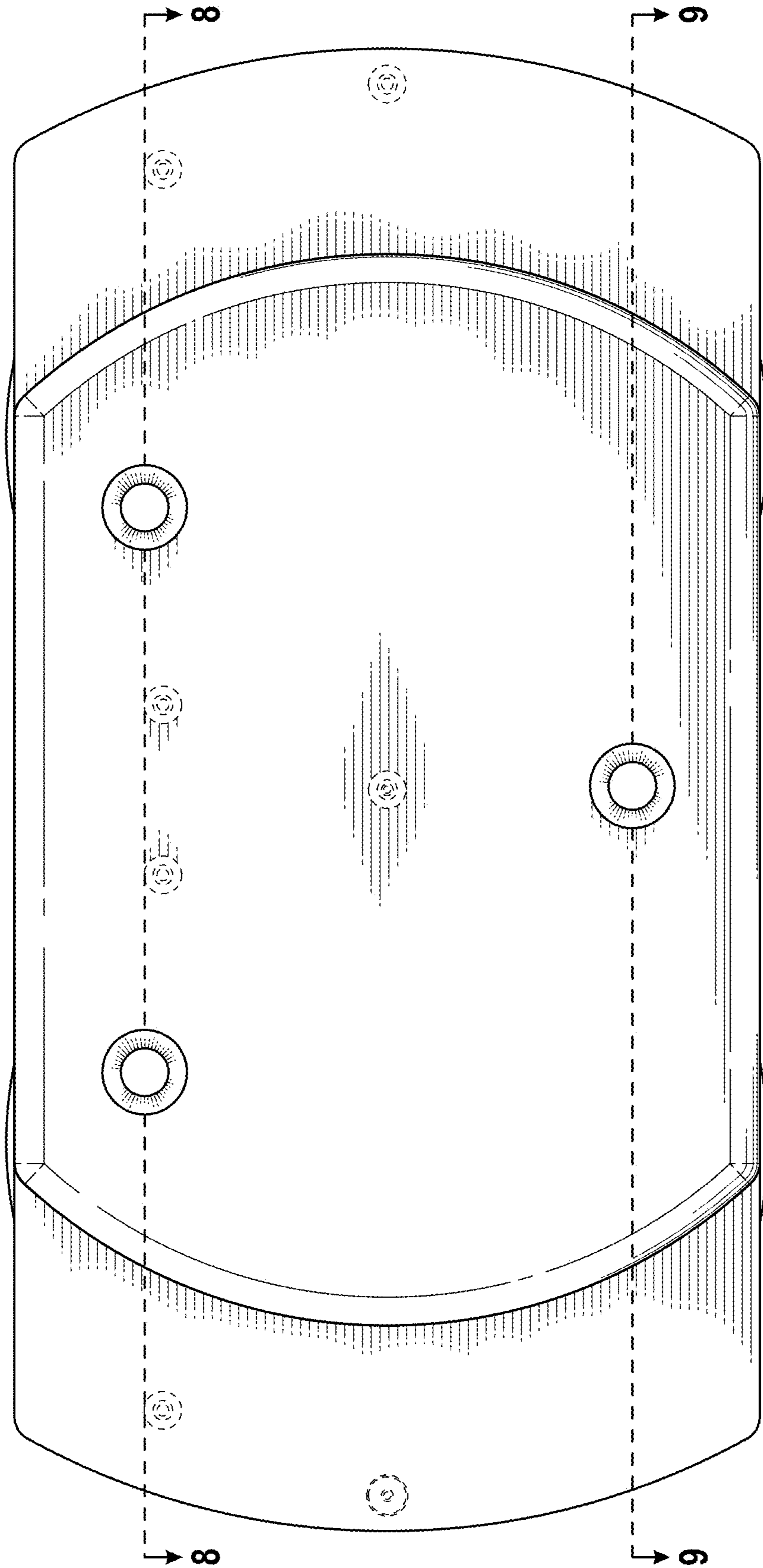


FIG. 7

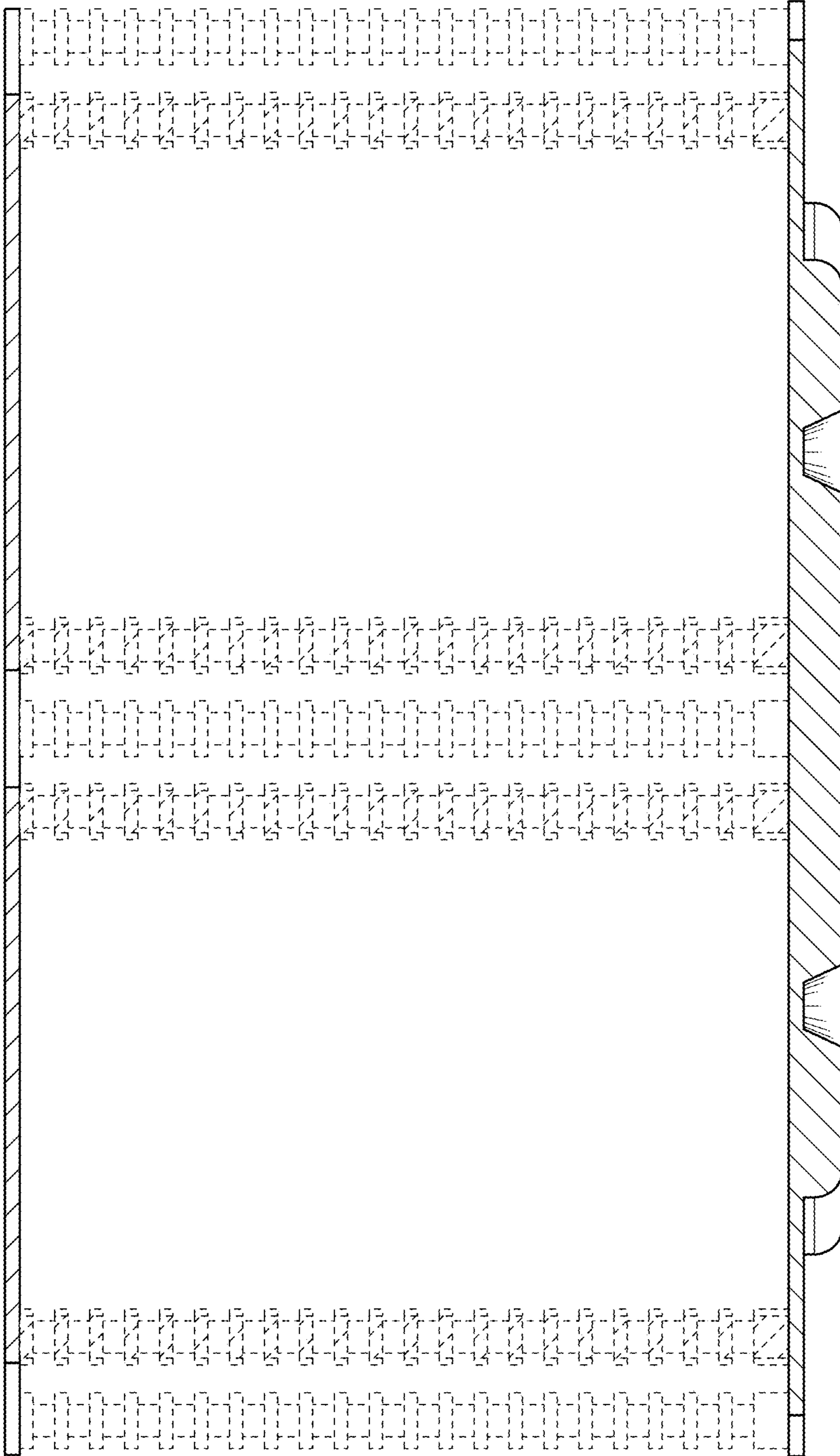


FIG. 8

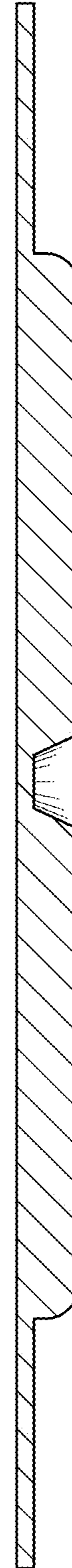


FIG. 9