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Murata et al.

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(54) **GAS INLET ATTACHMENT FOR WAFER PROCESSING APPARATUS**

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(**) Term: **15 Years**

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(30) **Foreign Application Priority Data**

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(51) **LOC (12) Cl.** **15-09**

(52) **U.S. Cl.**
USPC **D15/144.1**

(58) **Field of Classification Search**
USPC D13/182, 184, 199, 122; D15/144, D15/144.1, 144.2; D8/2, 382
CPC . C23C 16/00; C23C 16/455; C23C 16/45502; C23C 16/45504; C23C 16/45506; C23C 16/45508; C23C 16/4551; C23C 16/45512; C23C 16/45514; C23C 16/45517; C23C 16/45563; C23C 16/4557; C23C 16/45576; C23C 16/45578; C23C 16/402; C23C 16/4584; C23C 16/45587; C23C 16/45525; C23C 16/45544; C23C 16/46; C23C 16/45527; C23C 16/4412; H01L 21/00; H01L 21/02; H01L 21/02263; H01L 21/31; H01L 21/205; H01L 21/0228; H01L 21/02164
See application file for complete search history.

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(57) **CLAIM**

The ornamental design for a gas inlet attachment for wafer processing apparatus, as shown and described.

DESCRIPTION

FIG. **1** is a front, top and right side perspective view of a gas inlet attachment for wafer processing apparatus showing our new design;
FIG. **2** is a front elevational view thereof;
FIG. **3** is a rear elevational view thereof;
FIG. **4** is a right side elevational view thereof;
FIG. **5** is a left side elevational view thereof;
FIG. **6** is a top plan view thereof;
FIG. **7** is a bottom plan view thereof; and,

(Continued)

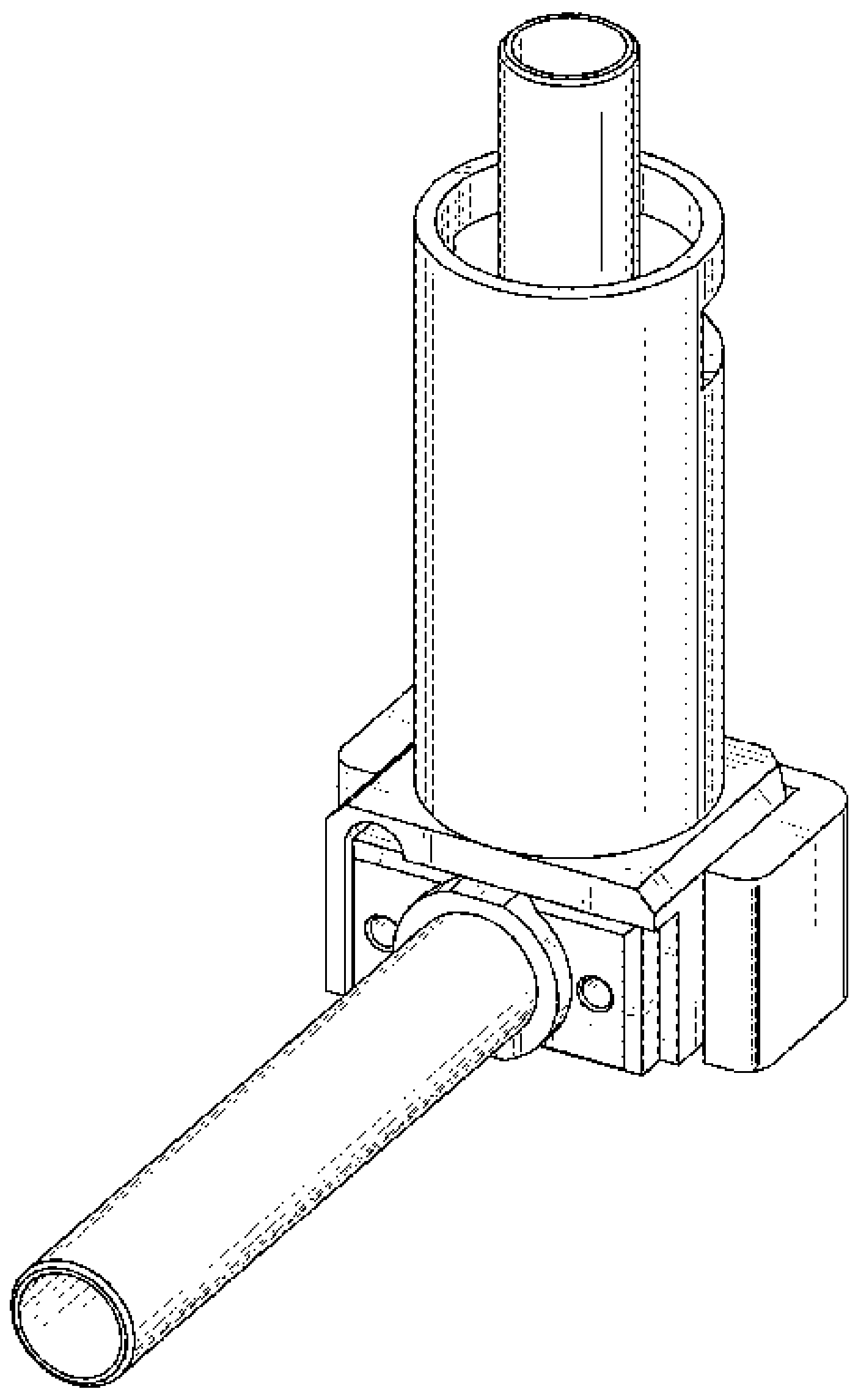

FIG. **8** is a cross sectional view taken along line **8-8** in FIG. **2**.

1 Claim, 6 Drawing Sheets

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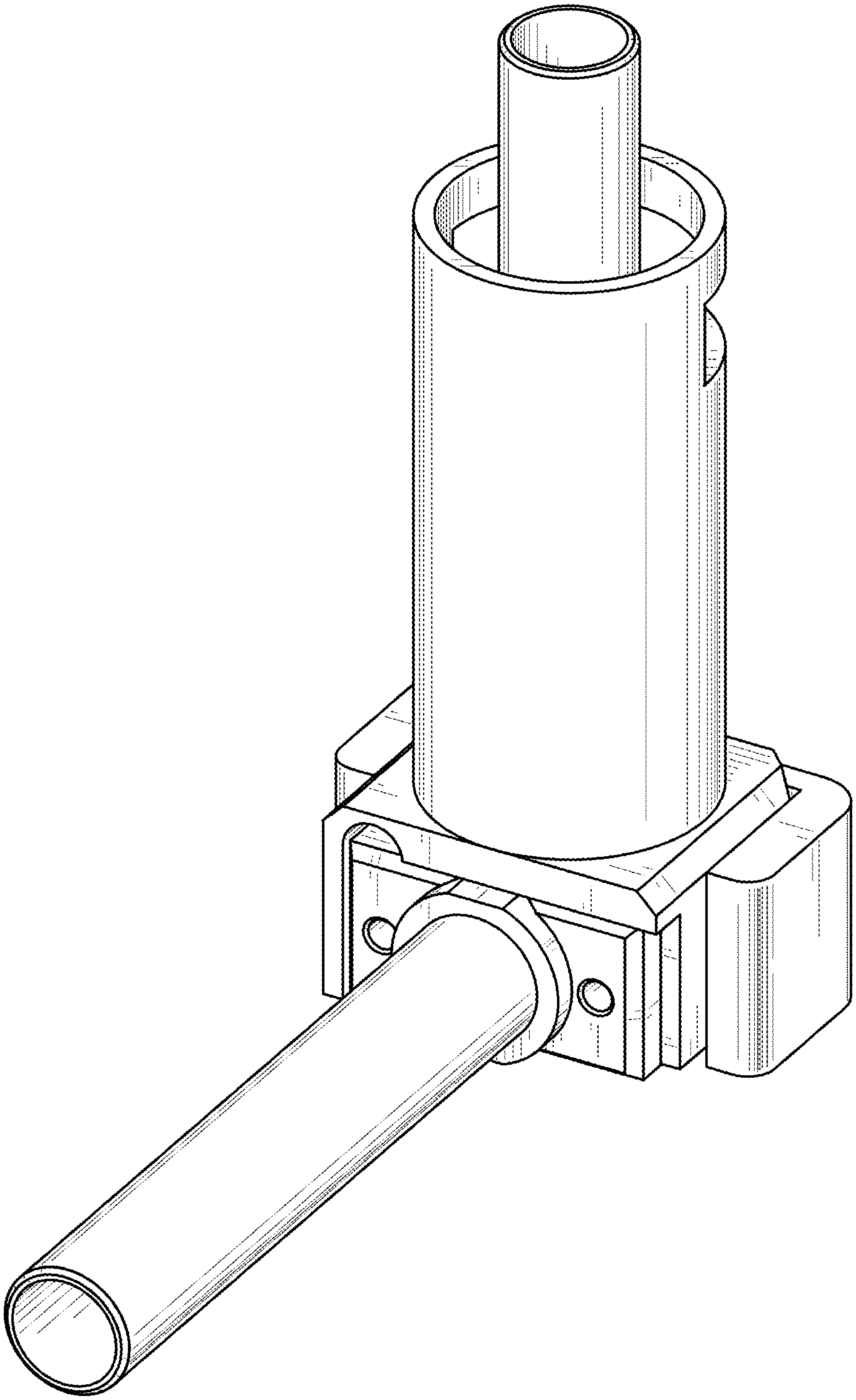

FIG. 1

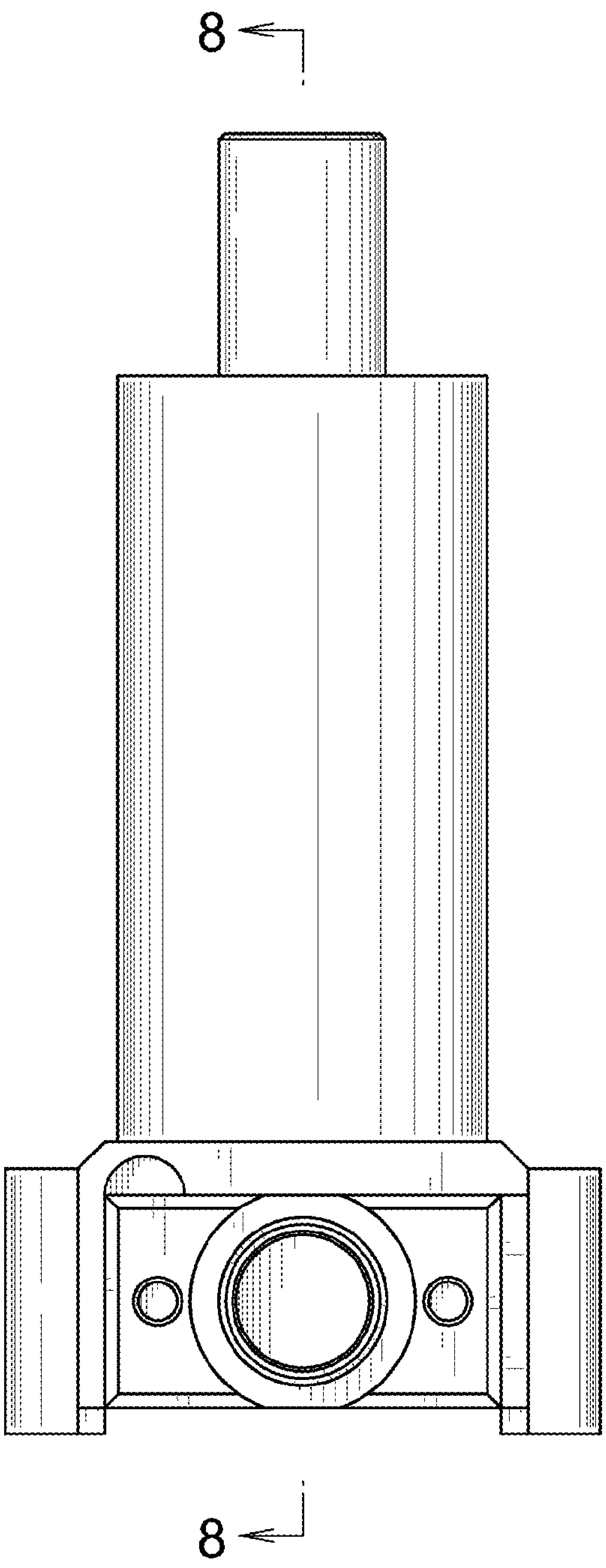

FIG. 2

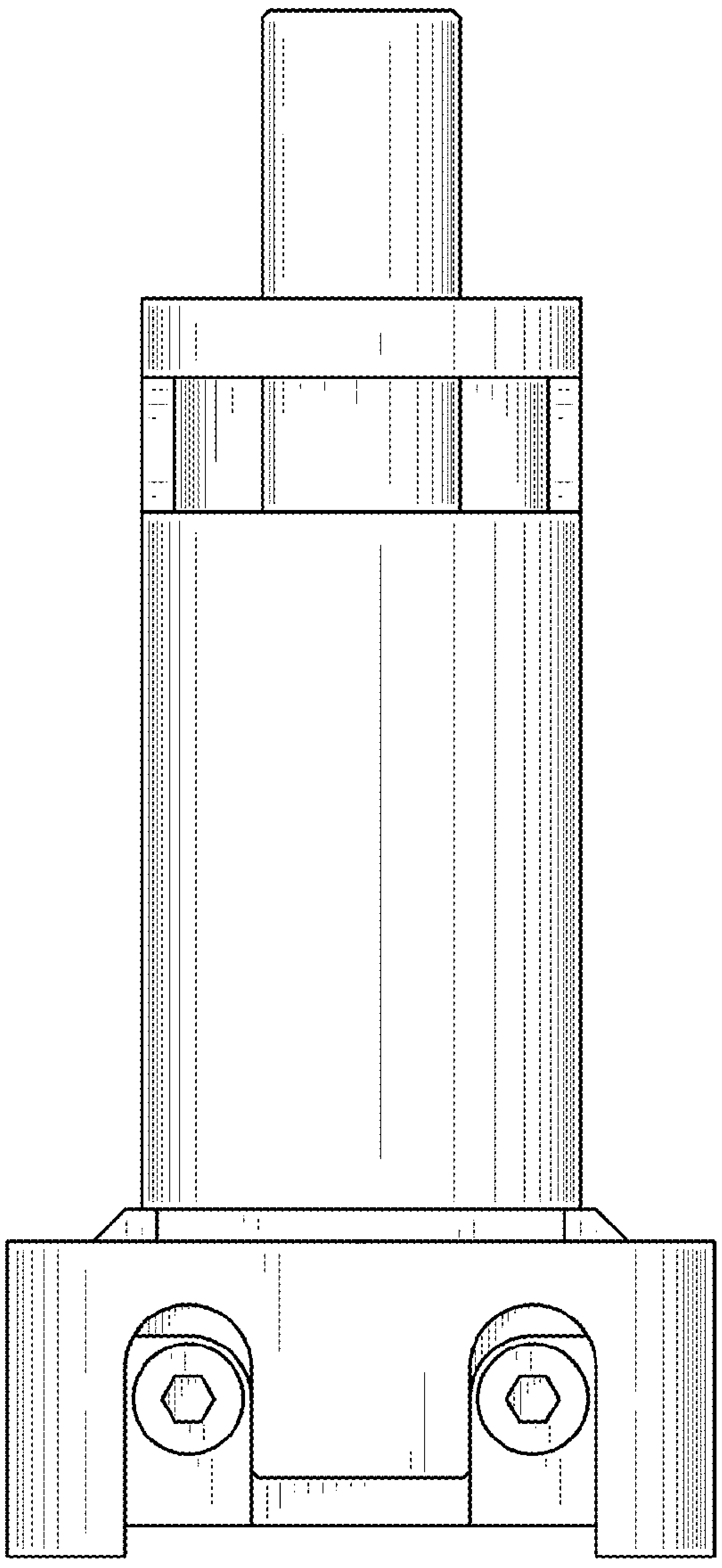

FIG. 3

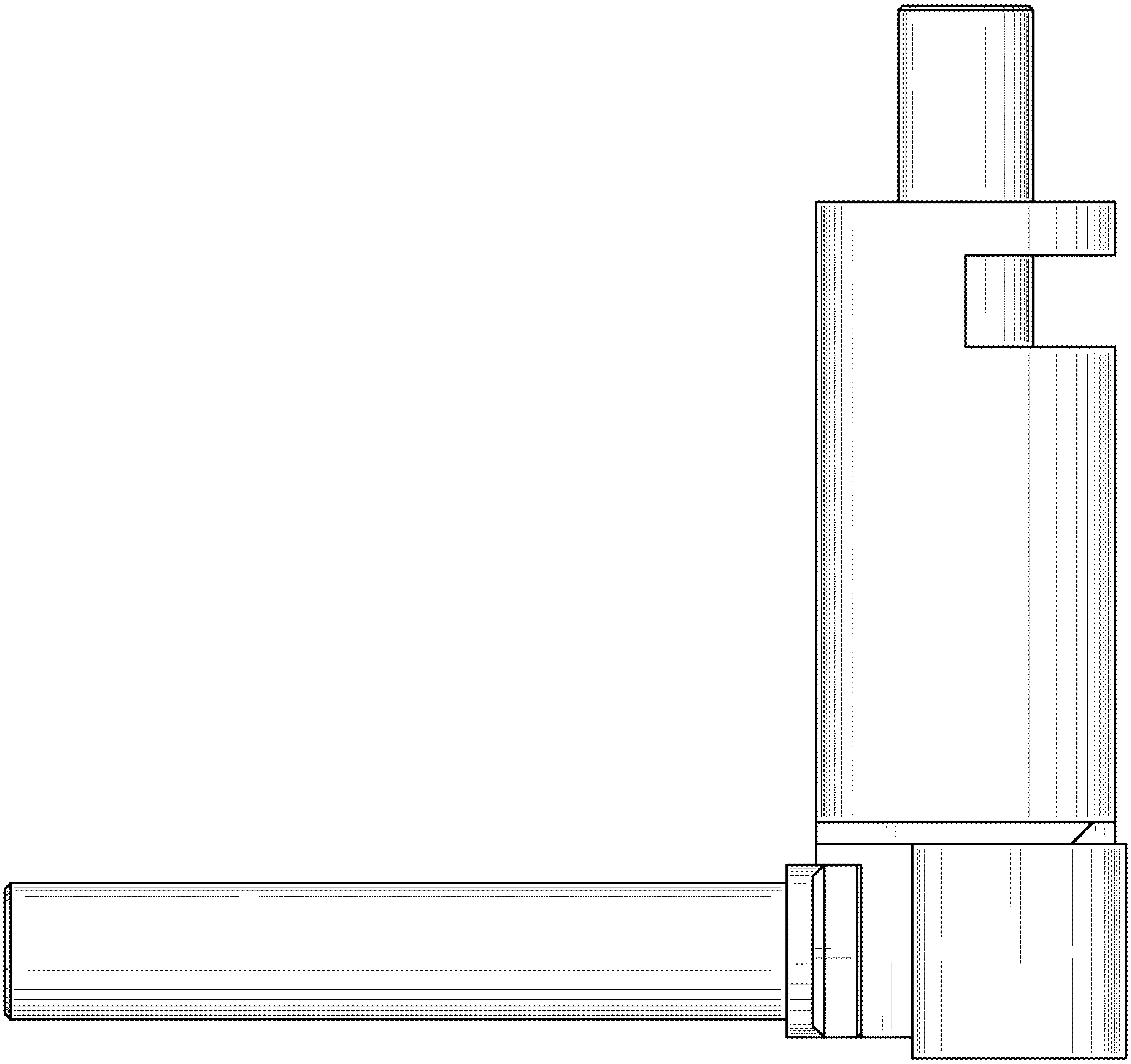

FIG. 4

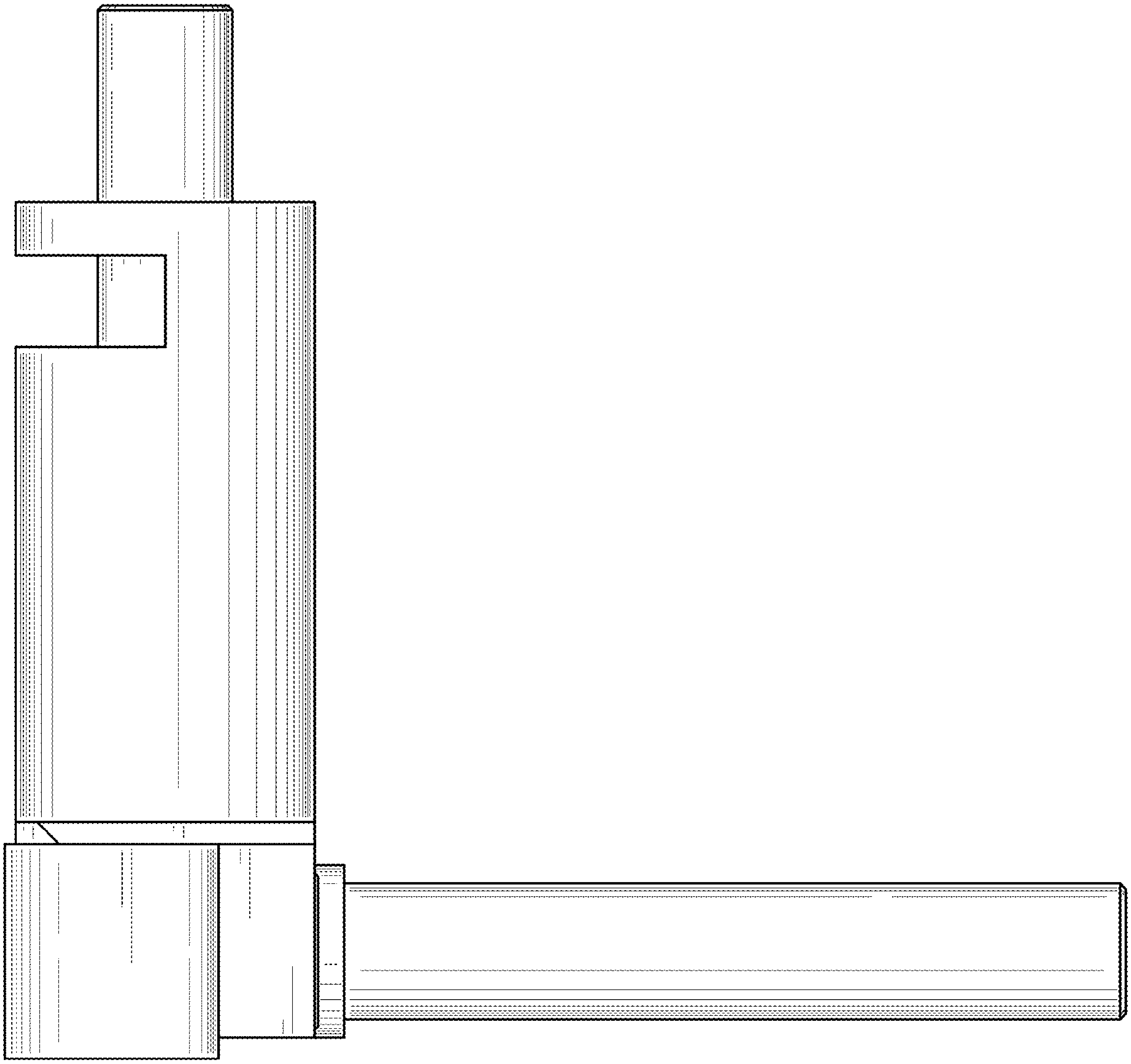

FIG. 5

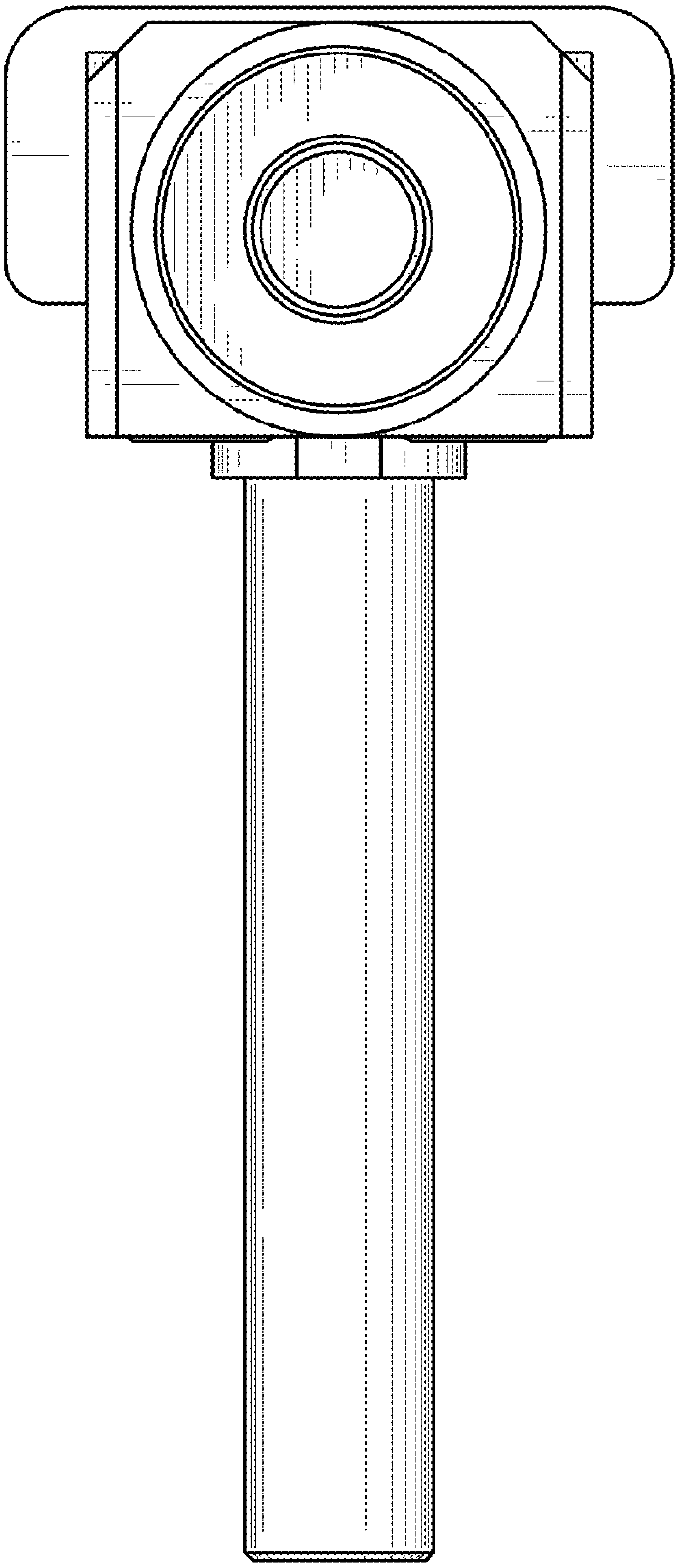

FIG. 6

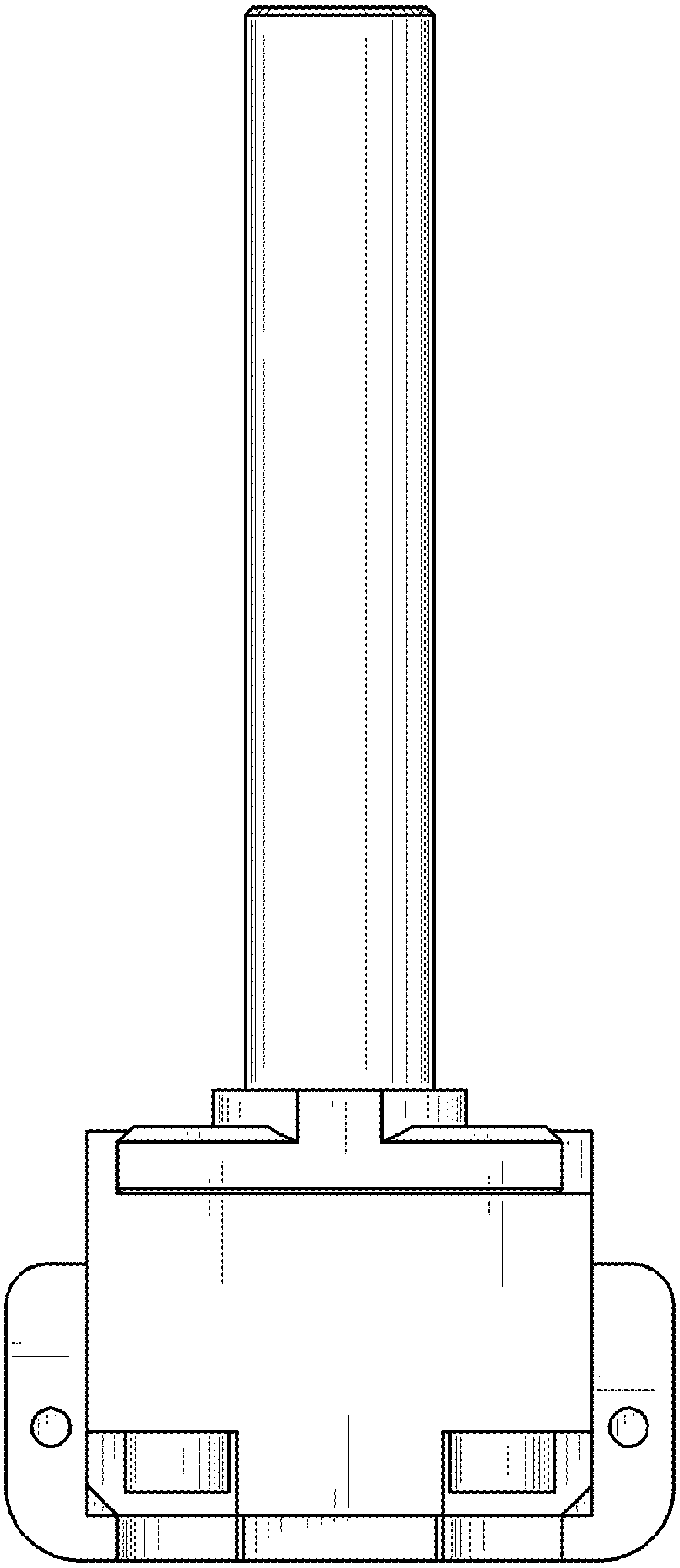

FIG. 7

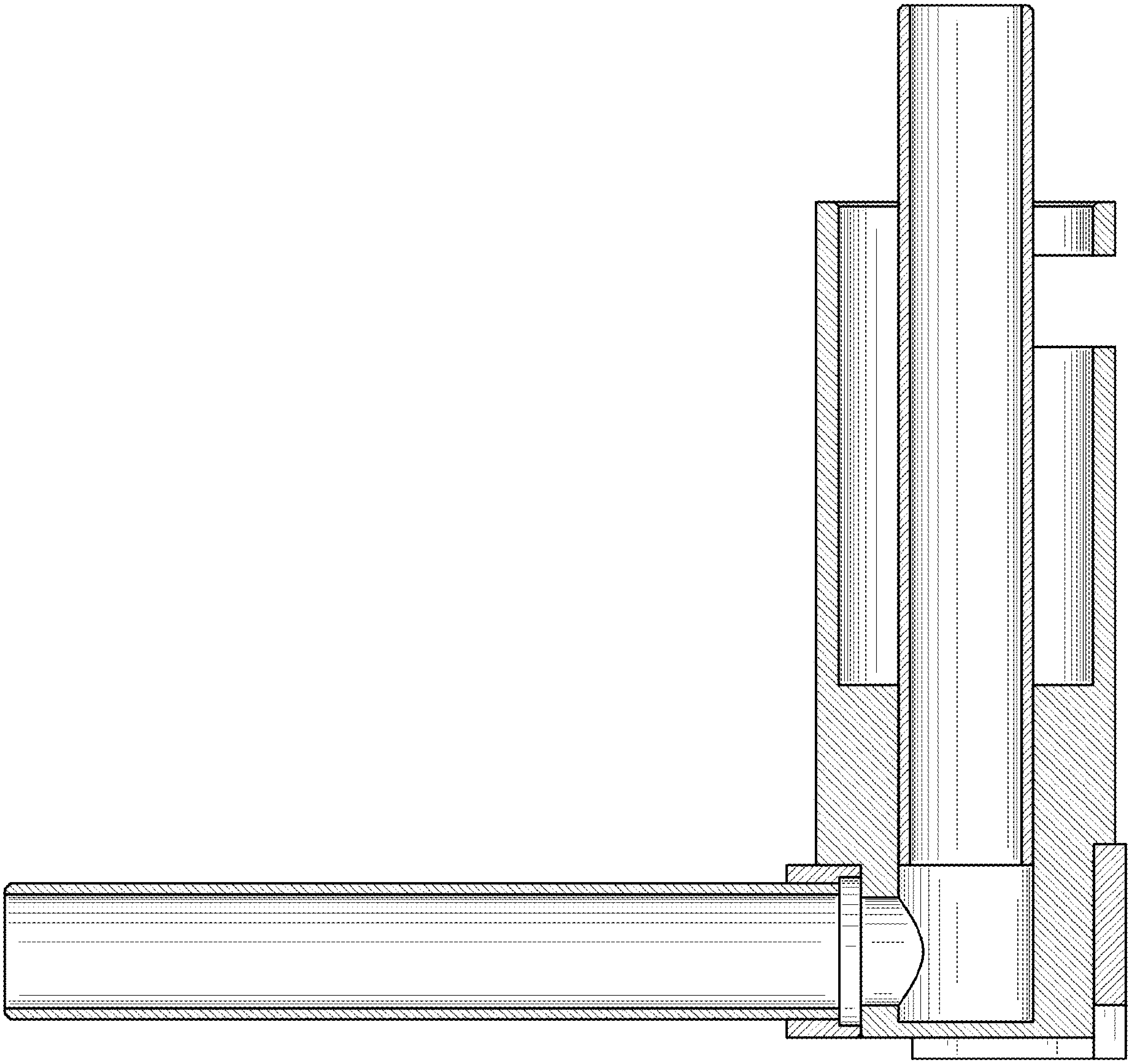

FIG. 8