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(12) **United States Design Patent** (10) **Patent No.:** **US D901,405 S**
Saito et al. (45) **Date of Patent:** **** Nov. 10, 2020**

(54) **SEMICONDUCTOR DEVICE**

(71) Applicant: **ROHM CO., LTD.**, Kyoto (JP)
(72) Inventors: **Koshun Saito**, Kyoto (JP); **Keiichi Takahashi**, Kyoto (JP)

(73) Assignee: **ROHM CO., LTD.**, Kyoto (JP)

(**) Term: **15 Years**

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(30) **Foreign Application Priority Data**

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(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182, 102, 133, 120
CPC H01L 21/44; H01L 21/48; H01L 21/50;
H01L 23/48; H01L 23/495
See application file for complete search history.

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Primary Examiner — Bridget L Eland

(74) *Attorney, Agent, or Firm* — Hamre, Schumann, Mueller & Larson, P.C.

(57) **CLAIM**

The ornamental design for a semiconductor device, as shown and described.

DESCRIPTION

FIG. 1 is a rear perspective view of a semiconductor device showing our new design;

FIG. 2 is a front perspective view thereof;

FIG. 3 is a top plan view thereof;

FIG. 4 is a front elevation view thereof;

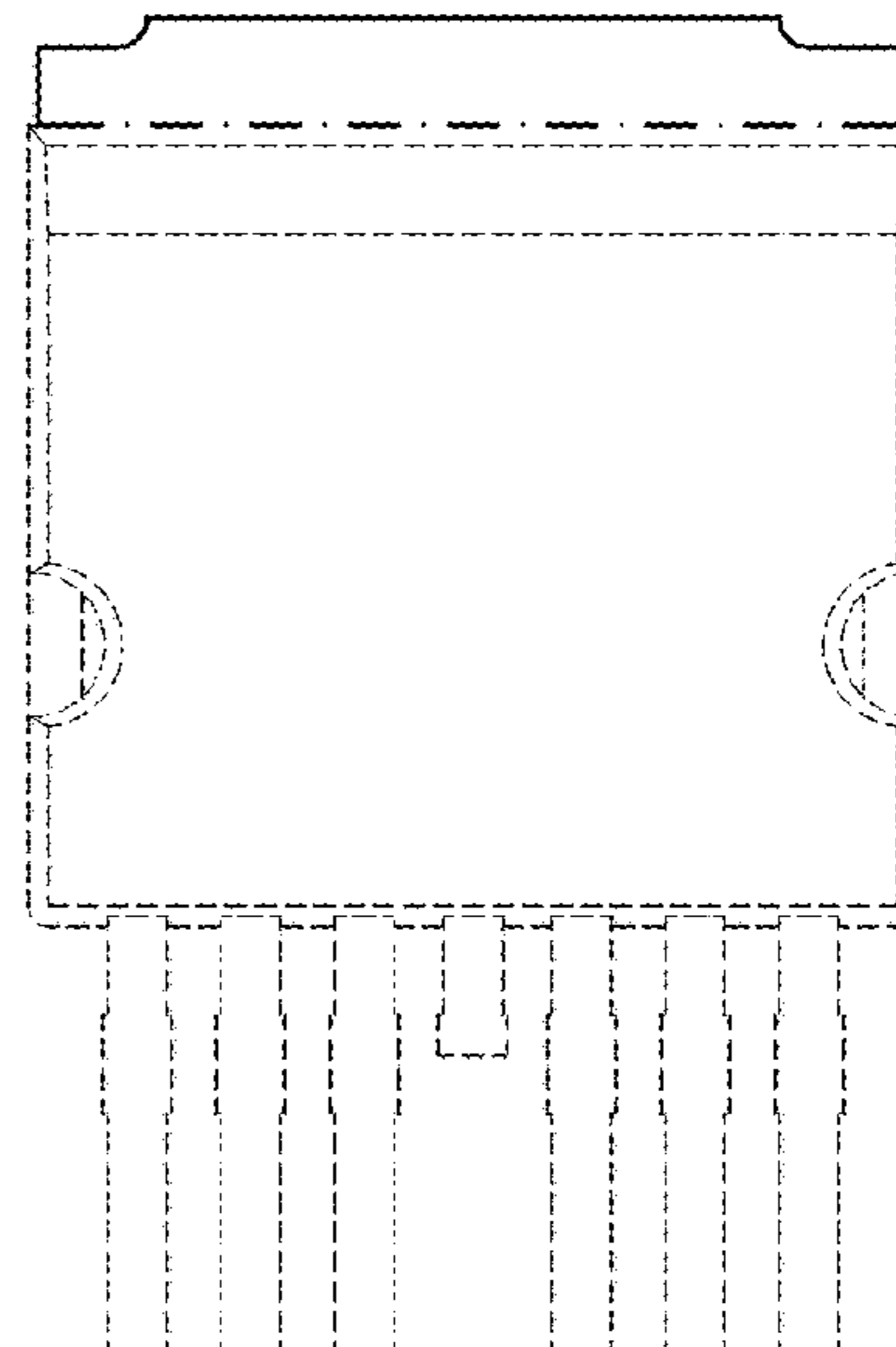
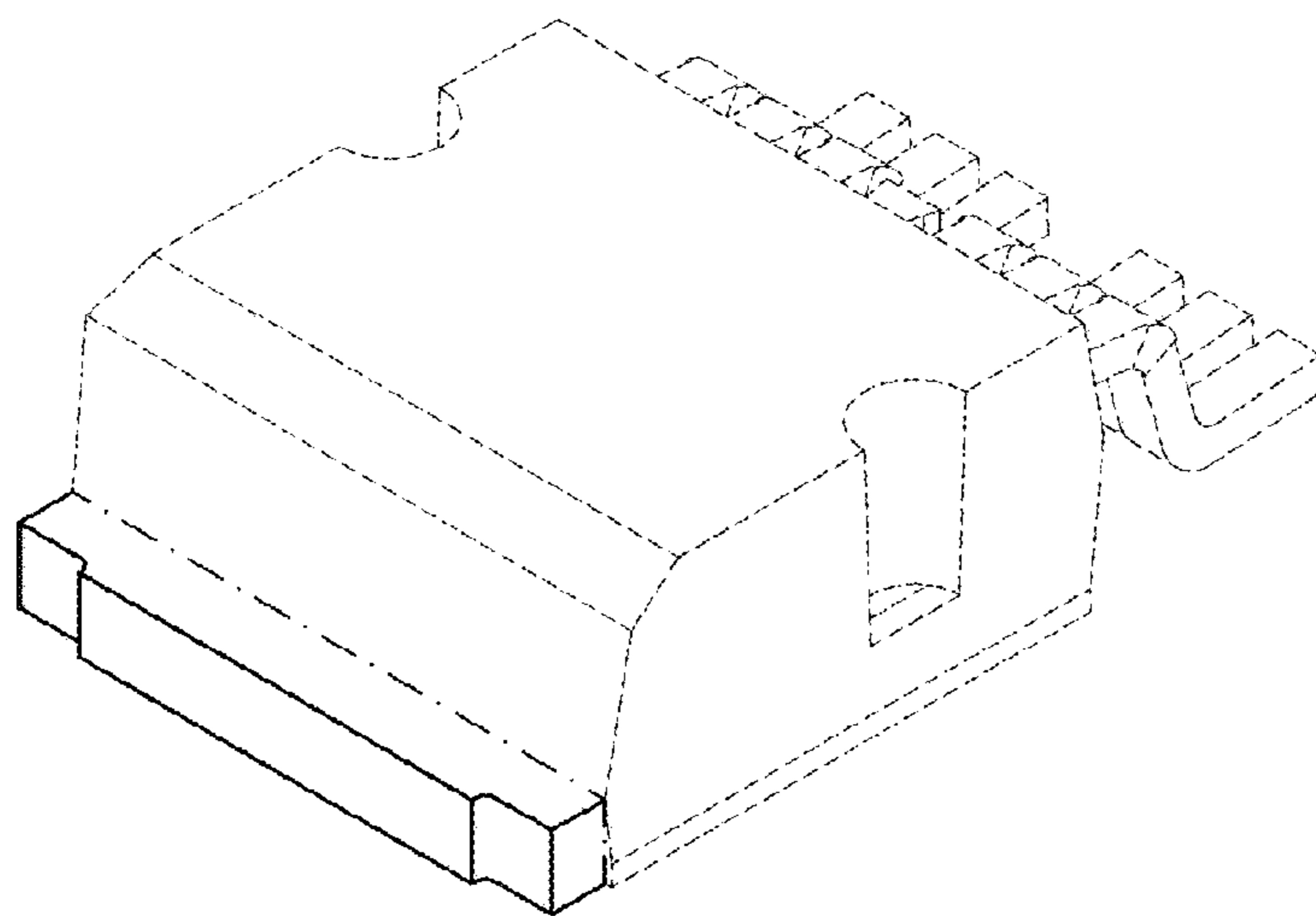
FIG. 5 is a rear elevation view thereof;

FIG. 6 is a bottom plan view thereof; and,

FIG. 7 is a right side view thereof, the left side view thereof being a mirror image.

The dot-dash broken lines represent the bounds of the claimed design, while all other broken lines are directed to environment and are for illustrative purposes only; the broken lines form no part of the claimed design. In addition, the unshaded surfaces in the FIG. 6 view between the solid line edge and the broken lines forms no part of the claimed design.

1 Claim, 4 Drawing Sheets



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Fig. 1

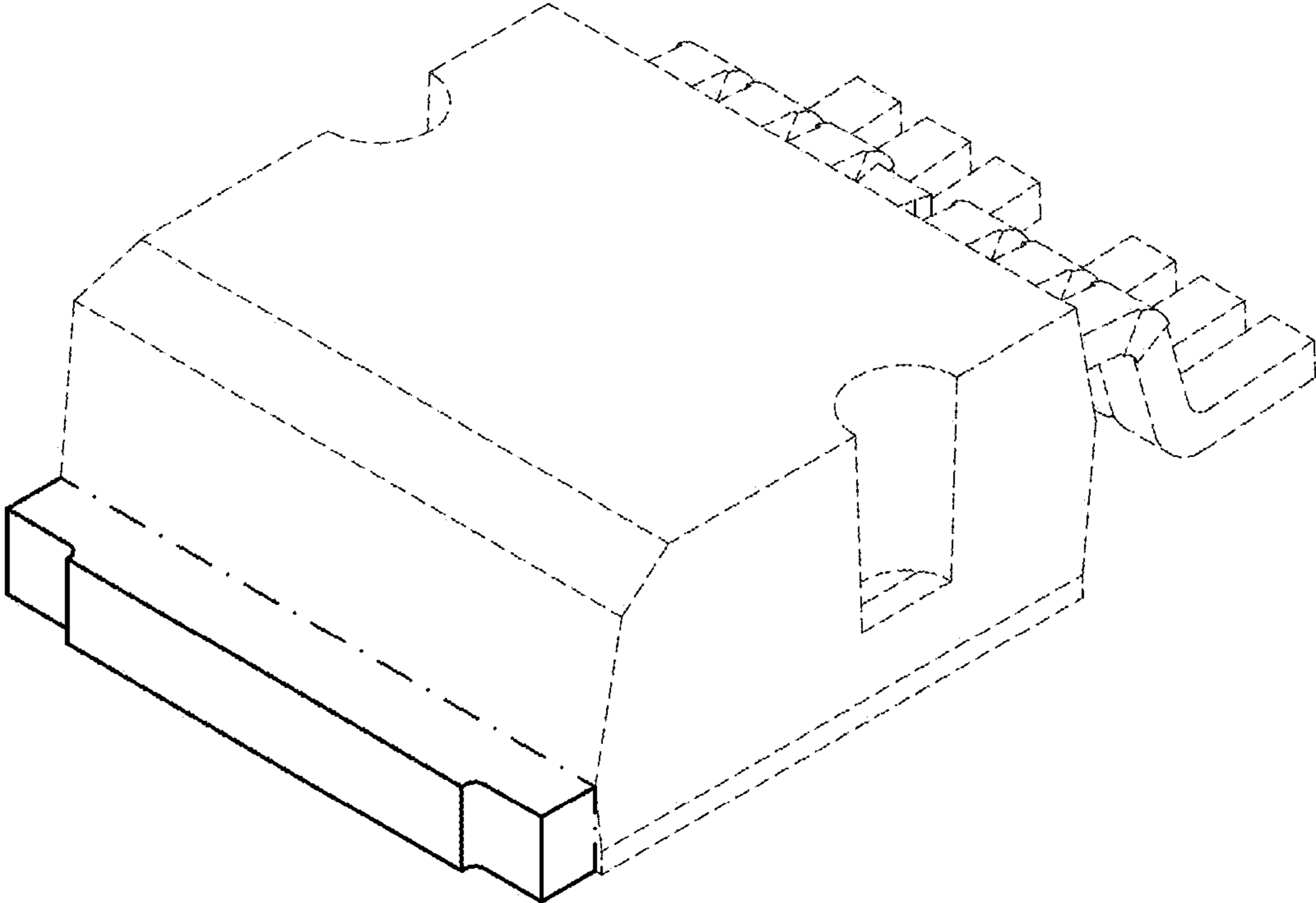


Fig. 2

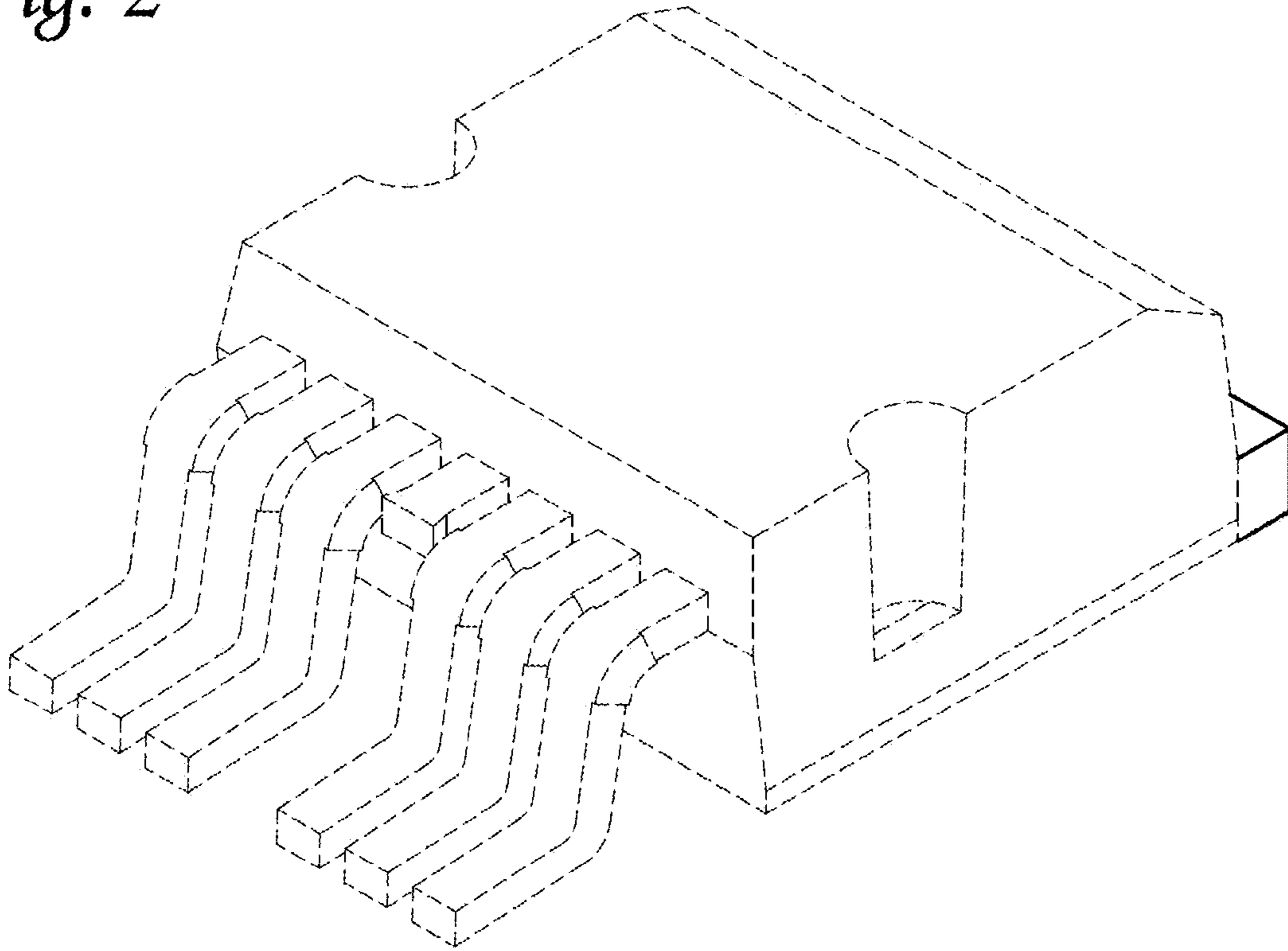


Fig. 3

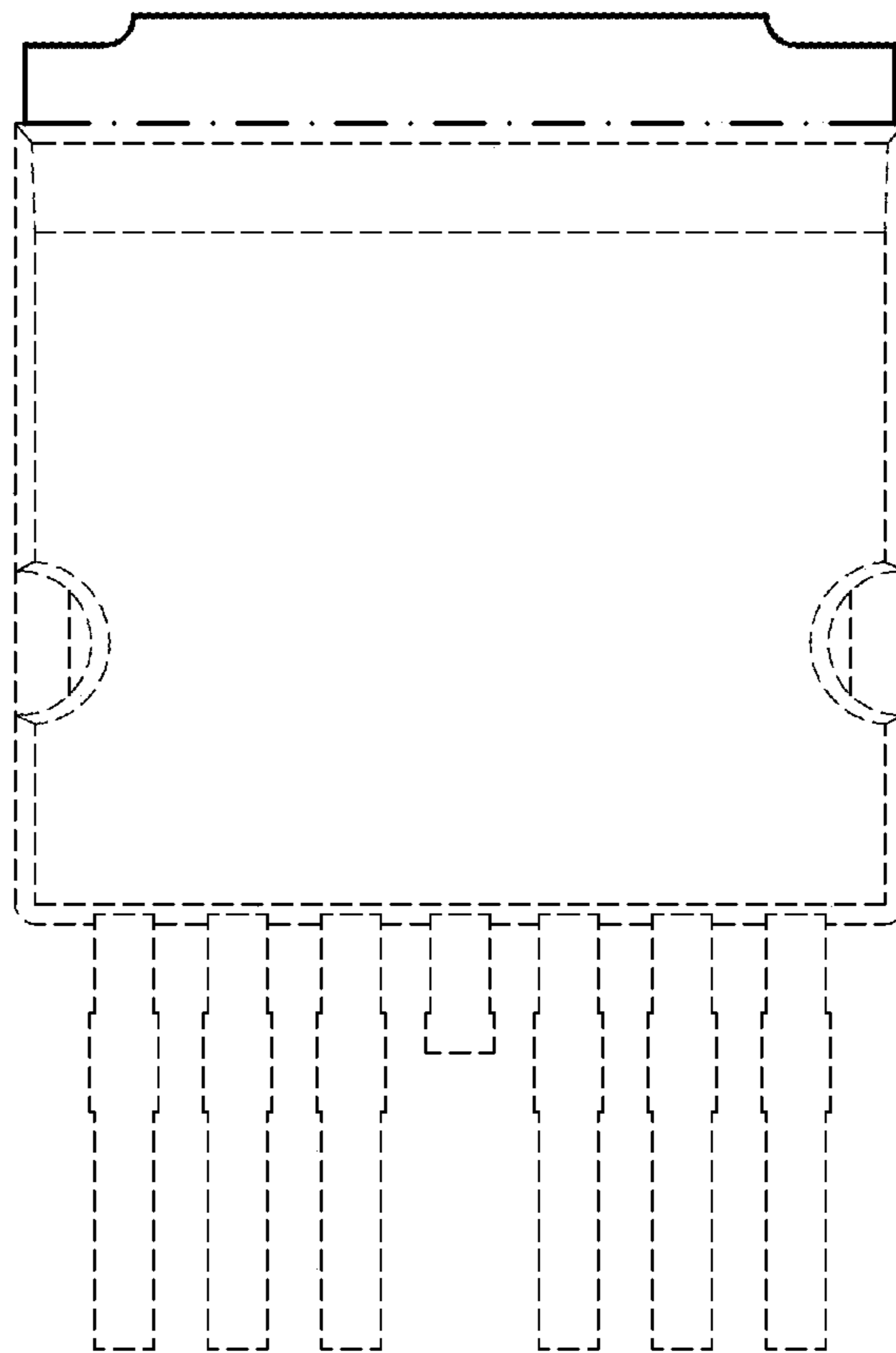


Fig. 4

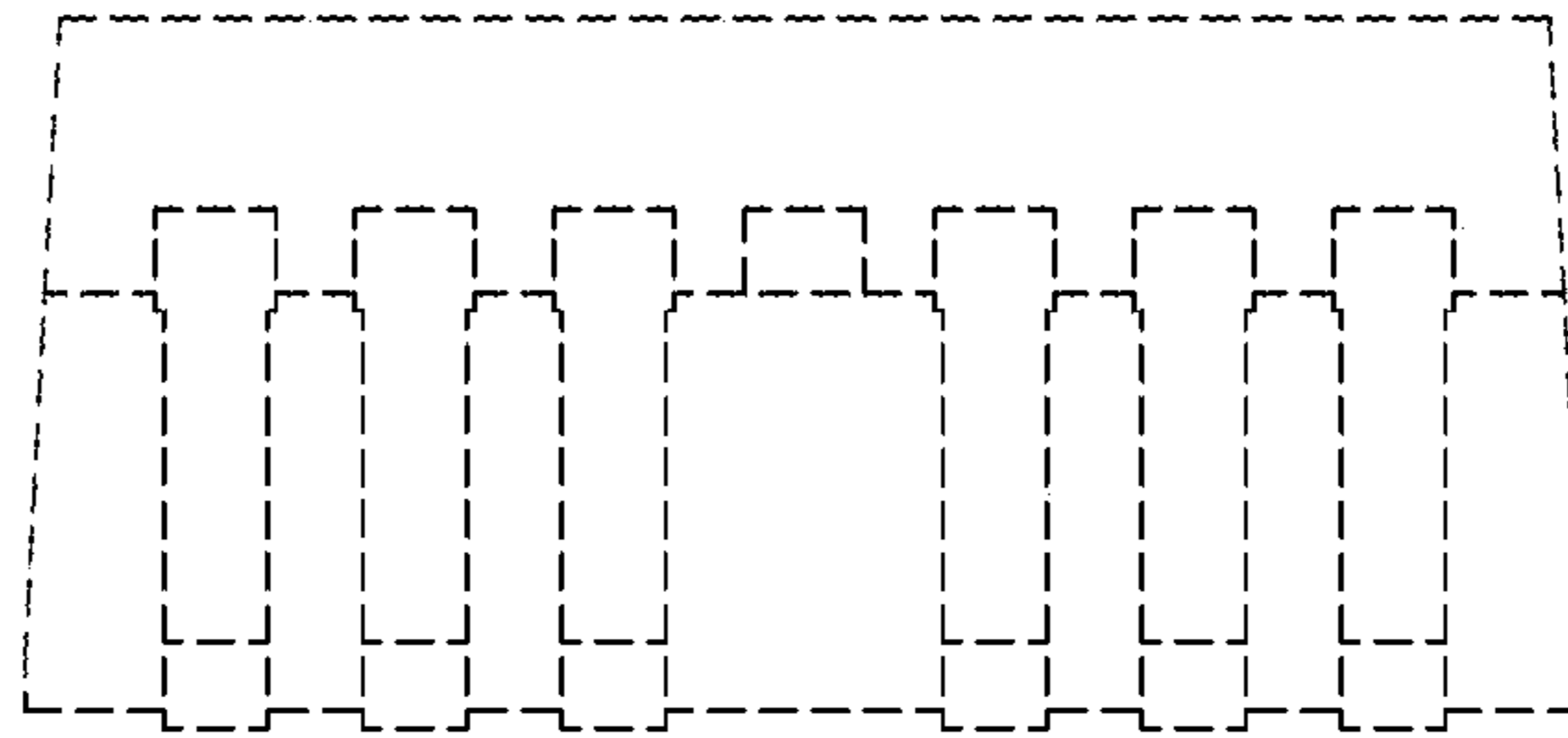


Fig. 5

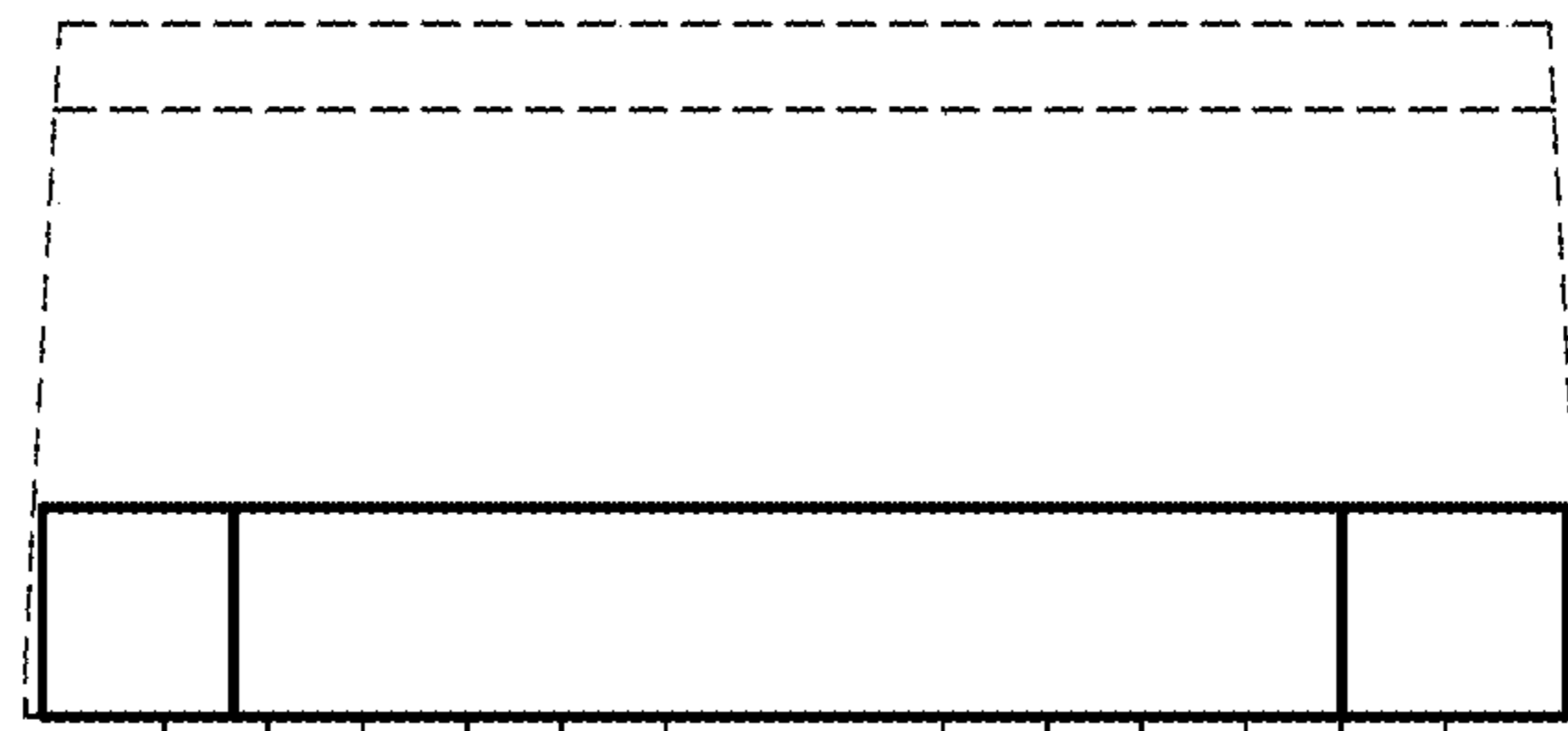


Fig. 6

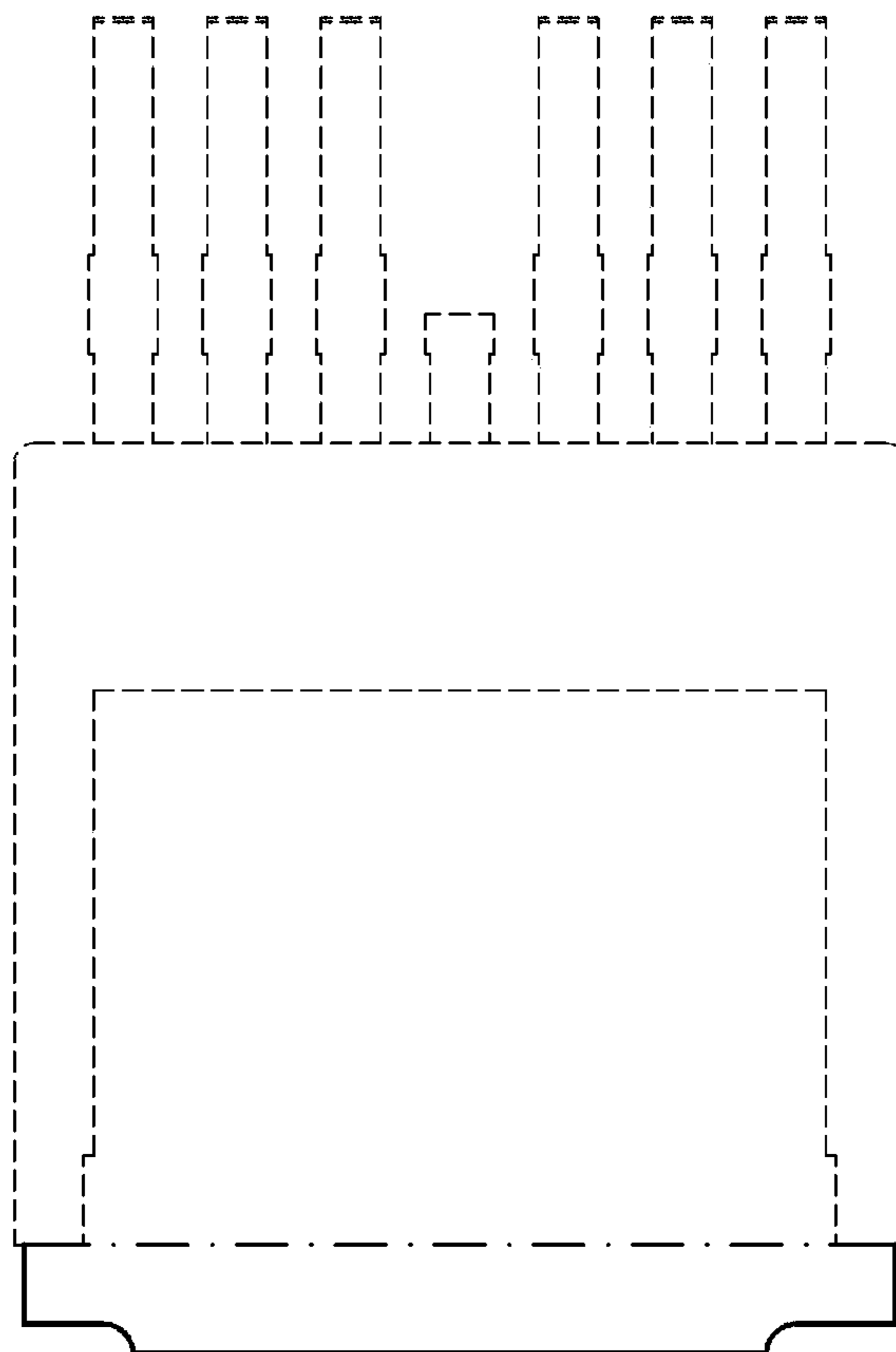


Fig. 7

