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(12) **United States Design Patent** (10) **Patent No.:** **US D891,405 S**
Ramones et al. (45) **Date of Patent:** **** Jul. 28, 2020**

(54) **ELECTRONICS DEVICE MOUNT**

(71) Applicant: **Arlo Technologies, Inc.**, Carlsbad, CA (US)

(72) Inventors: **John Kui Yin Ramones**, San Ramon, CA (US); **Christopher Vincent Fonzo**, Carlsbad, CA (US); **Beau Oyler**, Walnut Creek, CA (US); **Dayne Nathaniel Tanner**, Concord, CA (US)

(73) Assignee: **Arlo Technologies, Inc.**, Carlsbad, CA (US)

(**) Term: **15 Years**

(21) Appl. No.: **29/673,440**

(22) Filed: **Dec. 14, 2018**

(51) **LOC (12) Cl.** **14-03**

(52) **U.S. Cl.**
USPC **D14/238**

(58) **Field of Classification Search**

USPC D14/447, 432, 434, 439, 440, 451, 452,
D14/457, 239, 251-253; D13/133, 147,
D13/152, 184; D8/363, 373, 380;
D6/406.3, 406.4, 406.5, 406.6
CPC A47B 21/04; A47B 2097/006; A47B
2097/005; A47B 2023/049; A45C
2011/002; A45C 2011/003; F16M
2200/00; F16M 13/00

See application file for complete search history.

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Primary Examiner — Janice Hallmark

Assistant Examiner — Harold E Blackwell, II

(74) *Attorney, Agent, or Firm* — Boyle Fredrickson S.C.

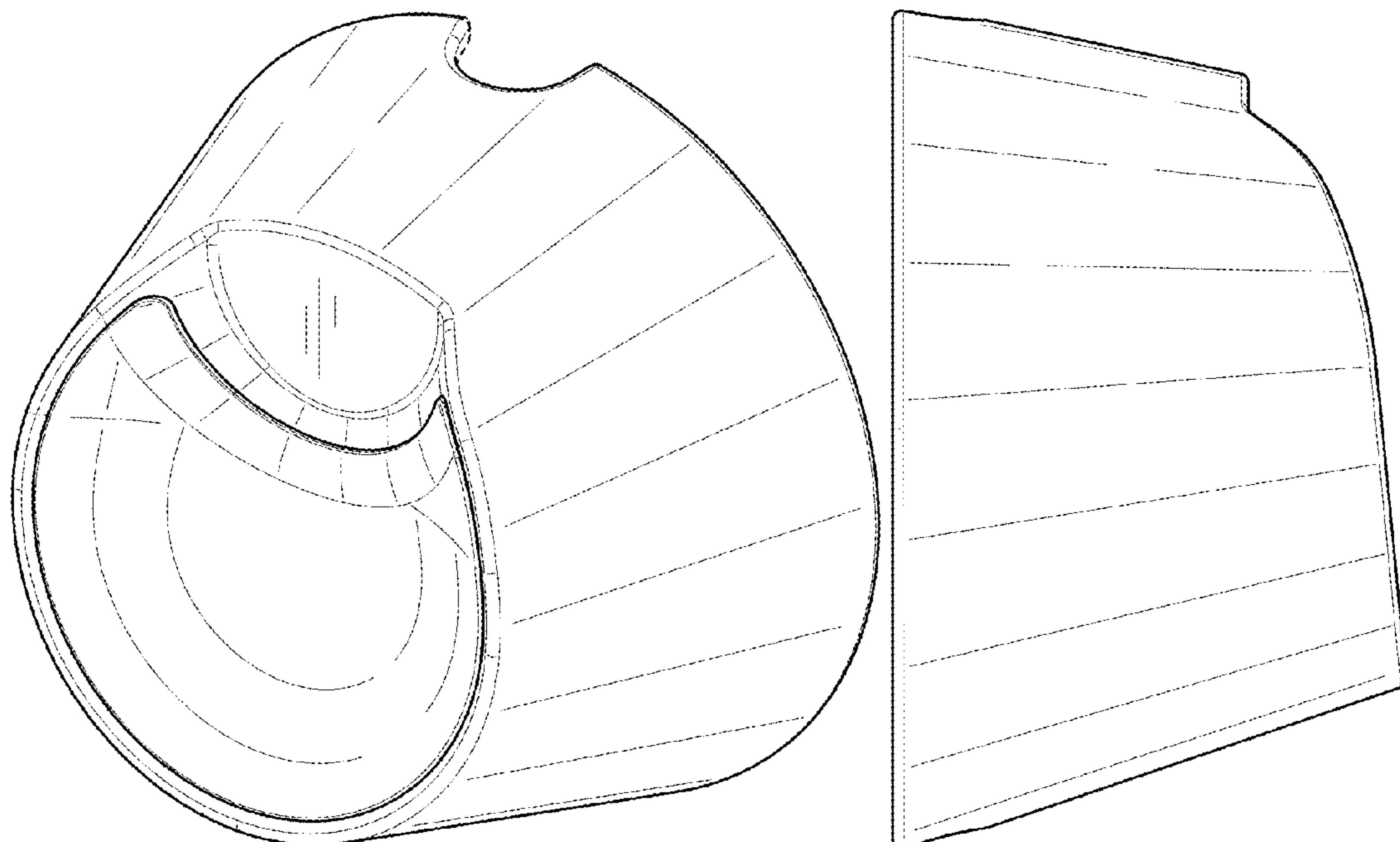
(57) **CLAIM**

The ornamental design for an electronics device mount, as shown and described.

DESCRIPTION

FIG. 1 is a top, front, right side perspective view of an electronics device mount showing our new design;
FIG. 2 is a front elevation view thereof;
FIG. 3 is a rear elevation view thereof;
FIG. 4 is a right-side elevation view thereof;
FIG. 5 is a left-side elevation view thereof;
FIG. 6 is a top plan view thereof; and,
FIG. 7 is a bottom plan view thereof.
The broken lines in the drawings represent the boundary of the claimed design. All of the broken lines form no part of the claimed design.

1 Claim, 7 Drawing Sheets



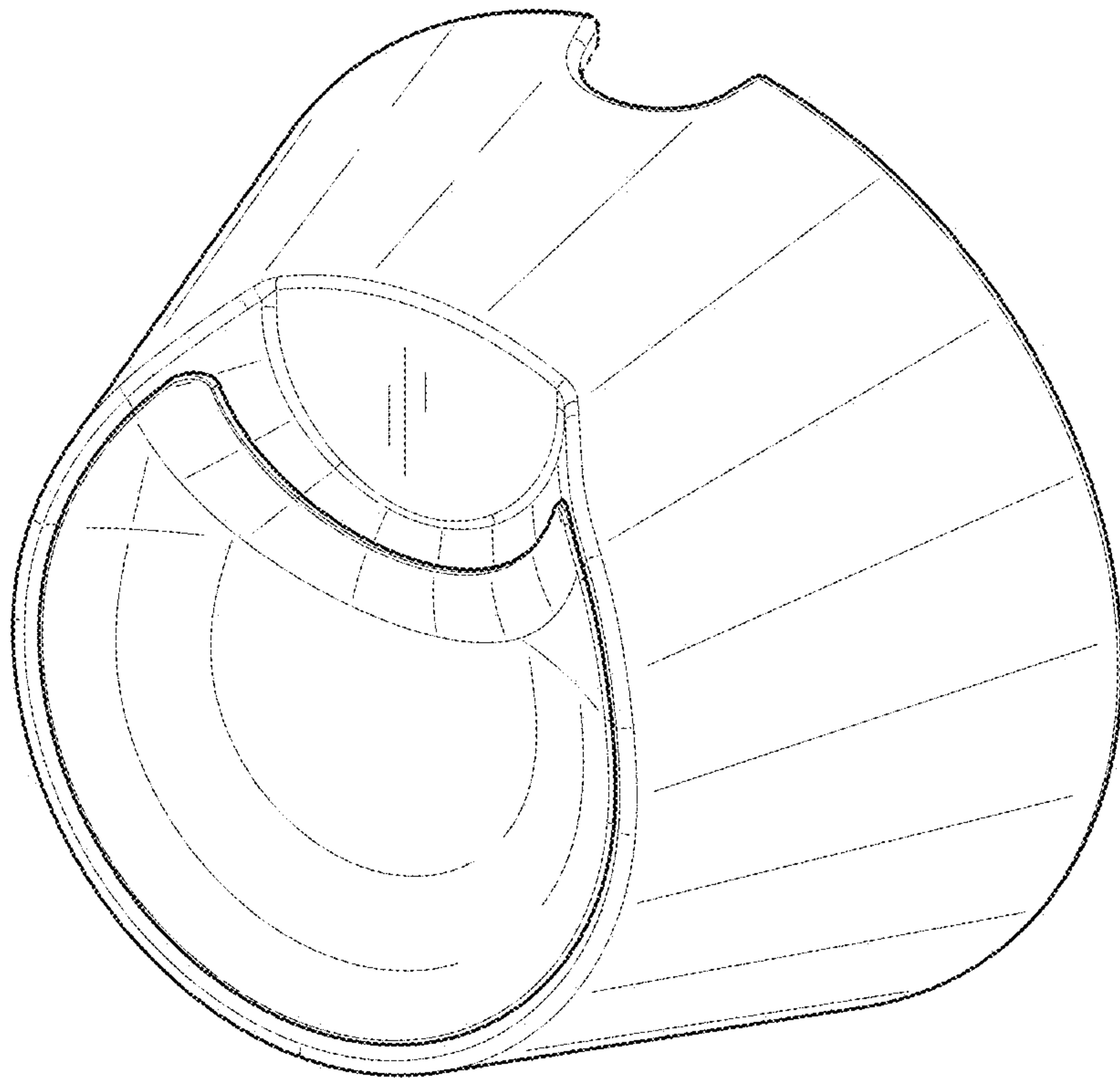


FIG. 1

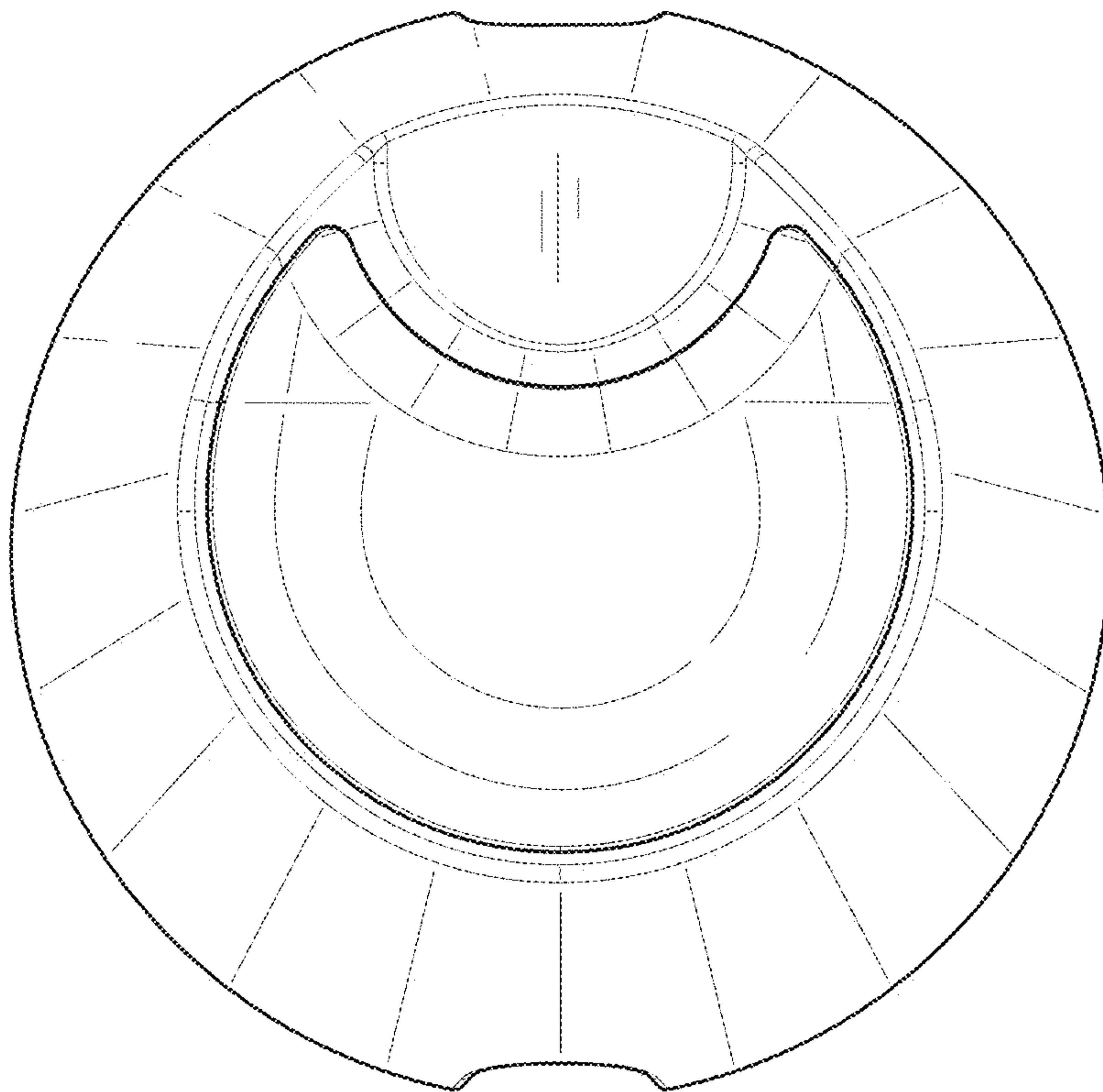


FIG. 2

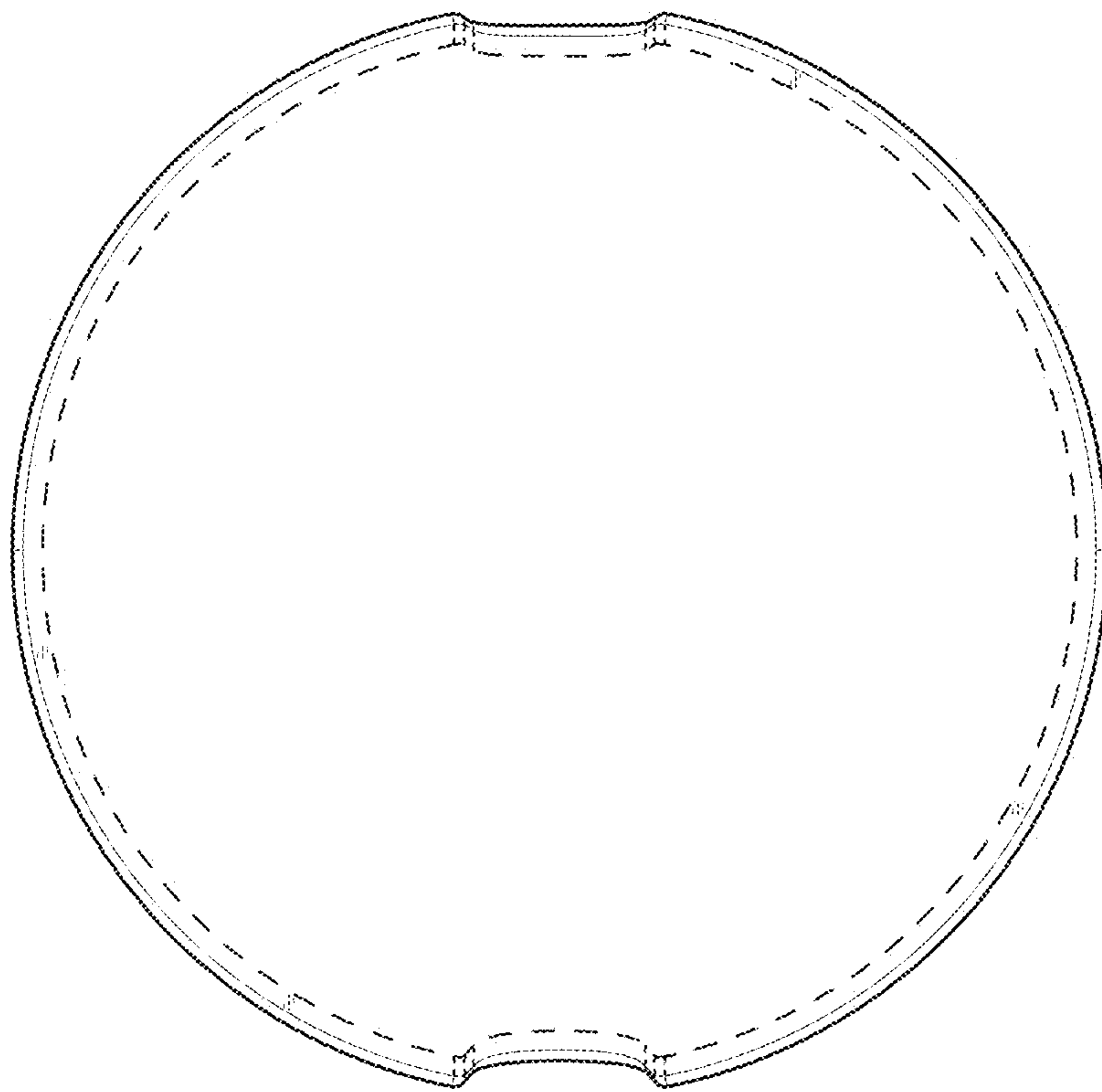


FIG. 3

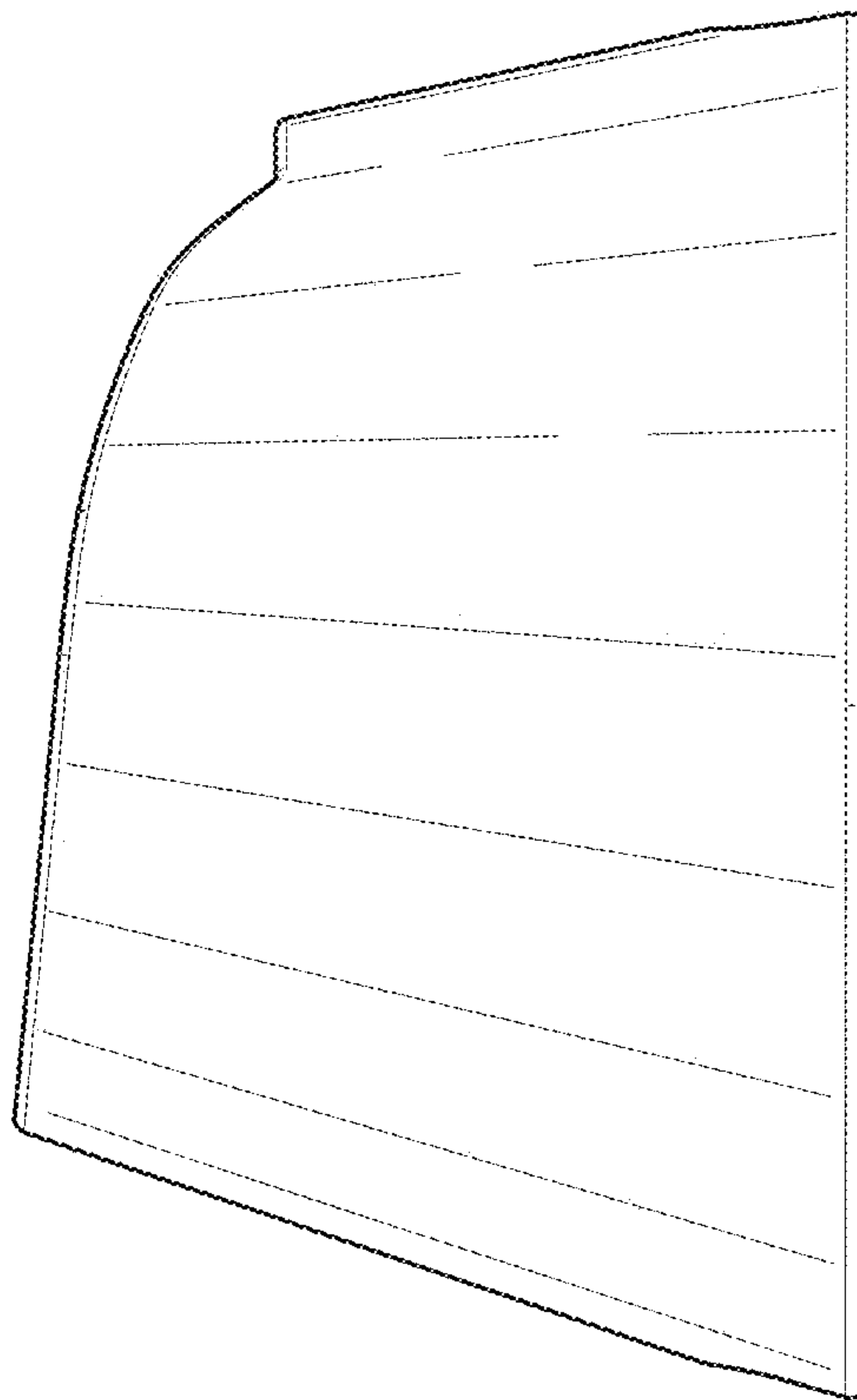


FIG. 4

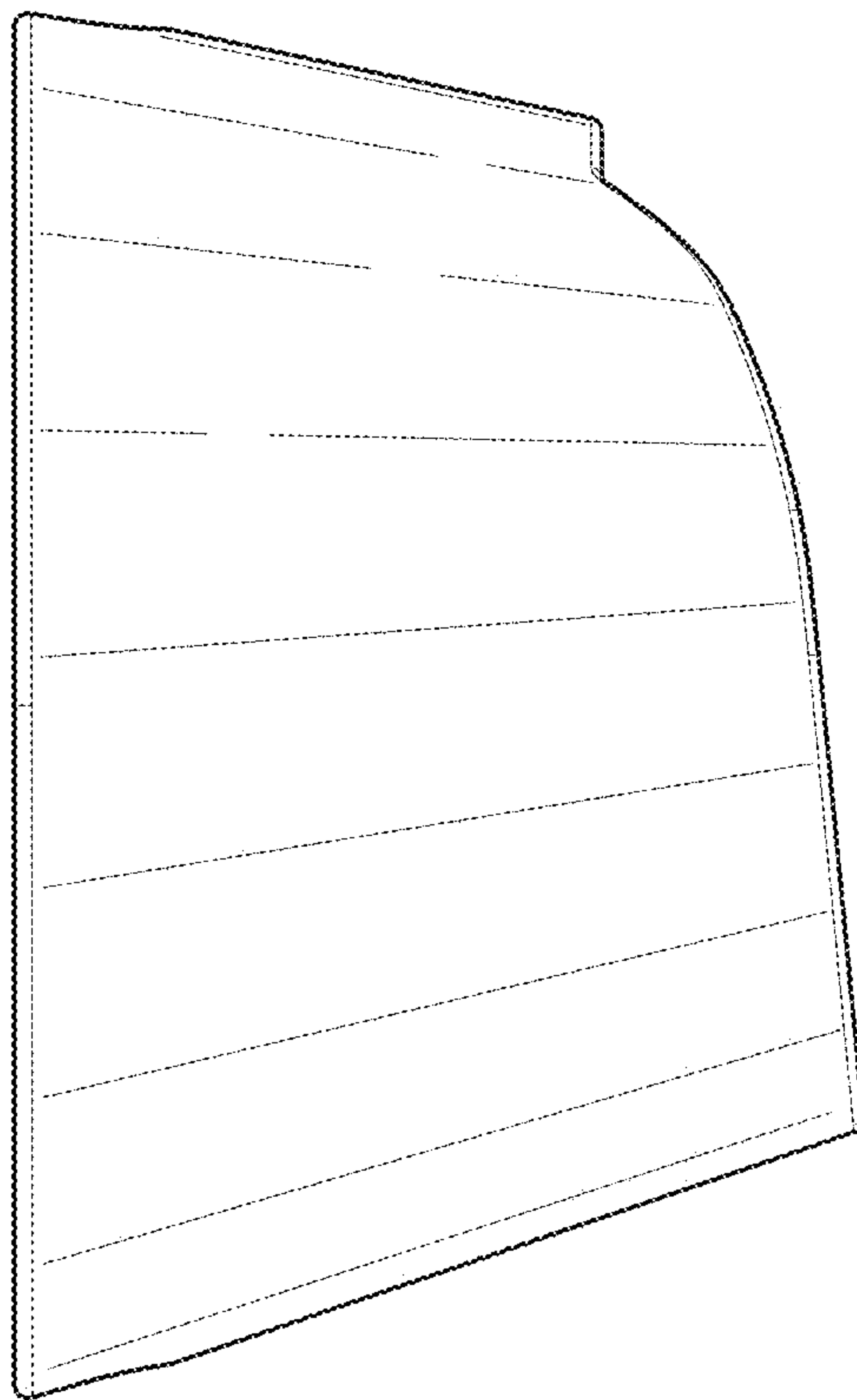


FIG. 5

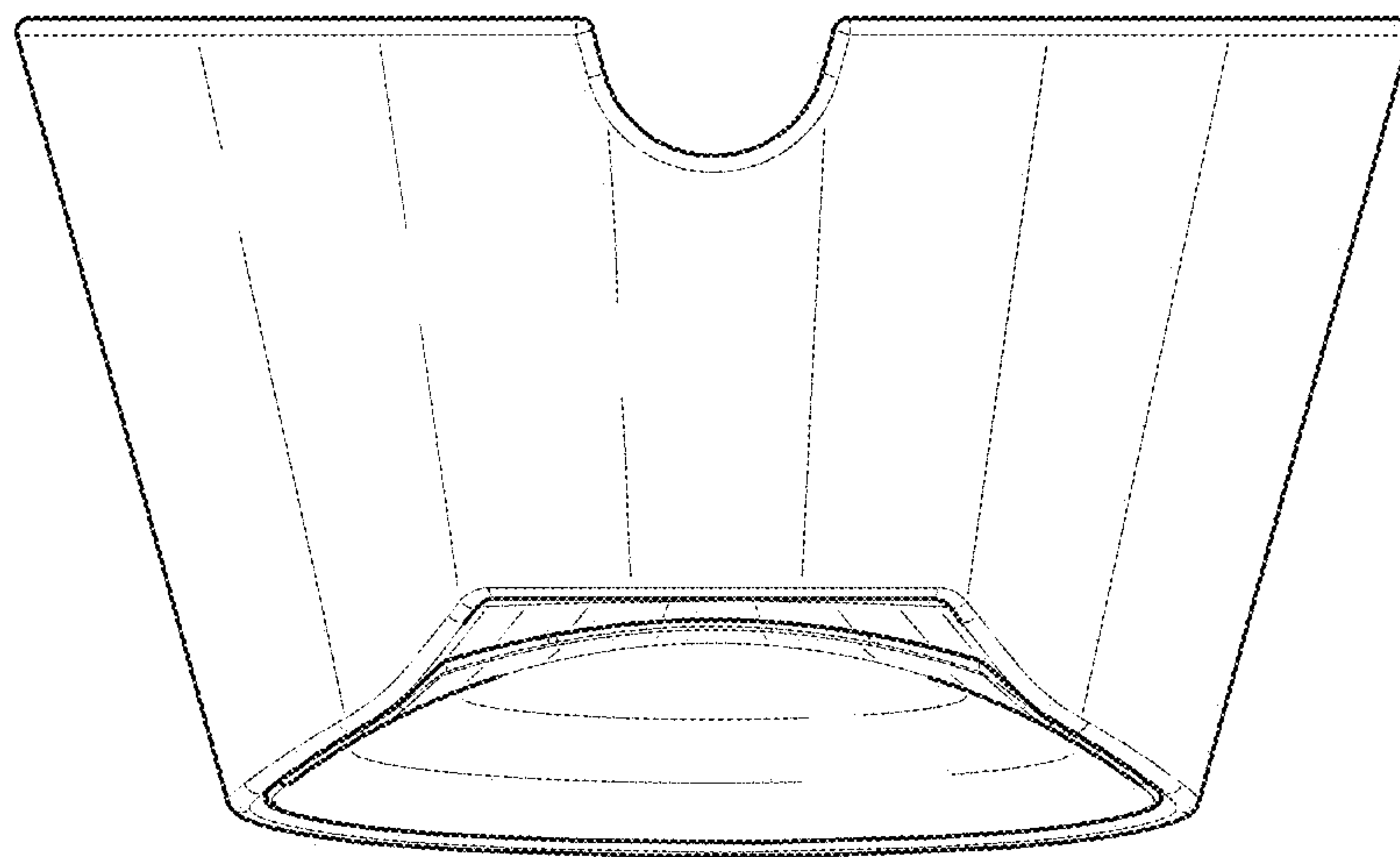


FIG. 6

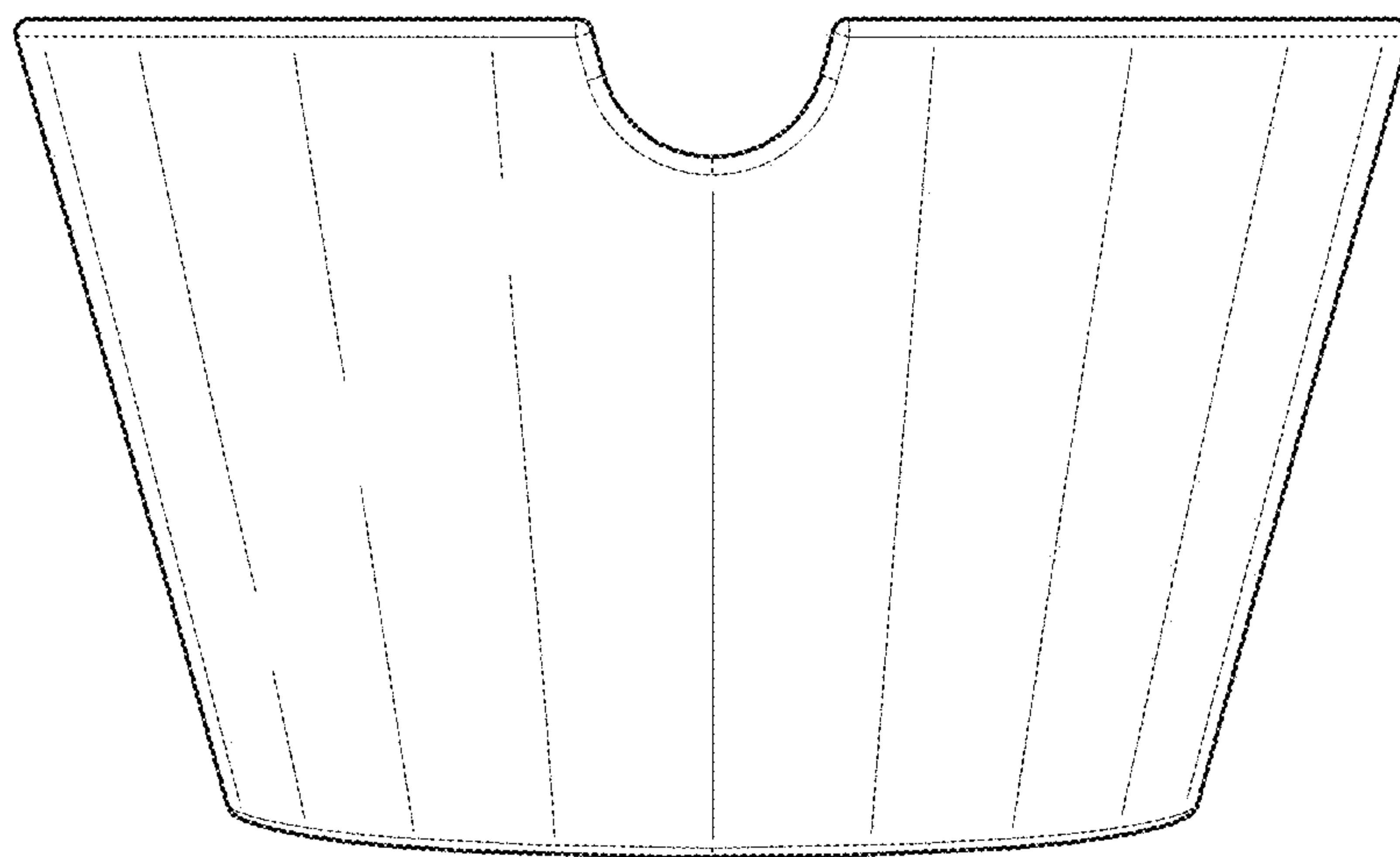


FIG. 7