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(12) **United States Design Patent**  
**Thompson**

(10) **Patent No.:** **US D887,448 S**

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- (54) **ELECTRONICS ENCLOSURE**
- (71) Applicant: **Bernard Jeffery Thompson**, Bellevue, WA (US)
- (72) Inventor: **Bernard Jeffery Thompson**, Bellevue, WA (US)
- (\*) Notice: This patent is subject to a terminal disclaimer.
- (\*\*) Term: **15 Years**
- (21) Appl. No.: **29/544,910**
- (22) Filed: **Nov. 6, 2015**
- (51) **LOC (12) Cl.** ..... **14-03**
- (52) **U.S. Cl.**  
USPC ..... **D14/496; D14/203.3**
- (58) **Field of Classification Search**  
USPC ..... D14/496, 401, 435, 474, 483, 217, 137, D14/138, 160, 168, 356, 203.1–203.8, D14/507, 188; 345/156, 169, 173–179, 345/905; 715/727–729, 864; 710/1, 5, 8; 713/1, 600; 455/1.1, 1.7, 73, 344–347, 455/93, 95, 3.01–3.06, 550.1, 573.1; 370/342–344; 369/1, 2, 6–12; 463/43–47, 29–35; 273/148 B  
CPC .. A63F 13/02; A63F 13/12; A63F 9/24; A63F 9/02; A63F 11/00; A63F 71/00; G06F 3/02; G06G 3/033; G09G 5/00  
See application file for complete search history.

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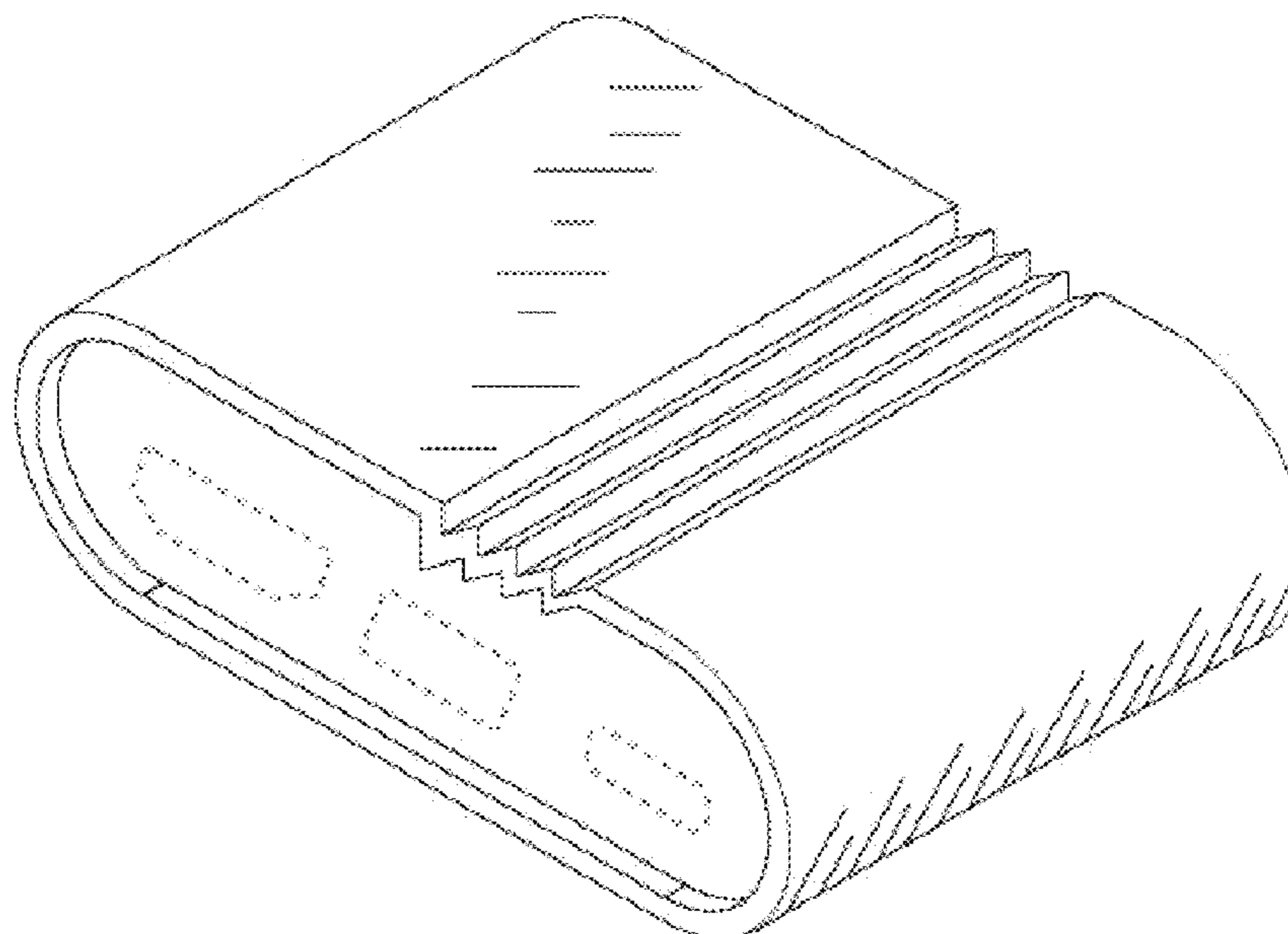
(57) **CLAIM**

The ornamental design for an electronics enclosure, as shown and described.

**DESCRIPTION**

FIG. 1 is a top and front perspective view of an electronics enclosure showing my new design;  
 FIG. 2 is a top and front perspective view thereof, shown in environmental use;  
 FIG. 3 is a front elevational view of FIG. 1;  
 FIG. 4 is a front elevational view of FIG. 2; and,  
 FIG. 5 is a rear elevational view thereof.  
 The broken lines environment is for illustration only and forms no part of the claimed design.

**1 Claim, 5 Drawing Sheets**



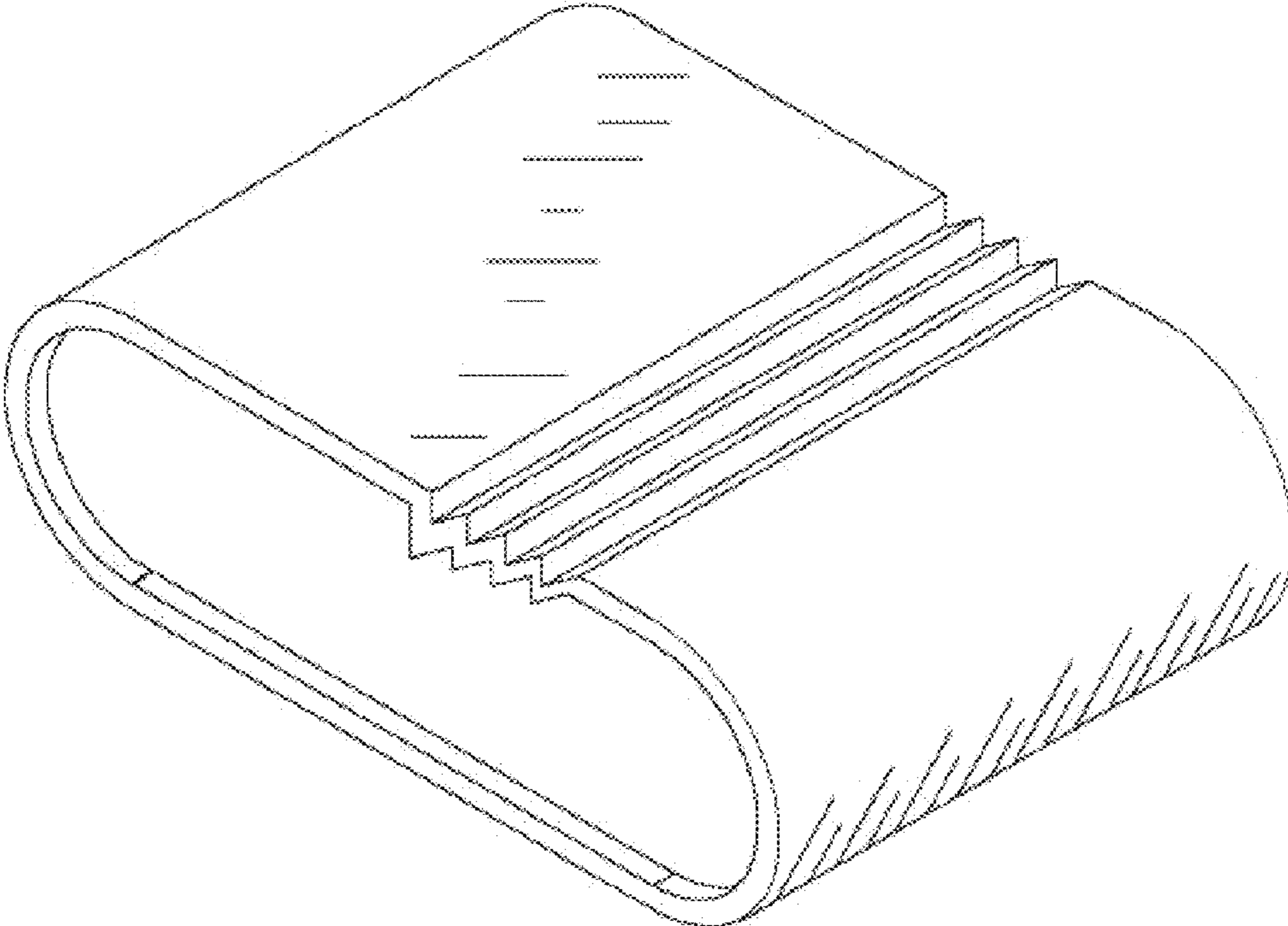


FIG. 1

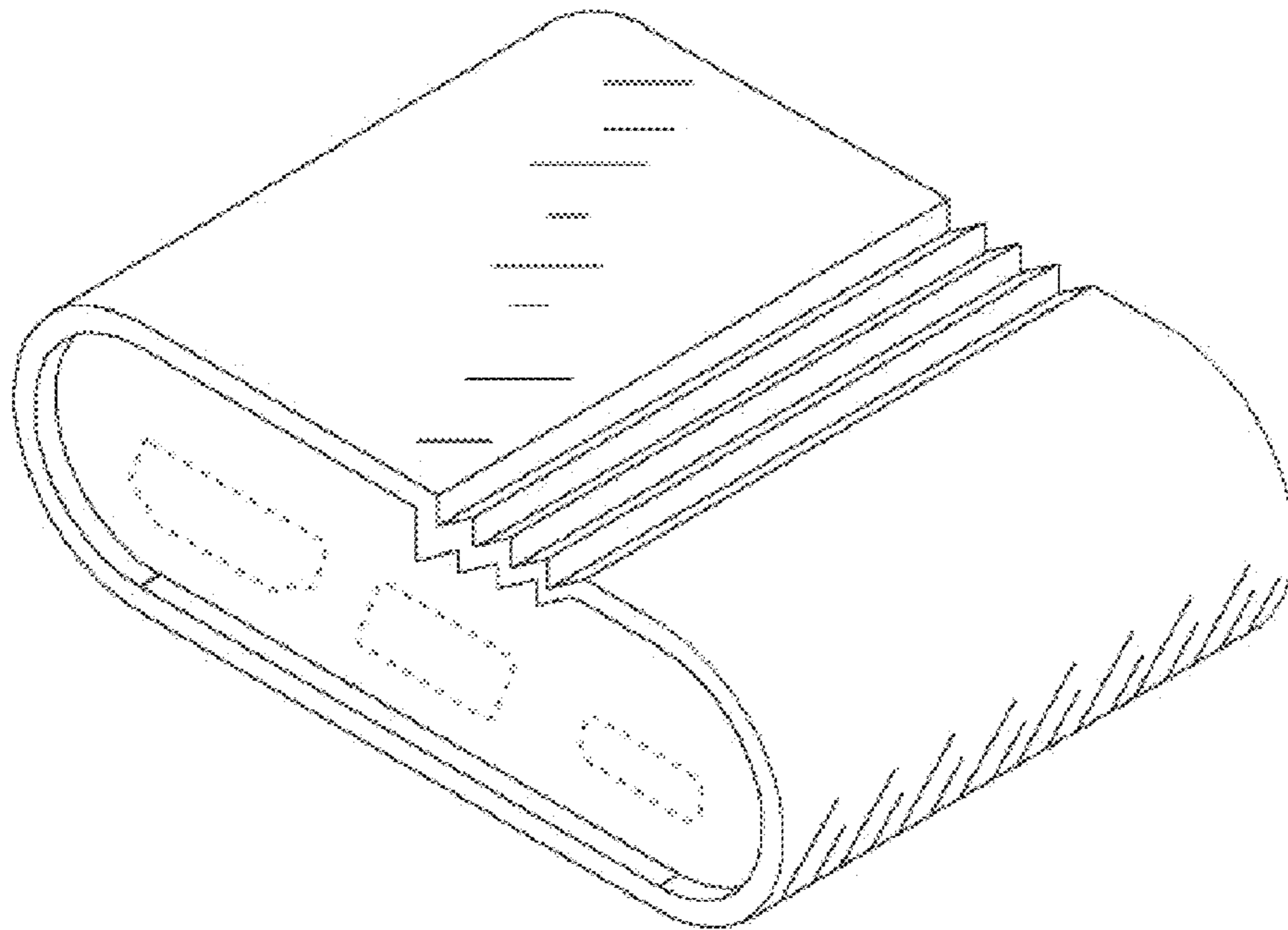


FIG. 2

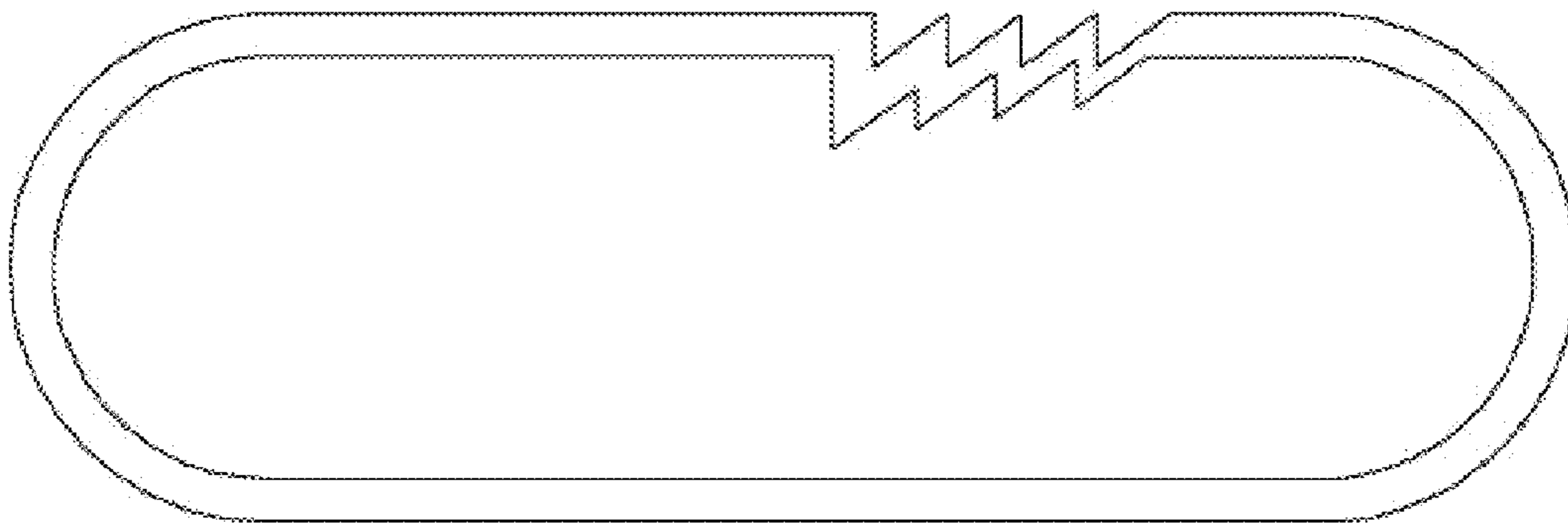


FIG. 3

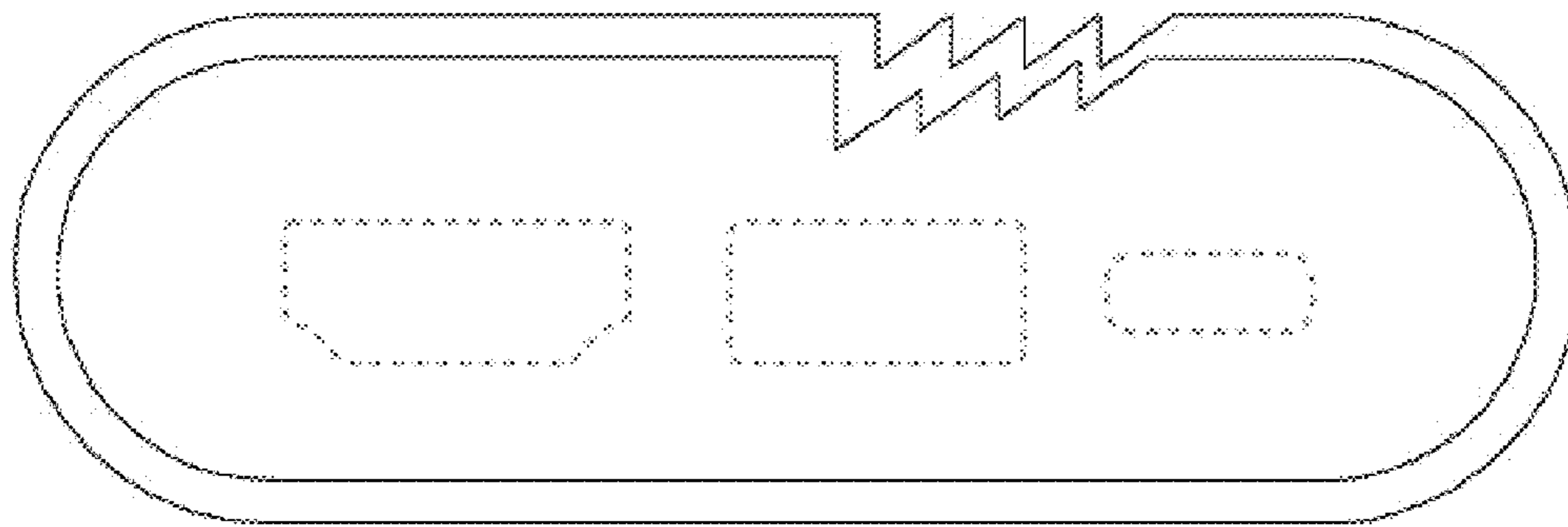


FIG. 4

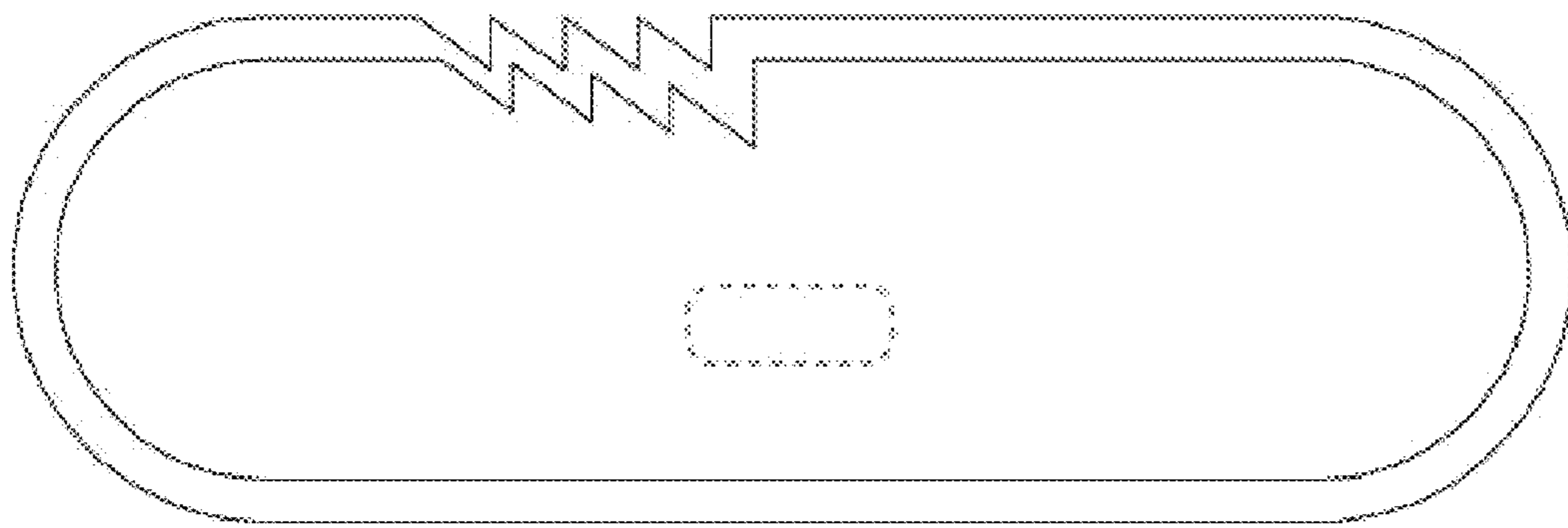


FIG. 5