

US00D874412S

(12) **United States Design Patent** (10) **Patent No.:** **US D874,412 S**
Kanda et al. (45) **Date of Patent:** **** Feb. 4, 2020**

(54) **SEMICONDUCTOR MODULE**

(71) Applicant: **ROHM CO., LTD.**, Kyoto-shi, Kyoto (JP)

(72) Inventors: **Takumi Kanda**, Kyoto (JP); **Masashi Hayashiguchi**, Kyoto (JP)

(73) Assignee: **ROHM CO., LTD.**, Kyoto (JP)

(**) Term: **15 Years**

(21) Appl. No.: **29/666,188**

(22) Filed: **Oct. 10, 2018**

(30) **Foreign Application Priority Data**

Apr. 13, 2018 (JP) 2018-008231

Apr. 13, 2018 (JP) 2018-008233

(51) **LOC (12) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182

(Continued)

(56) **References Cited**

U.S. PATENT DOCUMENTS

D394,244 S * 5/1998 Majumdar D13/182

D401,912 S * 12/1998 Majumdar D13/182

D448,739 S * 10/2001 Iwasaki D13/182

D505,399 S * 5/2005 Yoshida D13/182

D606,951 S * 12/2009 Soyano D13/182

(Continued)

FOREIGN PATENT DOCUMENTS

JP 1145764 S 7/2002

JP 1146361 S 7/2002

(Continued)

Primary Examiner — Antoine Duval Davis

(74) *Attorney, Agent, or Firm* — Hamre, Schumann, Mueller & Larson, P.C.

(57) **CLAIM**

The ornamental design for a semiconductor module, as shown and described.

DESCRIPTION

FIG. 1 is a front, top and left side perspective view of a first embodiment of a semiconductor module showing our new design;

FIG. 2 is a rear, bottom, and right side perspective view thereof;

FIG. 3 is a front view thereof;

FIG. 4 is a rear view thereof;

FIG. 5 is a top plan view thereof;

FIG. 6 is a bottom plan view thereof;

FIG. 7 is a left side view thereof;

FIG. 8 is an enlarged cross-sectional view at the portion of 8-8 taken along line 8-8 in FIG. 5;

FIG. 9 is an enlarged cross-sectional view taken along line 9-9 in FIG. 5;

FIG. 10 is a front, top and left side perspective view of a second embodiment of a semiconductor module showing our new design;

FIG. 11 is a rear, bottom, and right side perspective view thereof;

FIG. 12 is a front view thereof;

FIG. 13 is a rear view thereof;

FIG. 14 is a top plan view thereof;

FIG. 15 is a bottom plan view thereof;

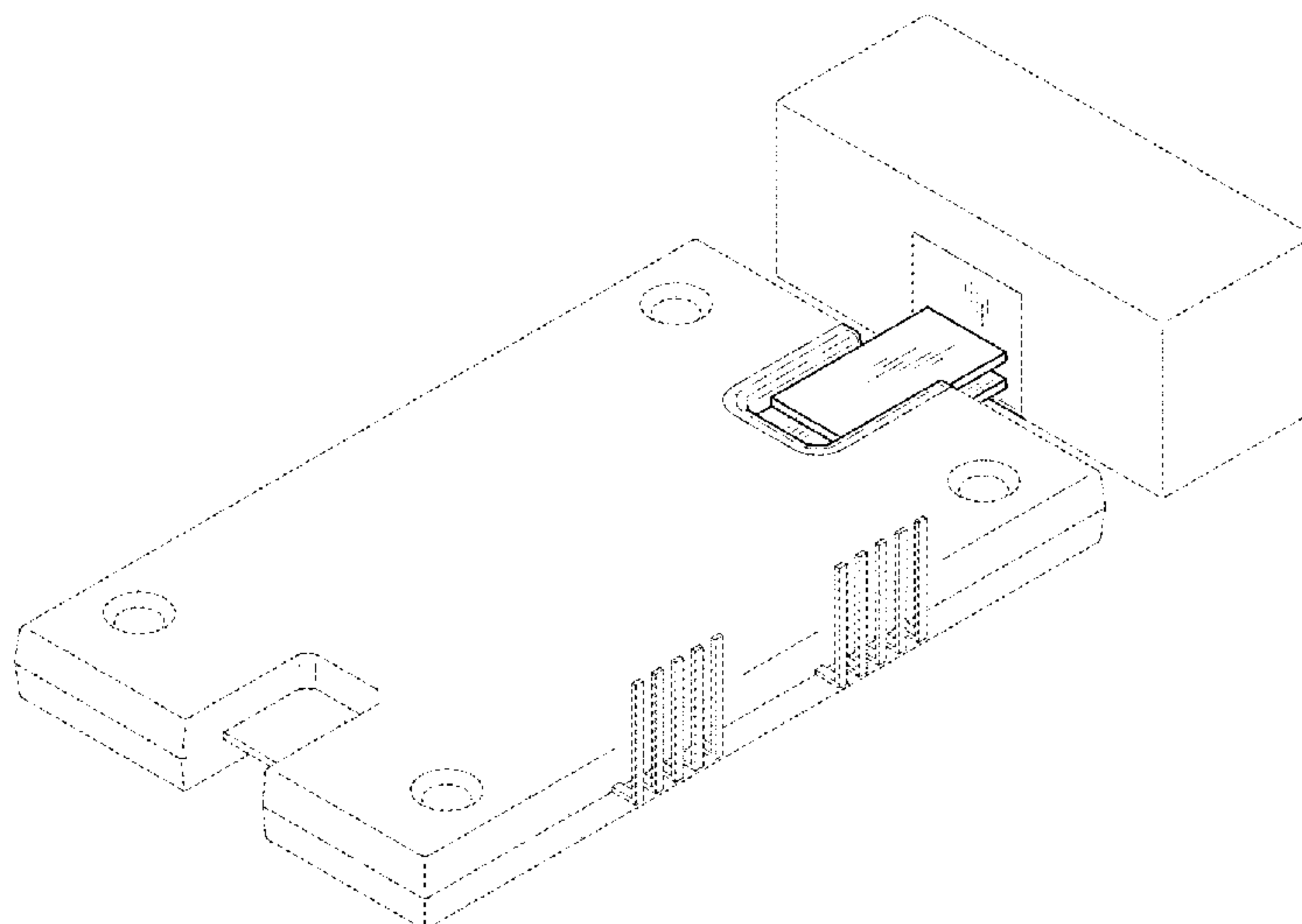
FIG. 16 is a left side view thereof;

FIG. 17 is an enlarged cross-sectional view at the portion of 17-17 taken along line 17-17 in FIG. 14; and,

FIG. 18 is an enlarged cross-sectional view taken along line 18-18 in FIG. 14.

The broken lines illustrate portions of the semiconductor module and form no part of the claimed design. The dash-dotted lines denote the boundary of the claim and form no part of the claimed design.

1 Claim, 18 Drawing Sheets



(58) Field of Classification Search

CPC H01L 21/02428; H01L 21/0243; H01L 21/02494; H01L 21/02496; H01L 21/02499; H01L 21/02502; H01L 21/02505; H01L 21/02507; H01L 21/0251; H01L 21/02513; H01L 21/02587; H01L 21/0259; H01L 21/02592; H01L 21/02595; H01L 21/02598; H01L 21/02603; H01L 21/02606; H01L 23/04; H01L 23/041; H01L 23/043; H01L 23/045; H01L 23/047; H01L 23/049; H01L 23/051; H01L 23/053; H01L 23/055; H01L 23/057; H01L 23/06; H01L 23/08; H01L 23/10; H01L 23/452; H01L 23/4922; H01L 29/02; H01L 29/04; H01L 29/045; H01L 29/06; H01L 29/0603; H01L 29/0657; H01L 29/0665; H01L 29/0684

See application file for complete search history.

(56)

References Cited

U.S. PATENT DOCUMENTS

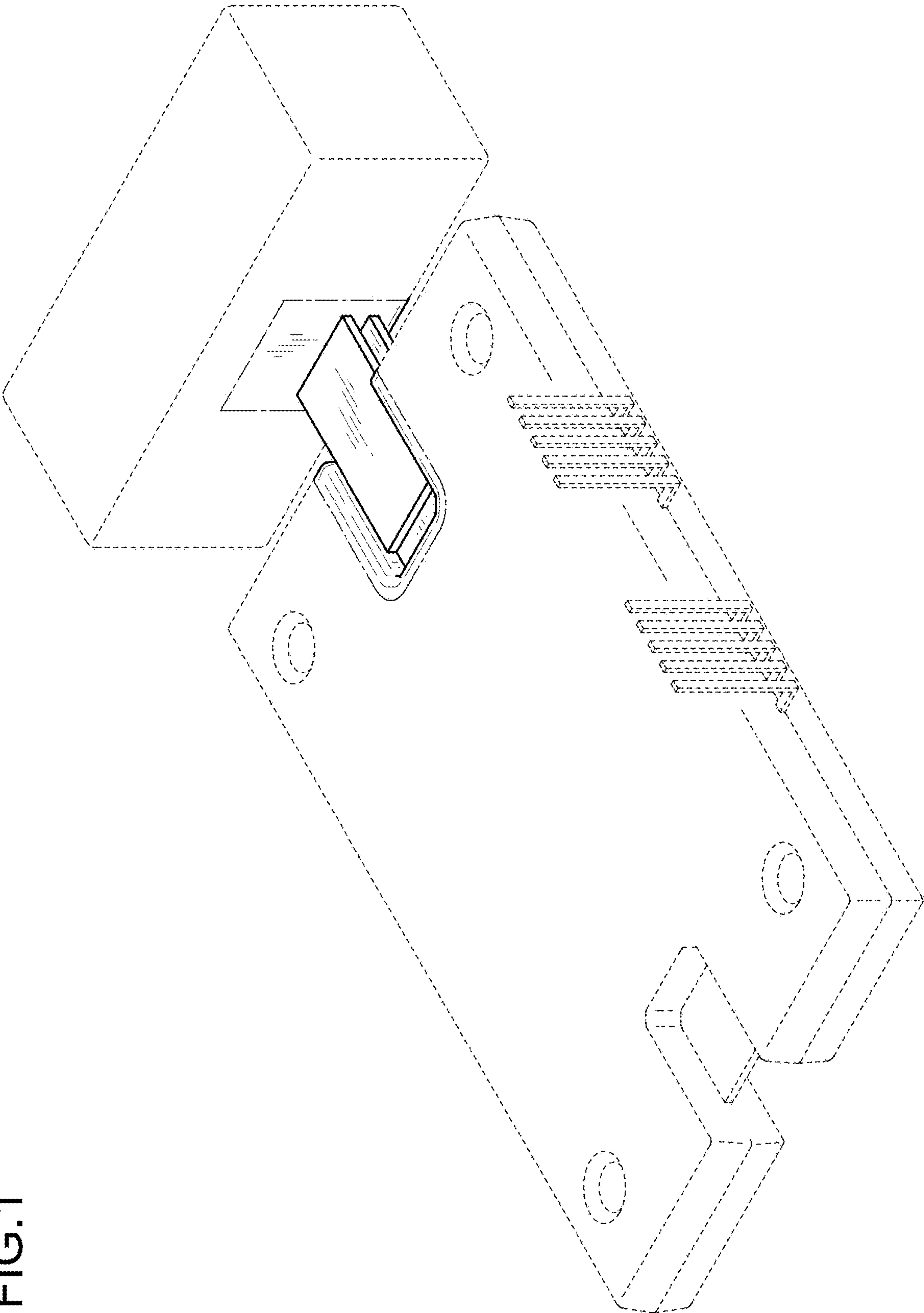
D705,184	S	*	5/2014	Takahashi		D13/182
D717,253	S	*	11/2014	Jo		D13/182
D717,254	S	*	11/2014	Jo		D13/182
D717,255	S	*	11/2014	Lim		D13/182
D717,256	S	*	11/2014	Sohn		D13/182
D719,113	S	*	12/2014	Sohn		D13/182
D719,537	S	*	12/2014	Kawase		D13/182
D719,926	S	*	12/2014	Sohn		D13/182

FOREIGN PATENT DOCUMENTS

JP	1146362	S	7/2002
JP	1146363	S	7/2002
JP	1305812	S	7/2007
JP	1551590	S	6/2016
JP	1565636	S	12/2016
JP	1578687	S	6/2017

* cited by examiner

FIG.1



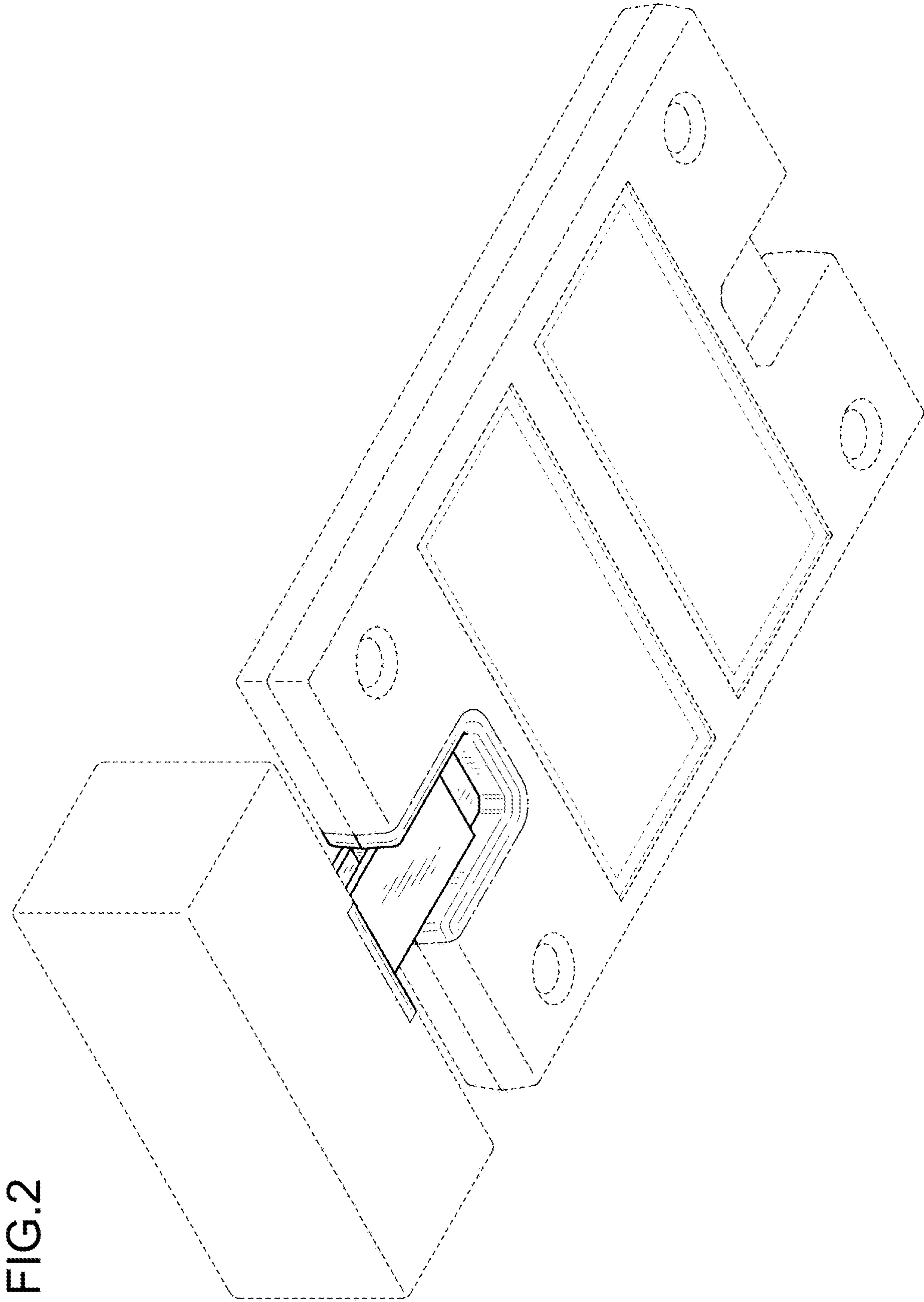


FIG.2

FIG.3

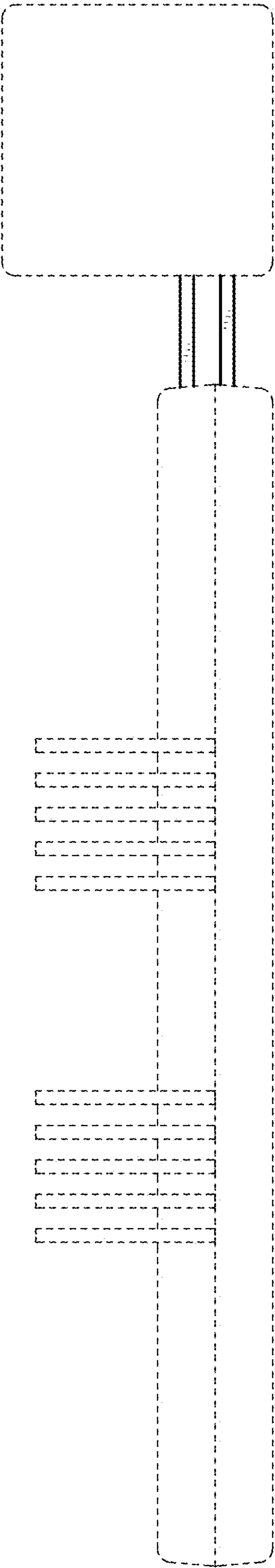
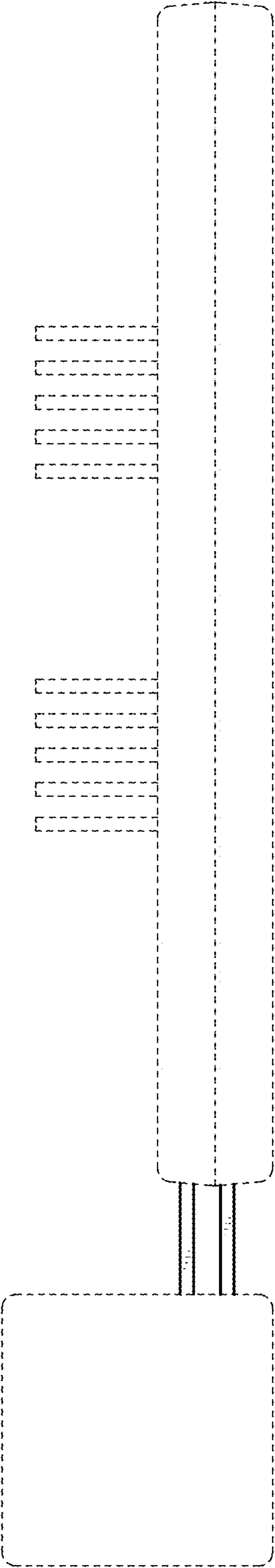


FIG.4



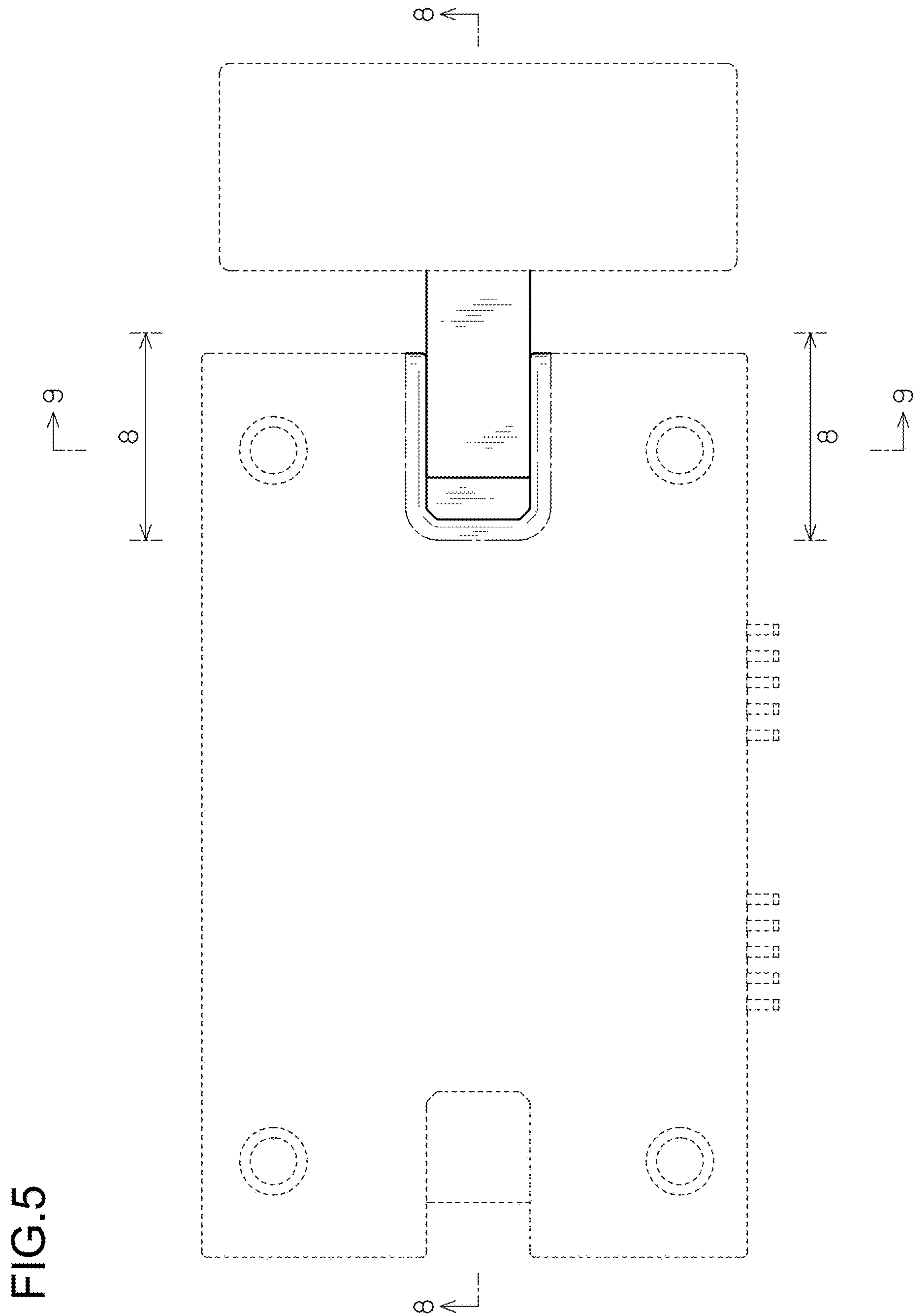


FIG.6

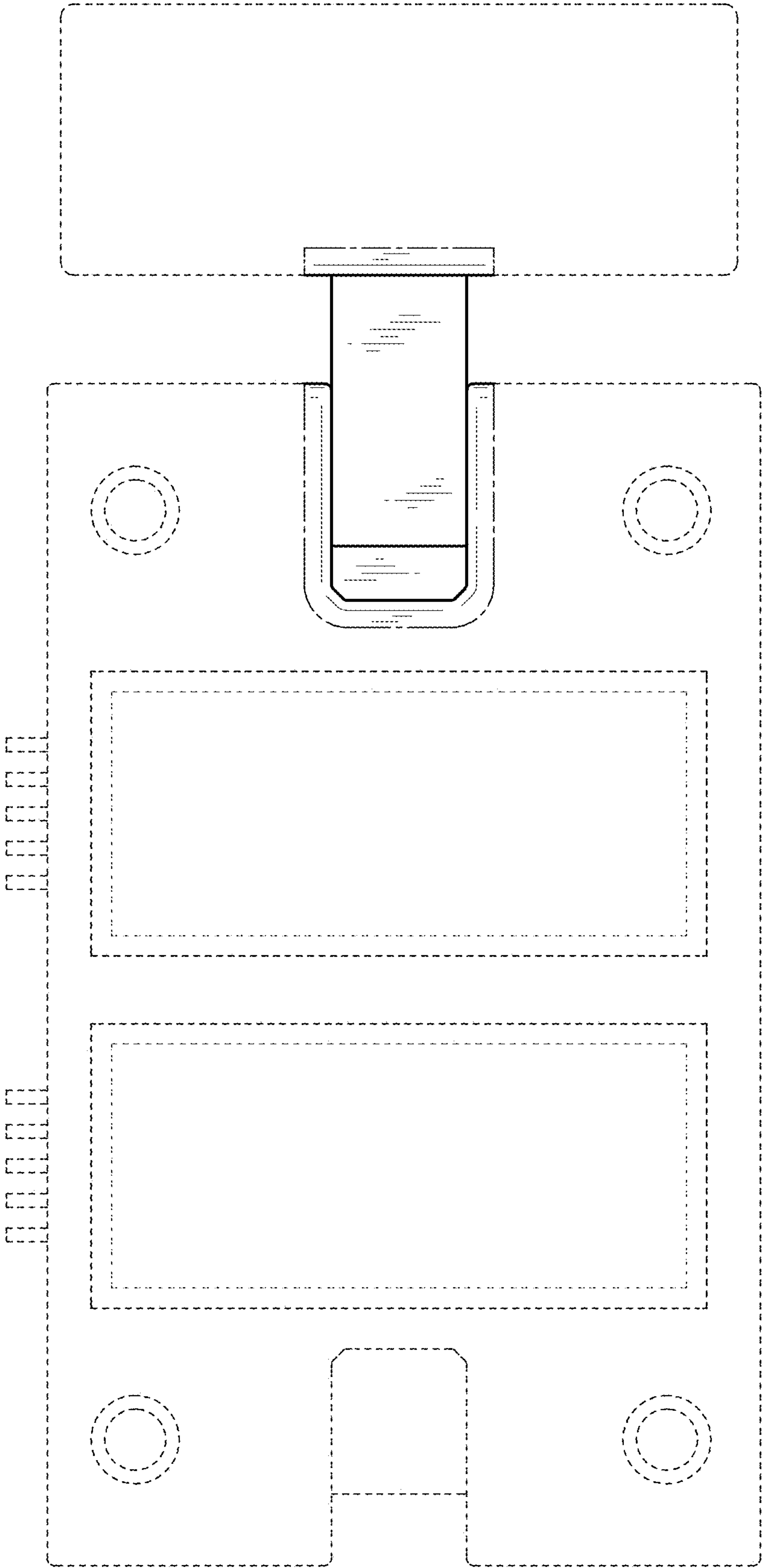
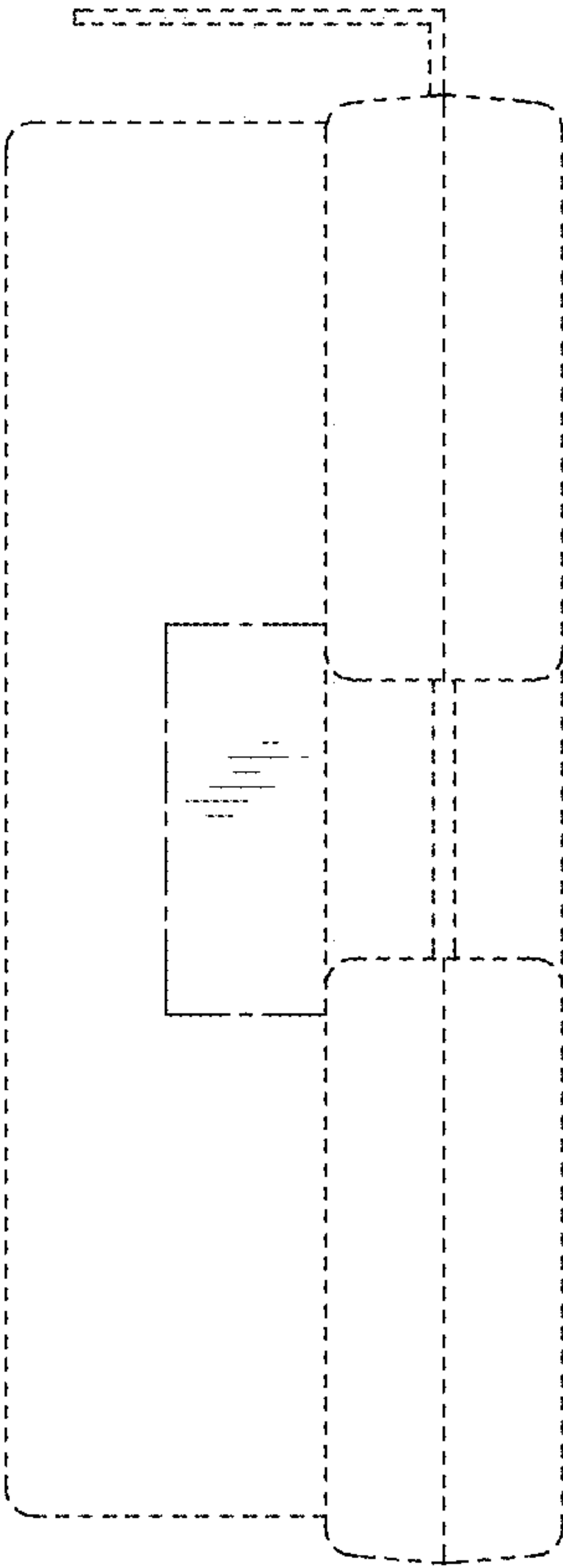


FIG.7



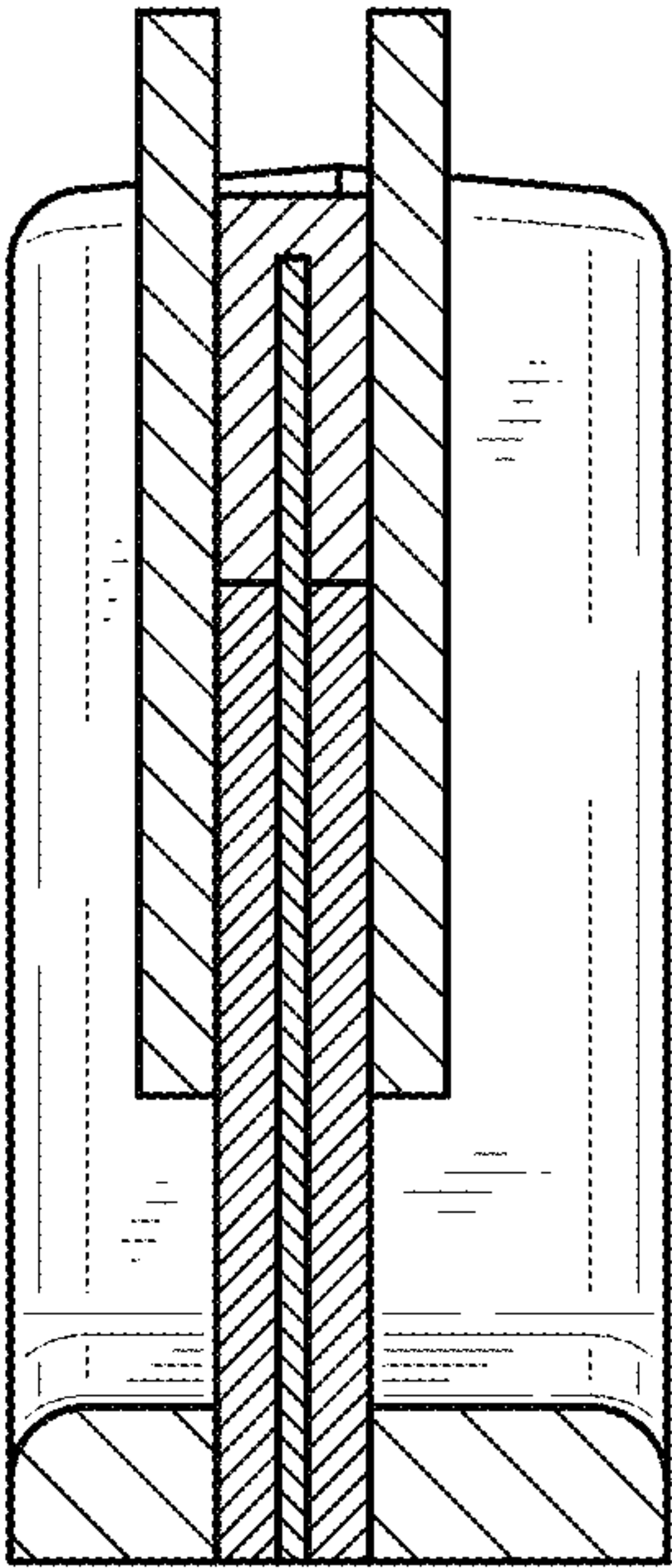


FIG.8

FIG.9

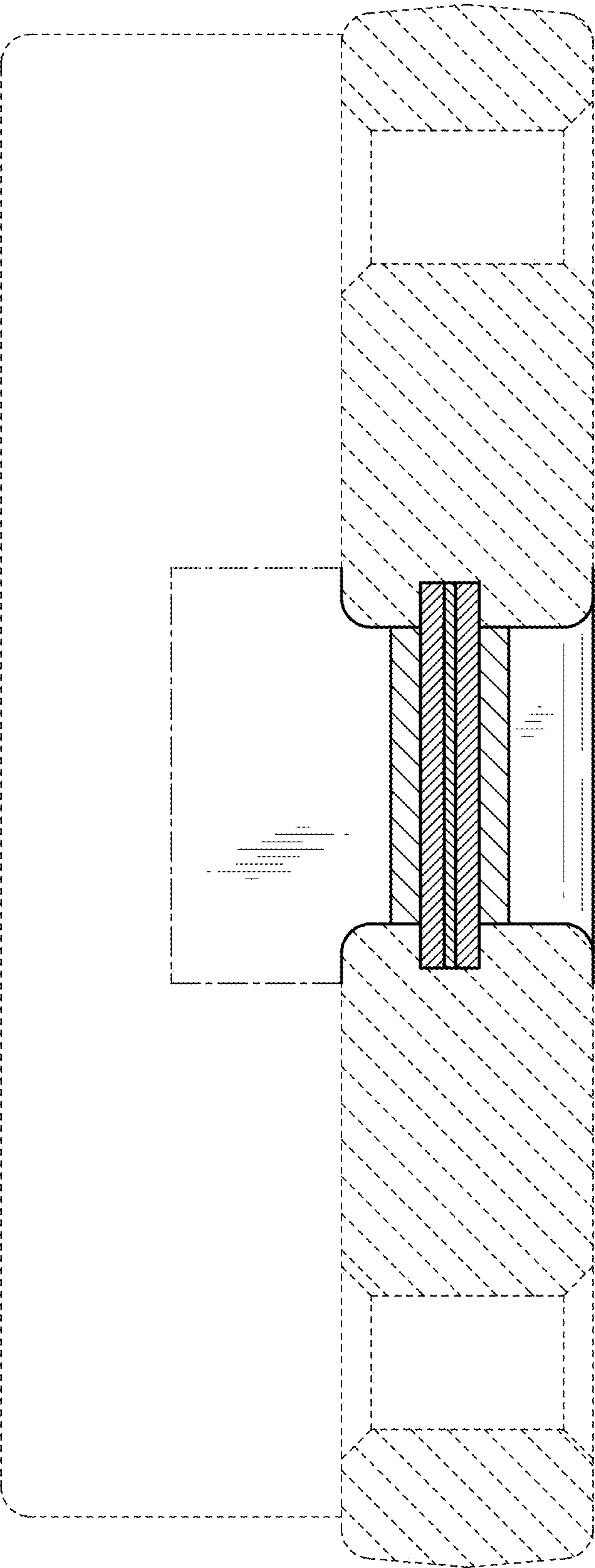


FIG.10

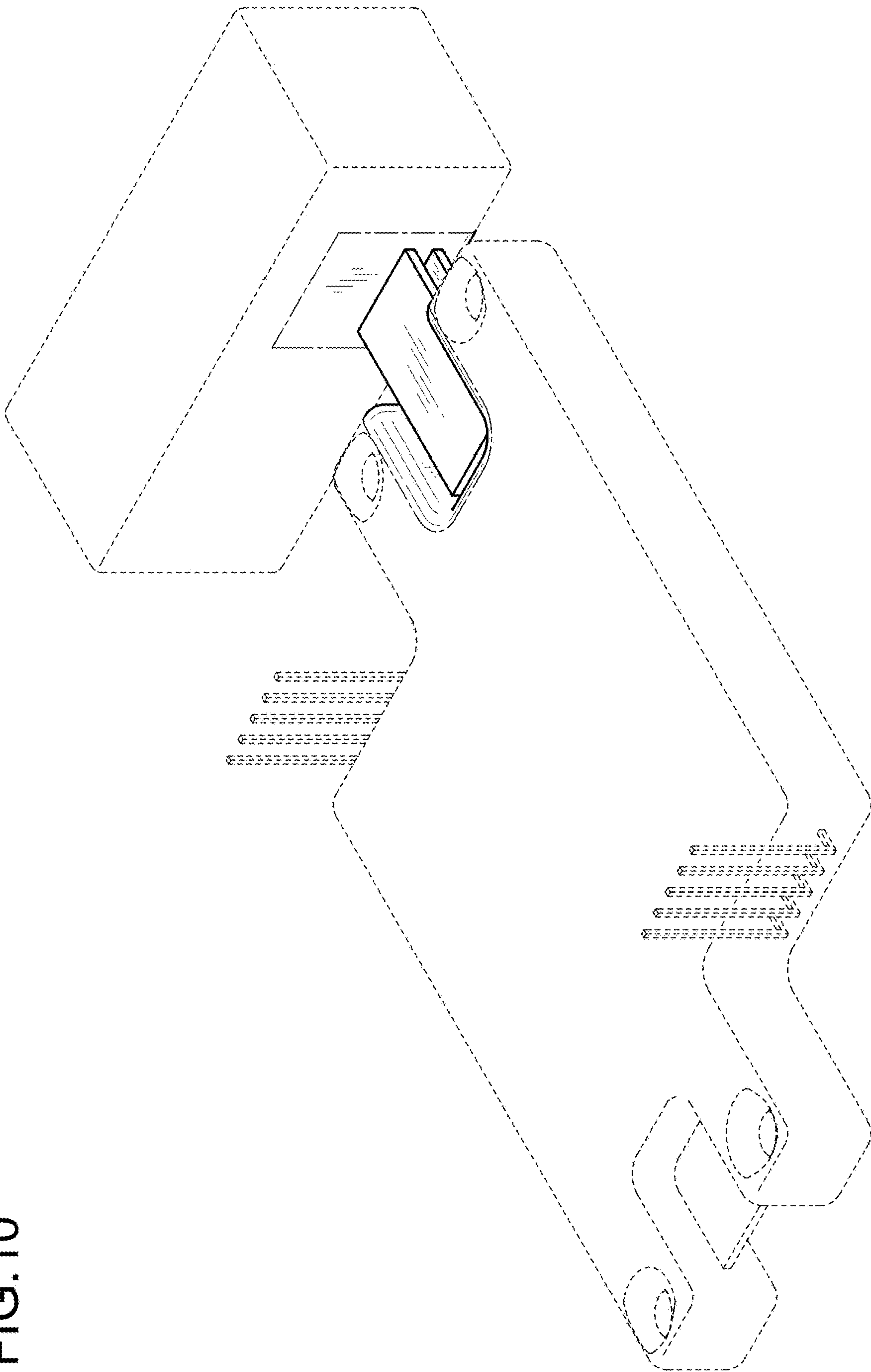


FIG.11

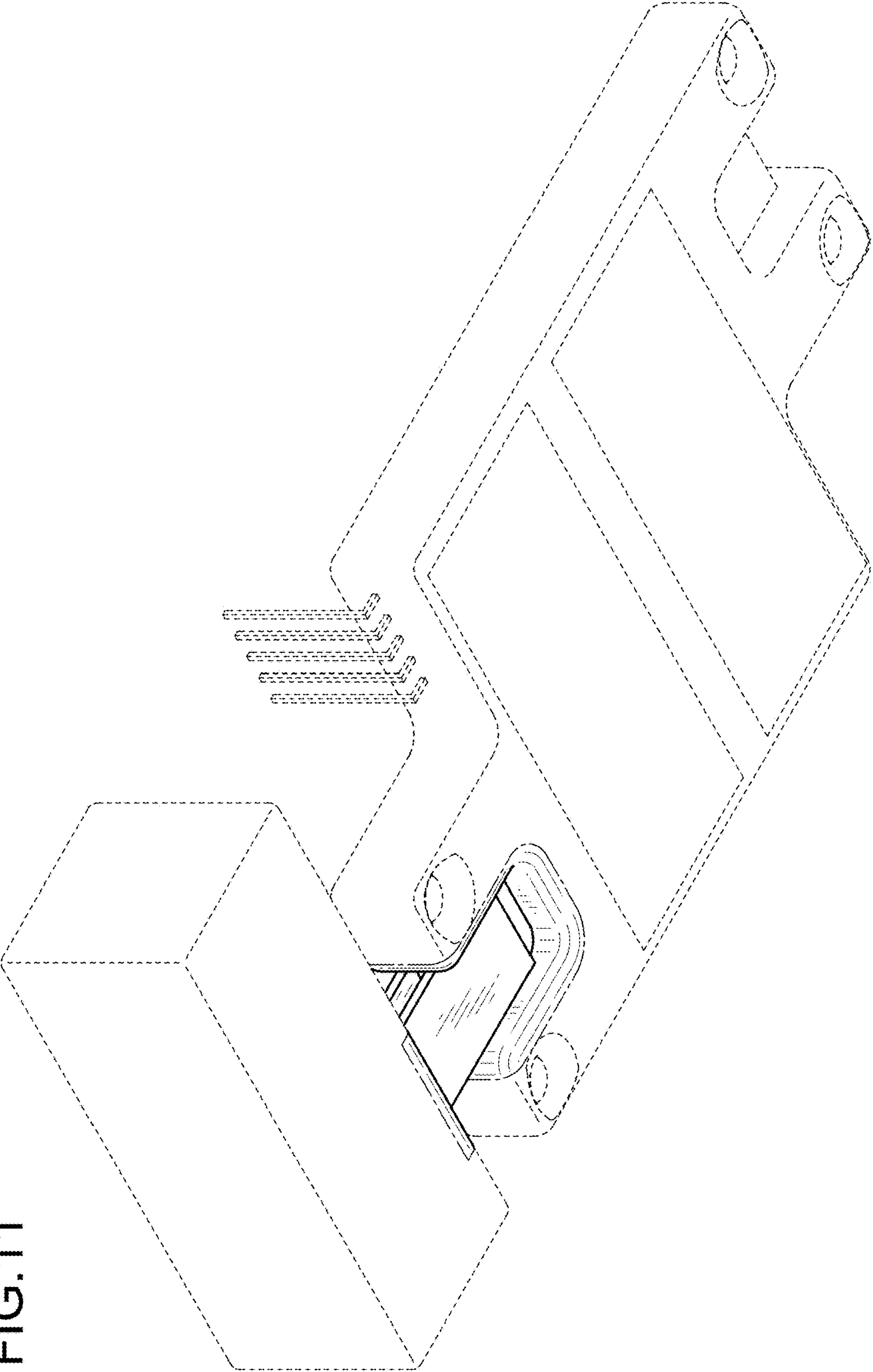


FIG.12

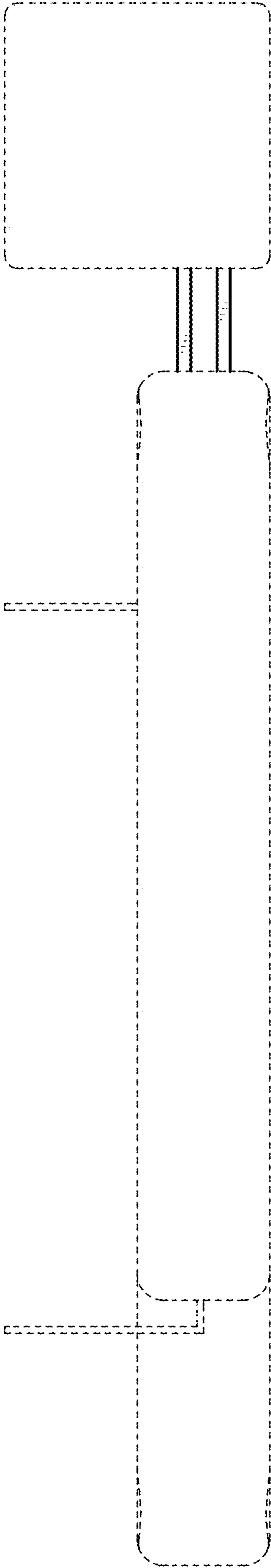


FIG.13

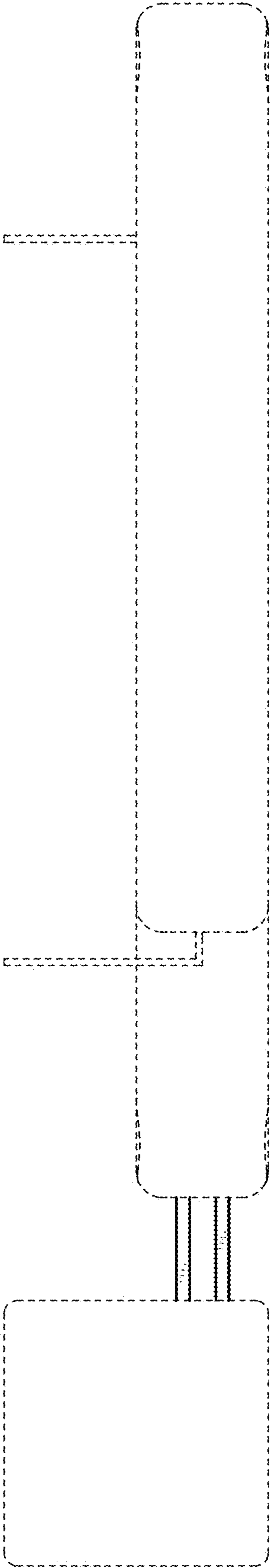


FIG.14

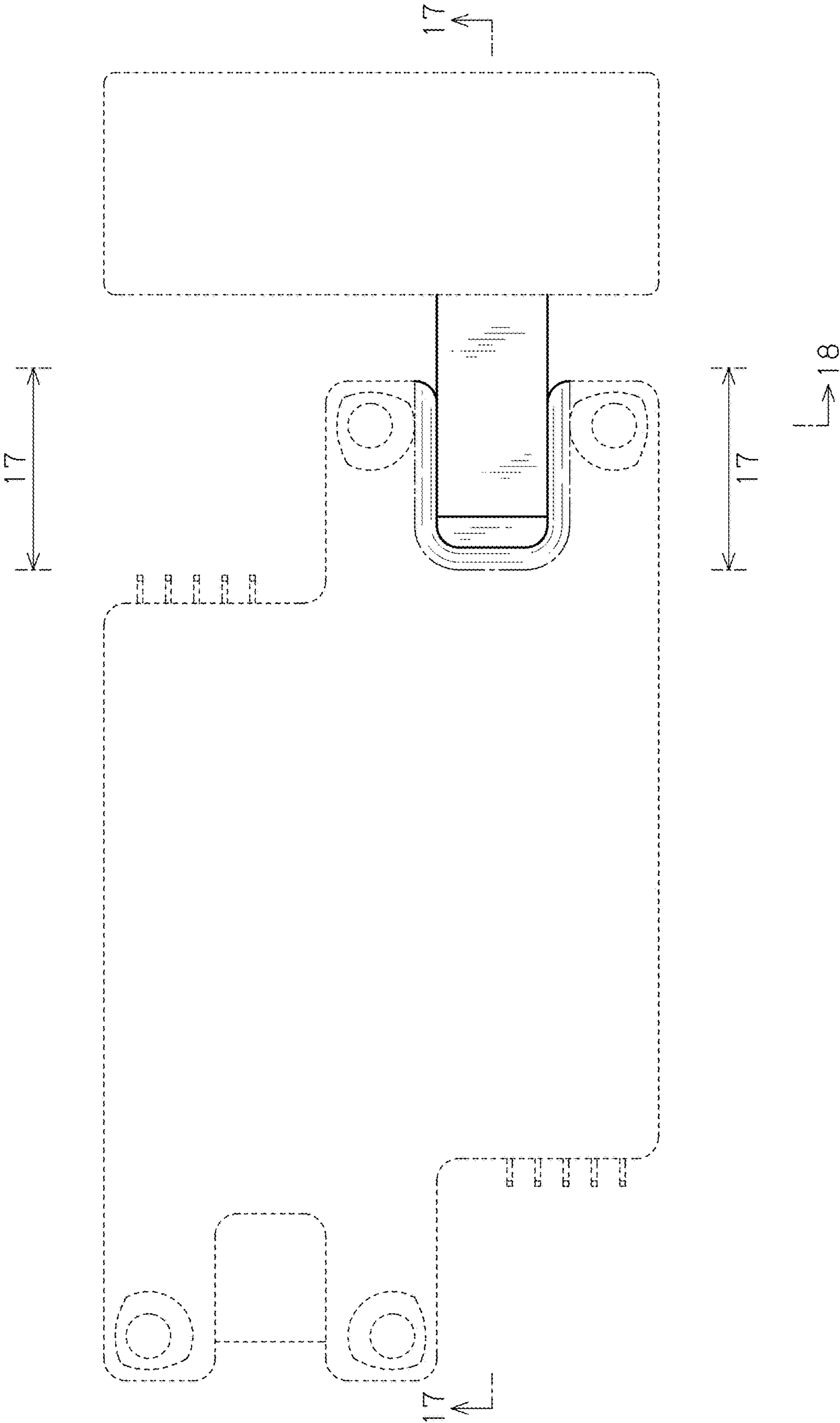


FIG.15

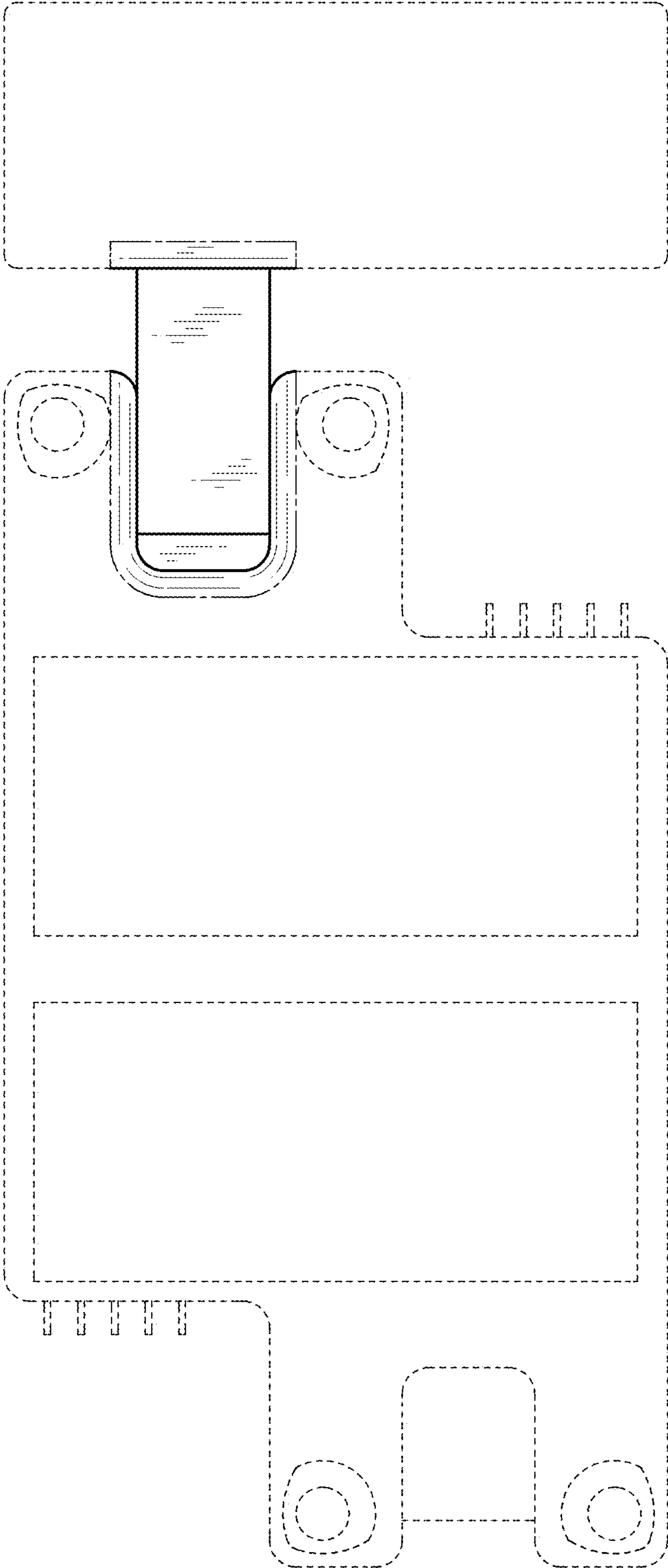
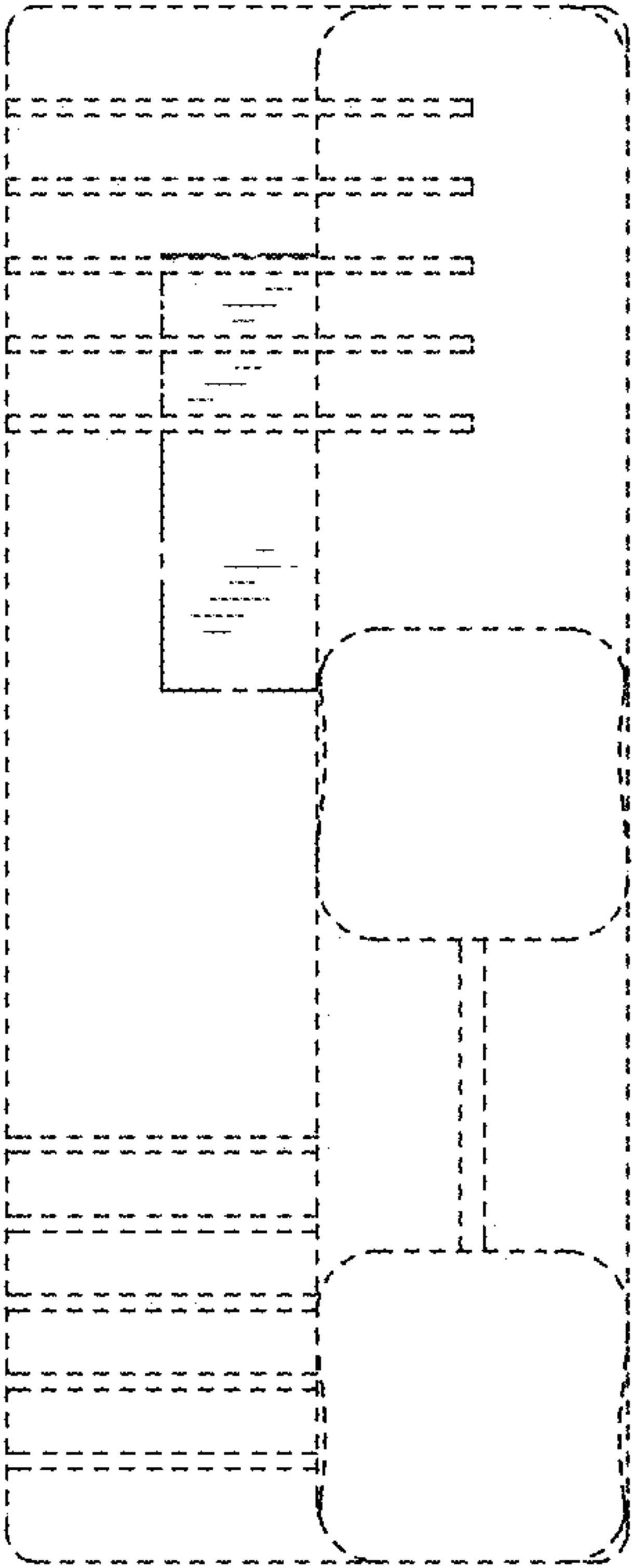


FIG.16



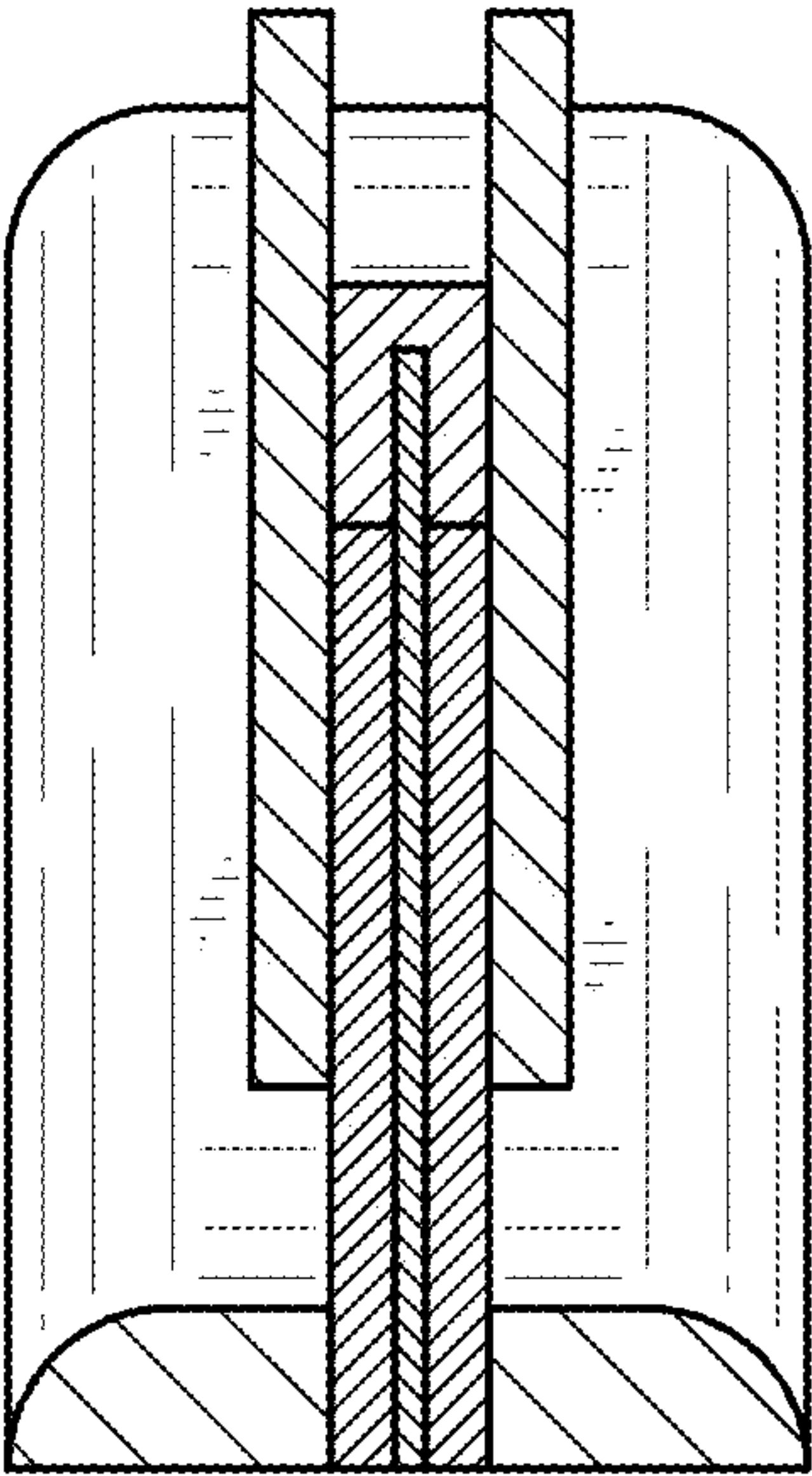


FIG.17

FIG.18

