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(12) **United States Design Patent**
Karasawa

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(45) **Date of Patent: ** Nov. 26, 2019**

(54) **CASSETTE RECEIVING TOOL FOR SEMICONDUCTOR MANUFACTURING APPARATUS**

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(73) Assignee: **KOKUSAI ELECTRIC CORPORATION**, Tokyo (JP)

(**) Term: **15 Years**

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(22) Filed: **Jul. 17, 2017**

(30) **Foreign Application Priority Data**

Jan. 18, 2017 (JP) 2017-000730

(51) **LOC (12) Cl.** **13-03**
(52) **U.S. Cl.**
USPC **D13/182**
(58) **Field of Classification Search**
USPC .... D13/182, 184, 199; D15/144, 144.1, D15/199, 140; 294/1.1, 2, 6, 12, 15, 16, 294/26–34, 49, 55.5, 87.1; 16/114 R; 118/500, 503, 728; 206/328, 334, 445, 206/454; 414/416, 217, 940, 331, 935, 414/939; 451/364; 269/903; 248/694
CPC B65G 49/07; H01L 21/673; H01L 21/67; H01L 21/67353; H01L 21/67769; H01L 21/67775; H01L 21/67379; H01L 23/32; B65D 25/28
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,947,675 A * 9/1999 Matsushima H01L 21/67775 414/416.08
5,947,677 A * 9/1999 Matsushima H01L 21/67769 414/609
6,152,680 A * 11/2000 Howells H01L 21/6732 414/781
6,270,307 B1 * 8/2001 Sinha H01L 21/67313 198/394
6,595,841 B2 * 7/2003 Lai B24B 37/345 248/694
D665,759 S * 8/2012 Sato D13/199
D674,365 S * 1/2013 Kajiwara D13/182
D695,240 S * 12/2013 Iida D13/182
(Continued)

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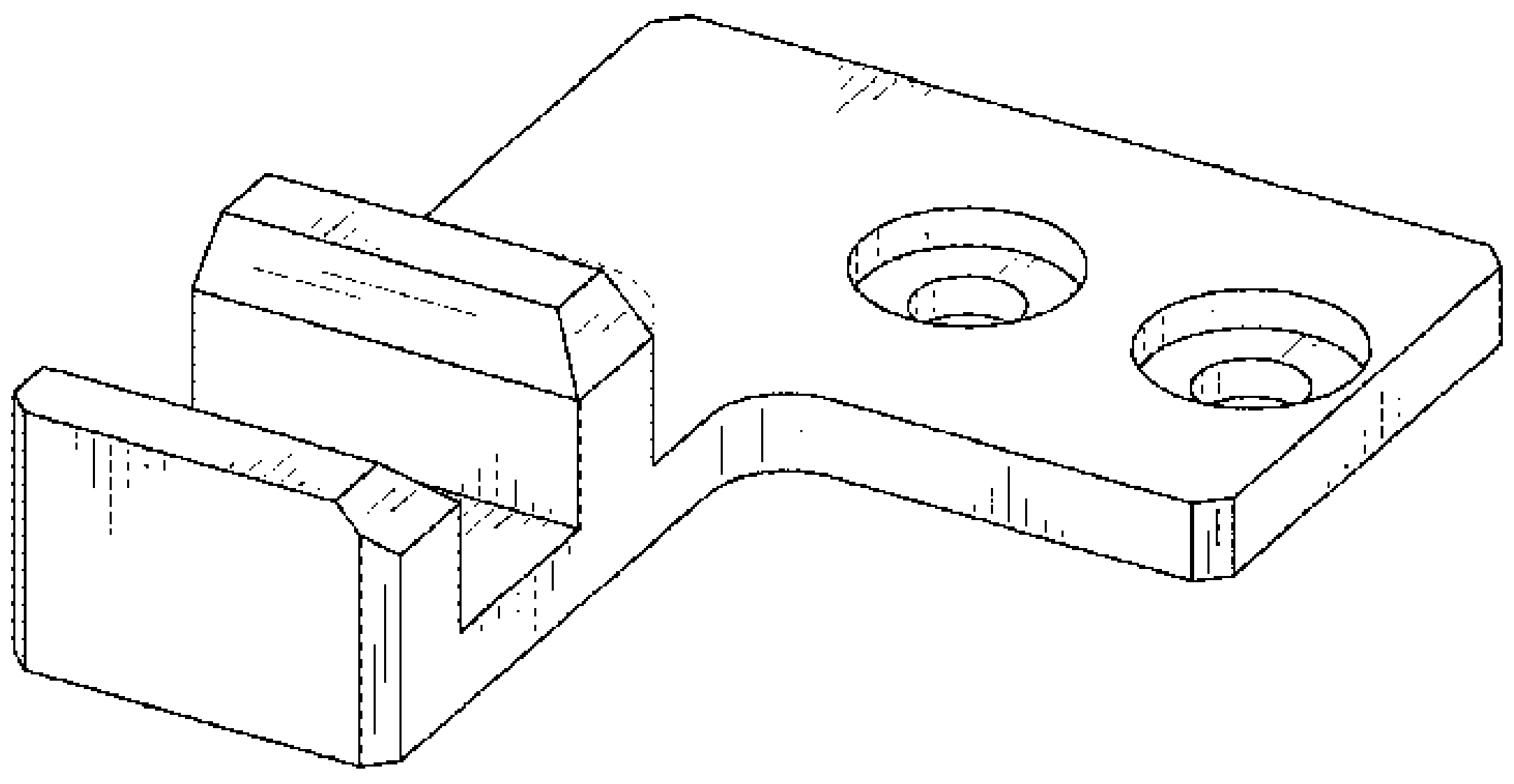
(57) **CLAIM**

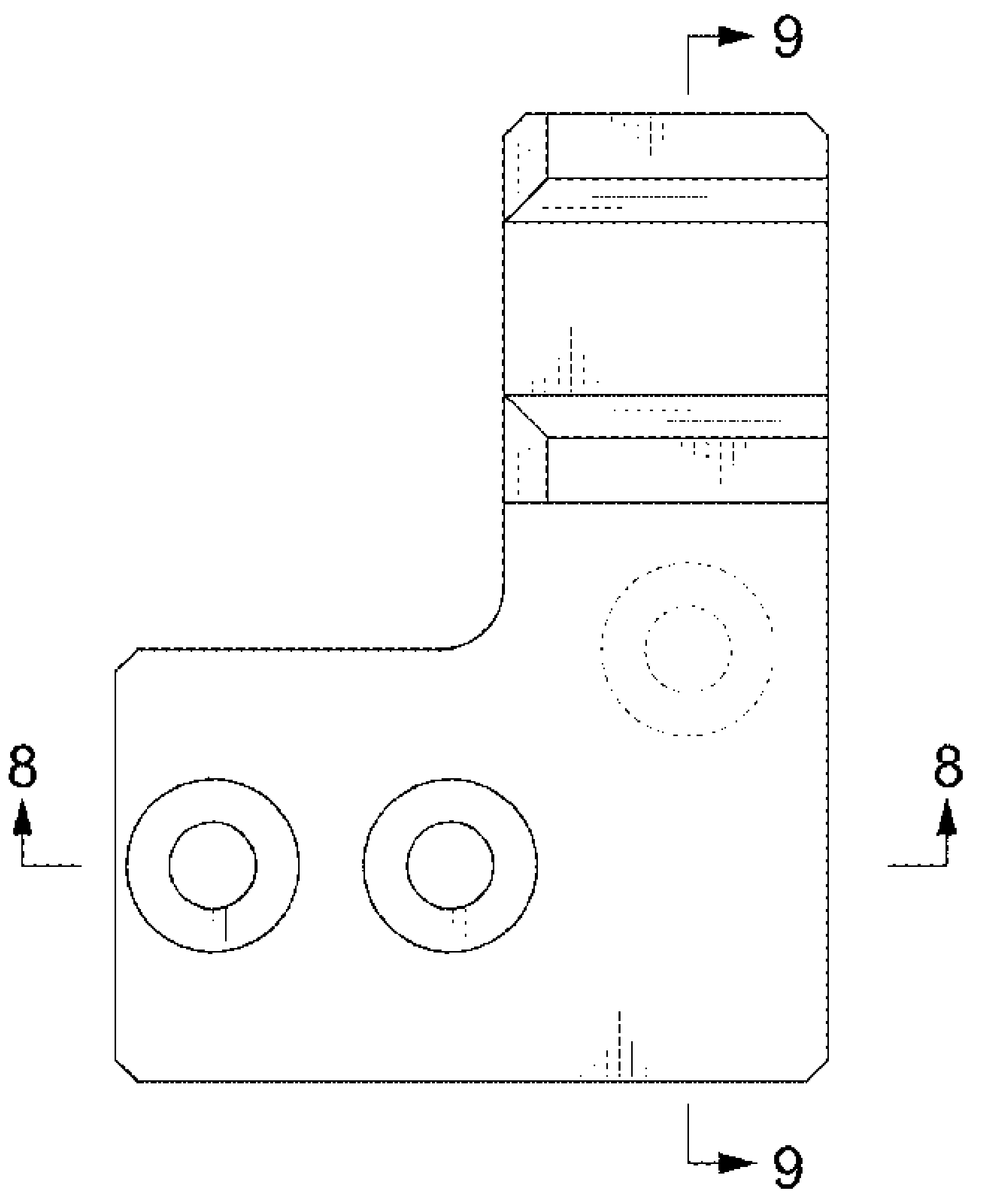
The ornamental design for a cassette receiving tool for semiconductor manufacturing apparatus, as shown and described.

DESCRIPTION

FIG. **1** is a front, top, and left side perspective view of a cassette receiving tool for semiconductor manufacturing apparatus, showing my new design;
FIG. **2** is a front elevational view thereof;
FIG. **3** is a rear elevational view thereof;
FIG. **4** is a left side elevational view thereof;
FIG. **5** is a right side elevational view thereof;
FIG. **6** is a top plan view thereof;
FIG. **7** is a bottom plan view thereof;
FIG. **8** is a cross sectional view taken along line **8-8** in FIG. **2**; and,
FIG. **9** is a cross sectional view taken along line **9-9** in FIG. **2**.
The broken lines shown in the drawings represent portions of the cassette receiving tool for semiconductor manufacturing apparatus that form no part of the claimed design.

1 Claim, 3 Drawing Sheets





(56) References Cited

U.S. PATENT DOCUMENTS

D701,498 S * 3/2014 Iida D13/182
8,676,375 B2 * 3/2014 Kraus H01L 21/67259
700/213

* cited by examiner

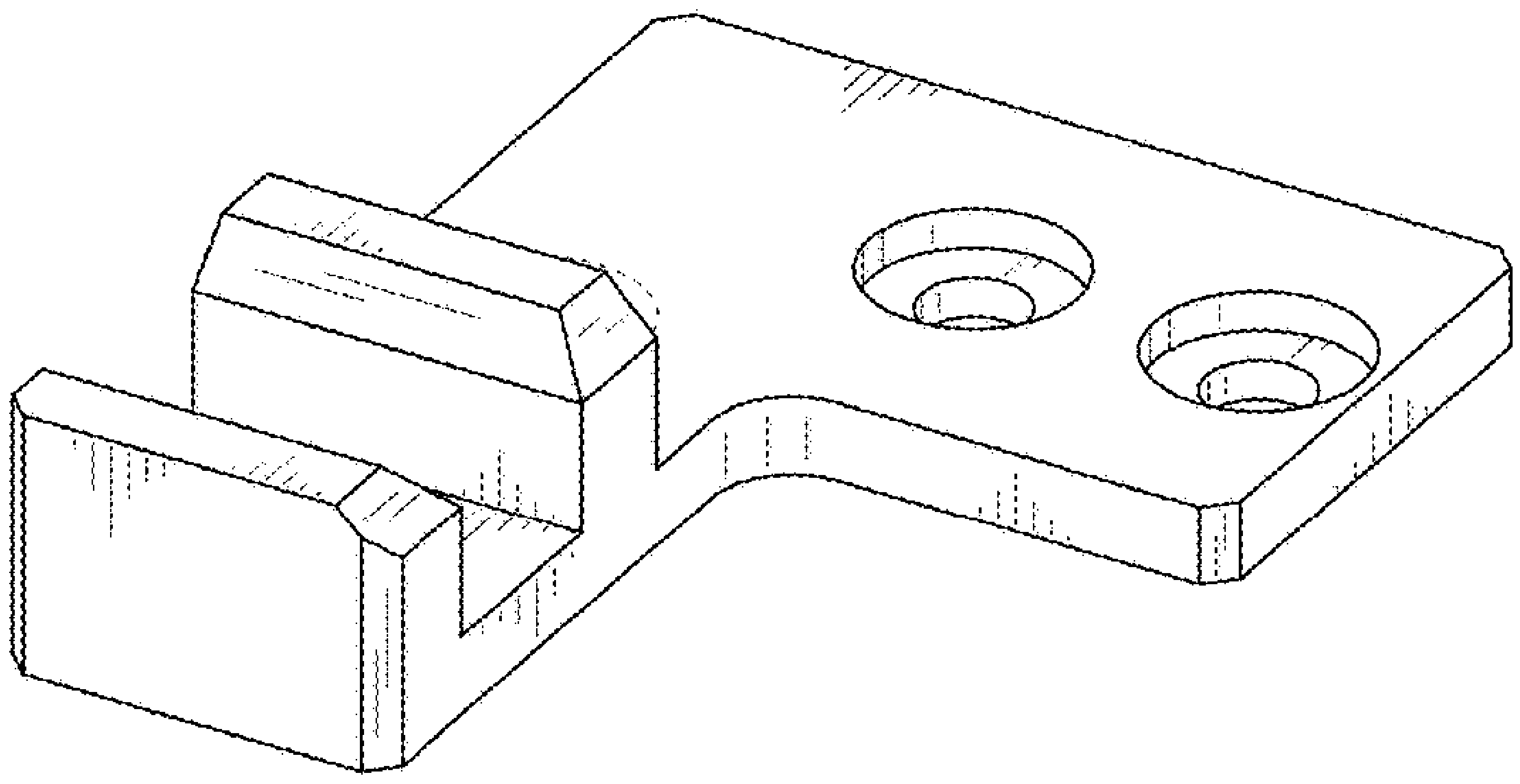


FIG. 1

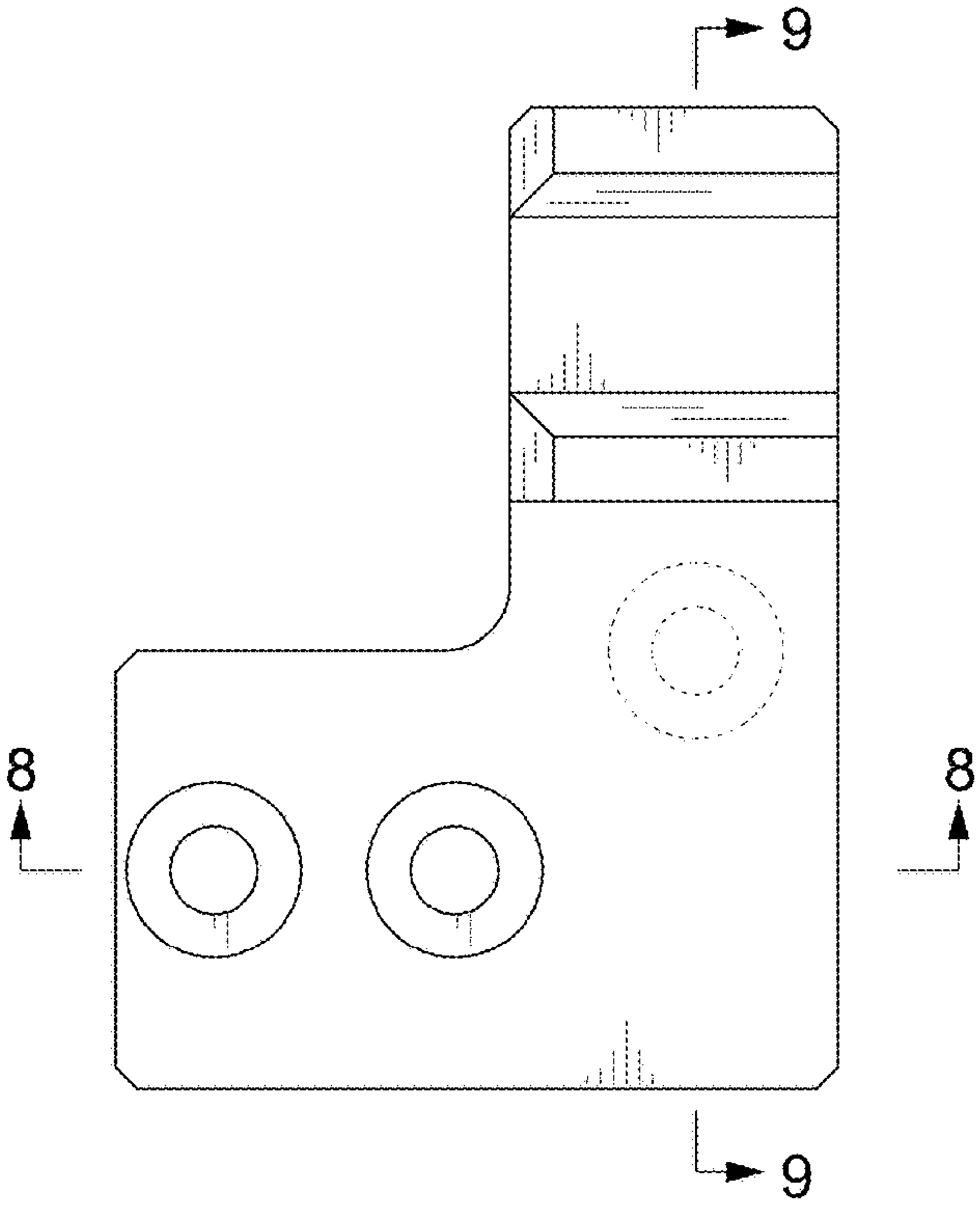


FIG. 2

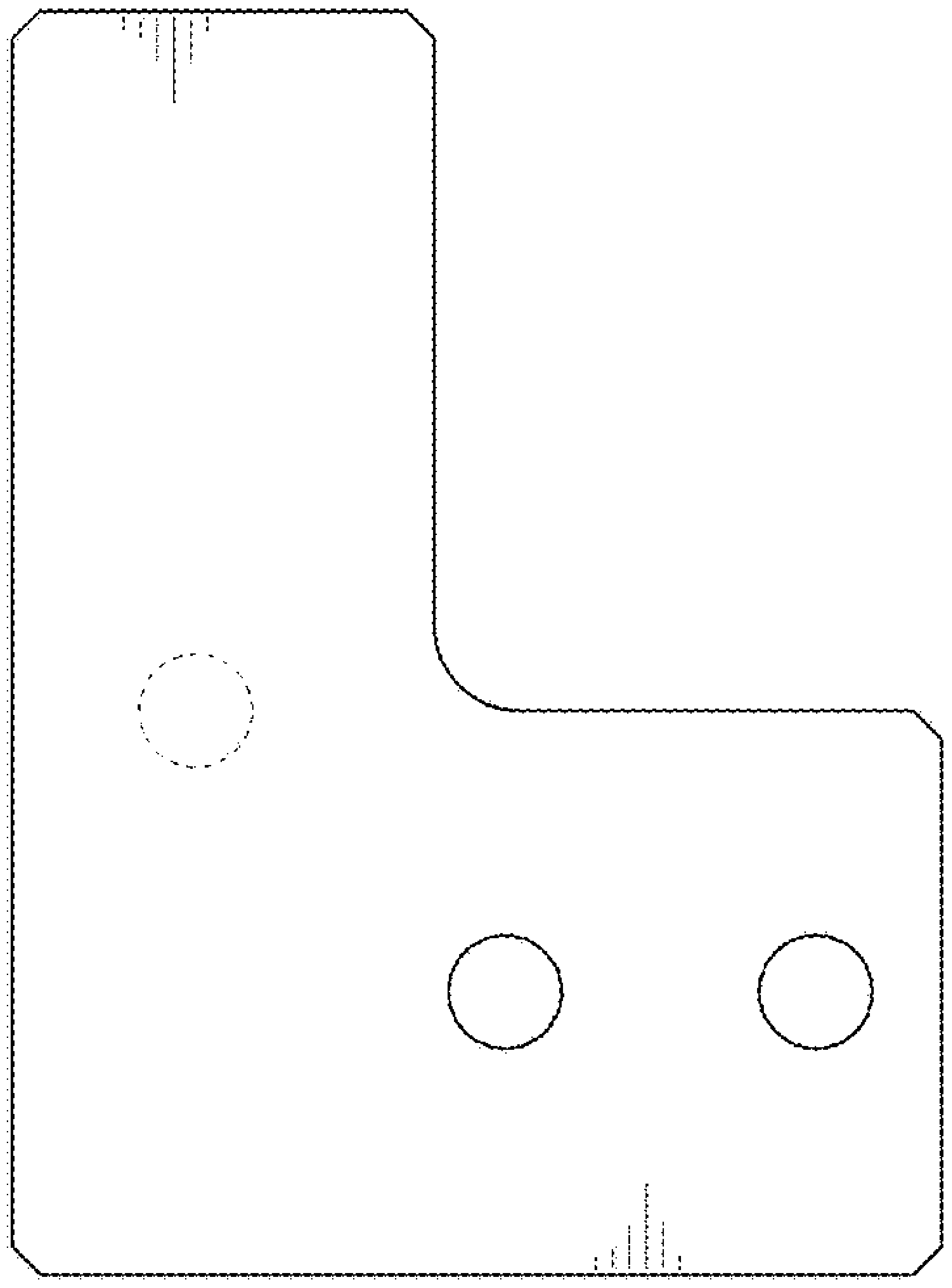


FIG. 3

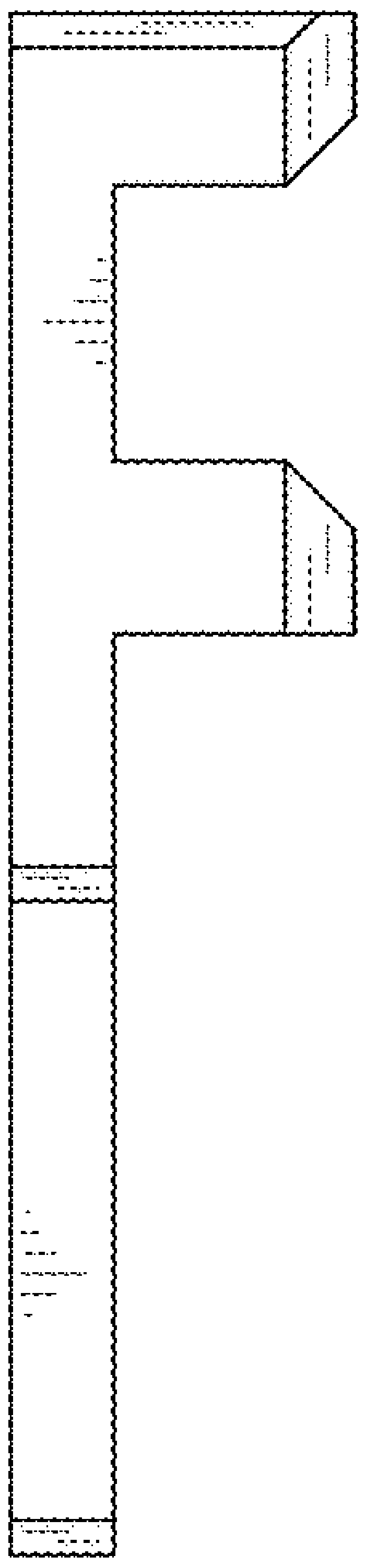


FIG. 4

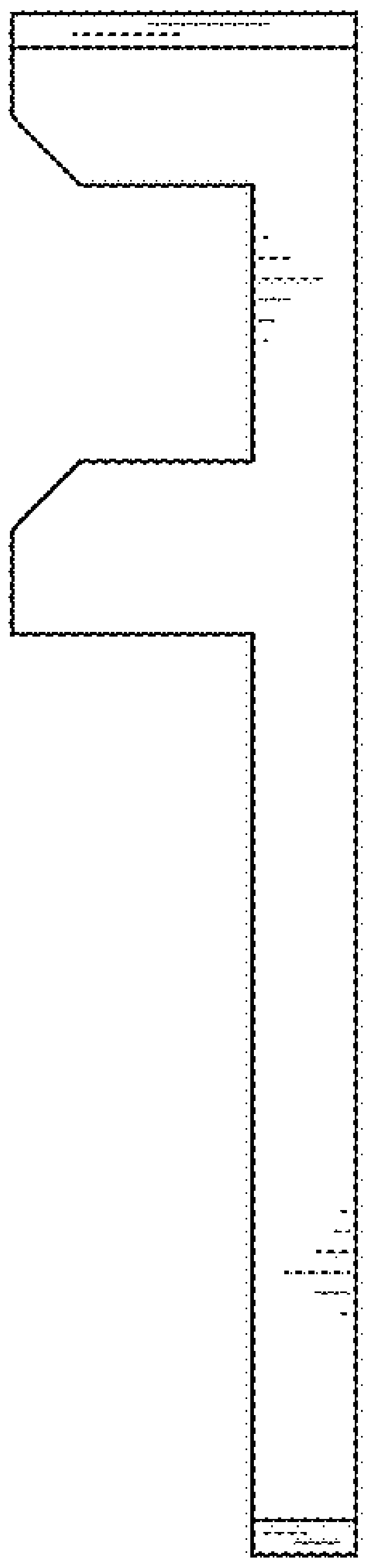


FIG. 5

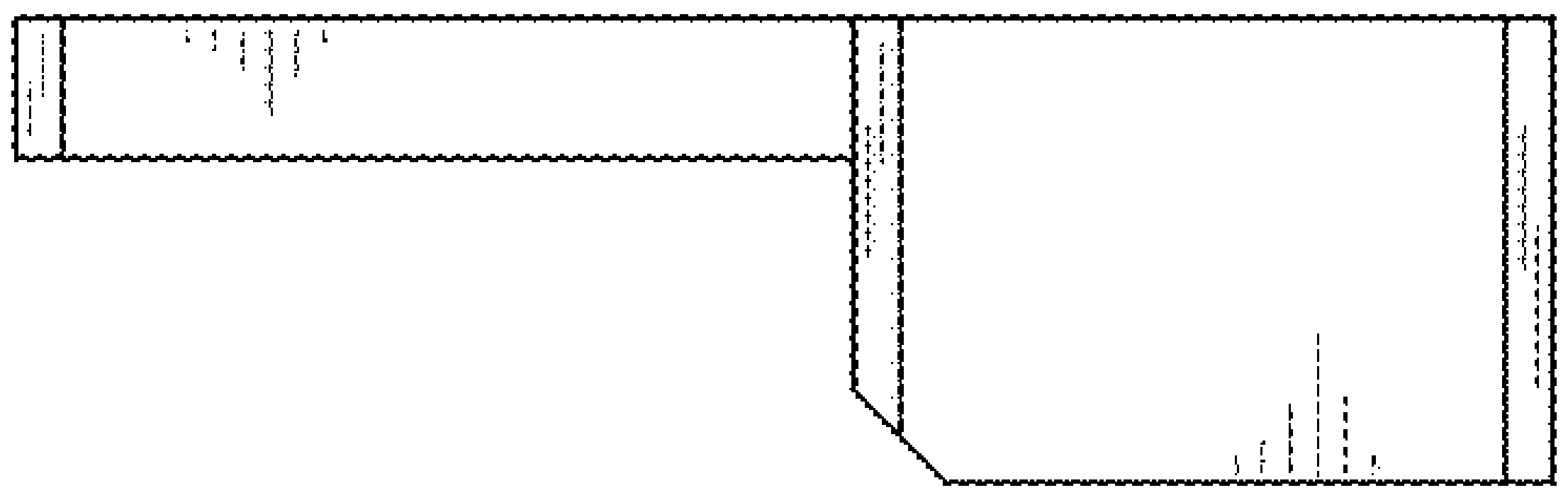


FIG. 6

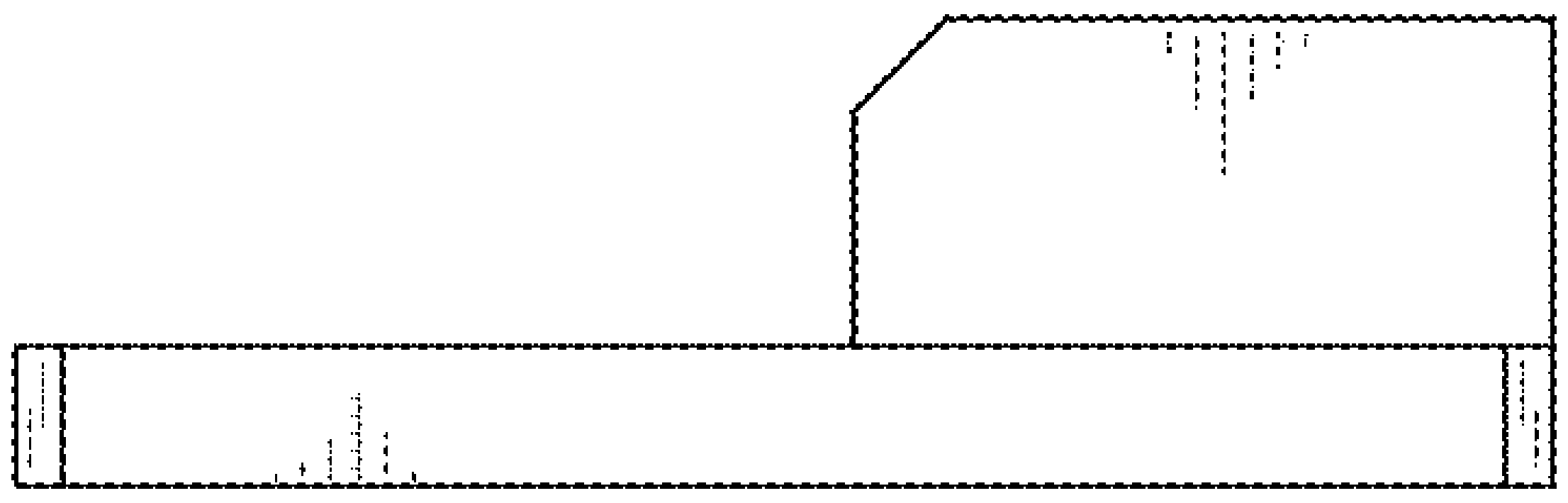


FIG. 7

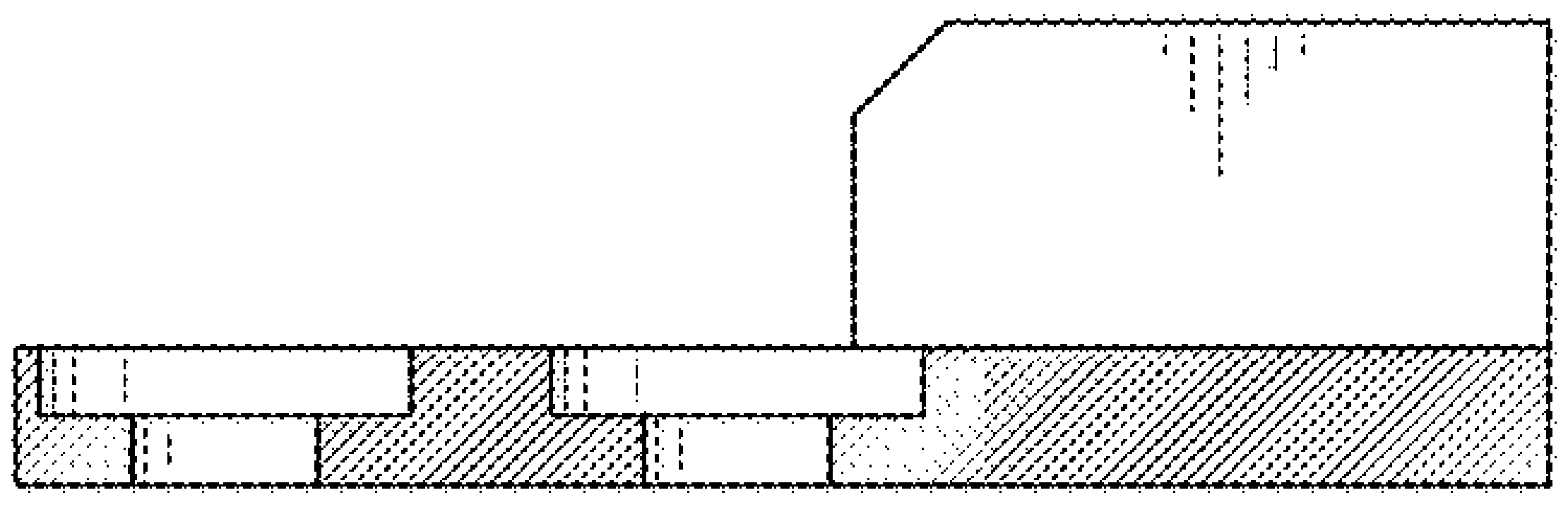


FIG. 8

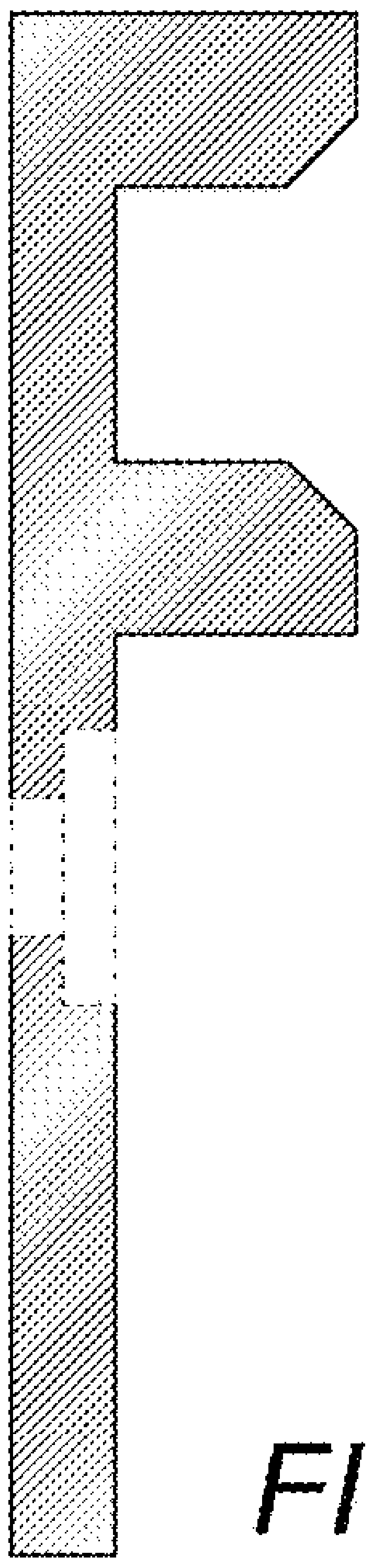


FIG. 9