



US00D864951S

(12) **United States Design Patent** (10) **Patent No.:** **US D864,951 S**
Ranade (45) **Date of Patent:** **** Oct. 29, 2019**

(54) **ELECTRONICS MODULE**

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(73) Assignee: **Intel Corporation**, Santa Clara, CA (US)

(**) Term: **15 Years**

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(51) **LOC (12) Cl.** **14-02**

(52) **U.S. Cl.**
USPC **D14/341; D14/344; D14/300; D14/432; D14/435**

(58) **Field of Classification Search**

USPC D14/341, 344, 300, 314, 315, 345, 348, D14/353, 357, 358, 359, 363, 383, 412, D14/420, 433, 434, 435-438, 478-480, D14/496, 507, 509, 511, 313, 356, 367, D14/370, 385, 388, 432, 439, 445, 474, D14/483, 140, 144, 168, 172, 203.1, D14/203.3, 203.5, 204; 235/441, 443, 235/487, 492, 493, 495; 361/737, 679, 361/752, 736, 728, 796, 797, 729, 730, 361/725-727, 679.59, 679.31, 679.32, 361/679.33, 679.03, 679.26, 679.3, 679.4, 361/679.41, 679.55, 679.56, 733, 734; 257/678, 679, 693, E23.064; 439/946, 439/948, 159; 174/250, 260, 52.1, 52.2; 710/300-303; 438/121; D13/110, 103, D13/146; 312/223.2; D24/185, 186; 379/428.01, 428.04, 419; 455/569.1, 455/575.6; D21/324, 330, 332, 333, 386, D21/436, 404, 411, 437, 441, 443, 447, D21/451, 468, 474, 475, 478, 479, 484, D21/567, 570, 578, 579-584; D17/22;

(Continued)

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(Continued)

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(57) **CLAIM**

The ornamental design for an electronics module, as shown and described.

DESCRIPTION

FIG. 1 is a front view of an electronics module showing my new design;

FIG. 2 is a rear view of the electronics module.

FIG. 3 is a right side view of the electronics module.

FIG. 4 is a left side view of the electronics module.

FIG. 5 is a top view of the electronics module.

FIG. 6 is a bottom view of the electronics module.

FIG. 7 is a top-rear-right perspective view of the electronics module.

FIG. 8 is a bottom-rear-right perspective view of the electronics module.

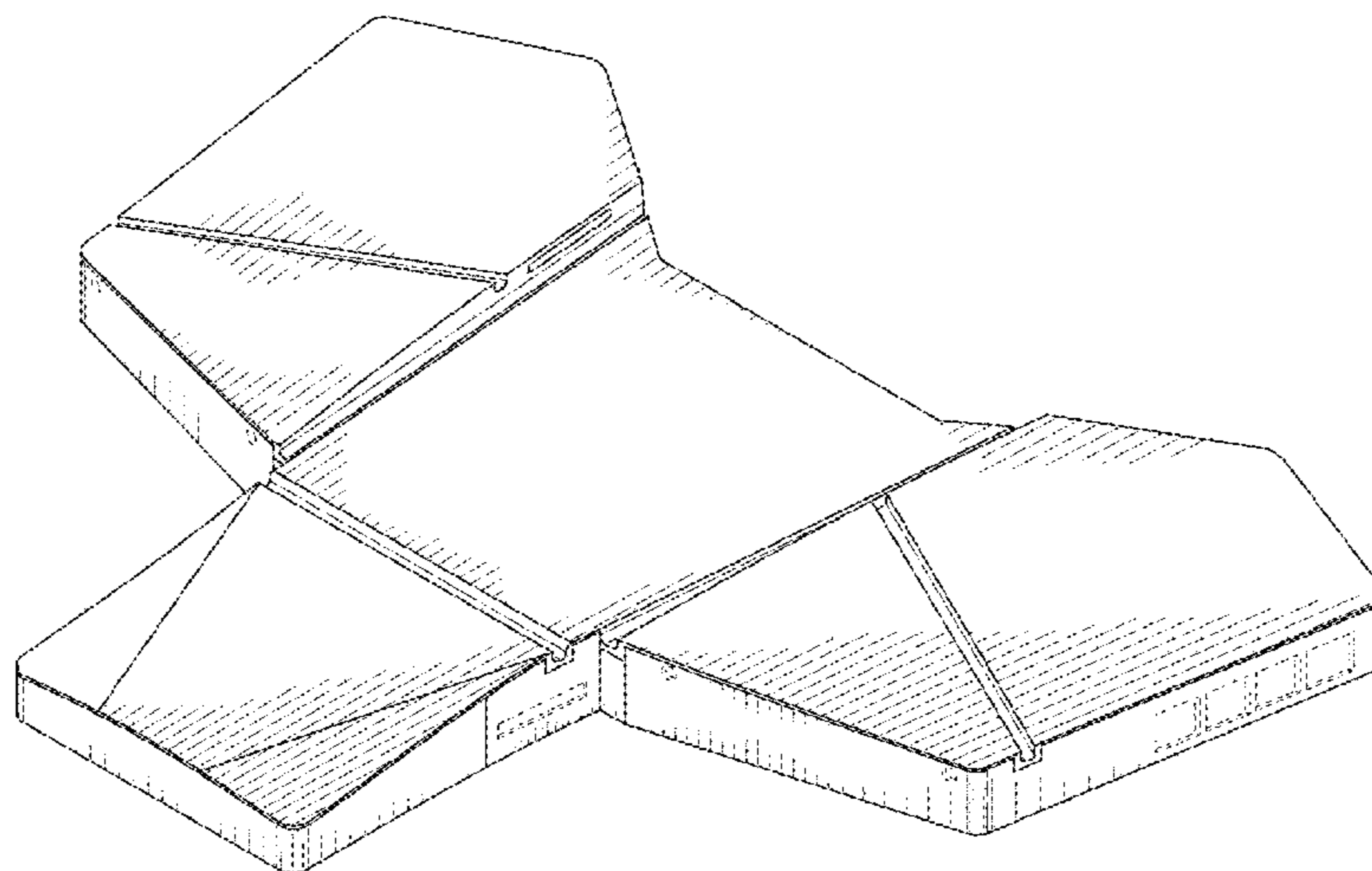
FIG. 9 is a top-rear-left perspective view of the electronics module; and,

FIG. 10 is a bottom-front-right perspective view of the electronics module.

The shade lines show surface contour and not surface ornamentation.

The broken line showing of communication ports, access panels, and openings in the exterior of the electronics module illustrates environmental structure, and the broken lines form no part of the claimed design.

1 Claim, 8 Drawing Sheets



(58) **Field of Classification Search**

USPC 446/71, 72, 80, 85, 137-139, 268, 99;
 273/153 S
 CPC G06F 1/1613; G06F 1/1622; G06F 1/1624;
 G06F 1/163; G06F 1/1632; G06F 1/1633;
 G06F 1/1635; G06F 1/1656; G06F
 1/1658; G06F 1/166; G06F 1/1684; G06F
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 21/86; G06F 21/87; G06F 21/77-80;
 G06F 21/85-88; G06F 21/00; G06K
 19/06196; G06K 19/072; G06K 19/0721;
 G06K 19/0722; G06K 19/0723; G06K
 19/0724; G06K 19/0725; G06K 19/0726;
 G06K 19/0727; G06K 19/0728; G06K
 19/073; G06K 19/07309; G06K 19/077;
 G06K 19/07701; G06K 19/07715; G06K
 19/0772; G06K 19/07722; G06K
 19/07724; G06K 19/07726; G06K
 19/07728; G06Q 20/3229; G06Q 20/34;
 G06Q 20/341; G06Q 20/346; G06Q
 20/349; G06Q 20/3563; G06Q 20/3567;
 G06Q 20/357; G06Q 20/3576; H05K
 5/026; H05K 5/0256; H05K 5/0265;
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 5/0278; H05K 5/0282; H05K 5/0286;
 H05K 5/0291; H05K 5/0295; H05K 5/03;
 H05K 5/04; H05K 5/06; H05K 5/061;
 H05K 5/062; H05K 5/063; H05K 5/064;
 H05K 5/065; H05K 5/066; H05K 5/067;
 H05K 5/068; H05K 5/069; H05K 7/00;
 H05K 7/005; H05K 7/02; H05K 7/023;
 H05K 7/026; H05K 7/04; H05K 7/10;
 H05K 7/1418; H05K 7/142; H05K
 7/1424; H05K 7/1427-1439; H05K
 7/1461; H05K 7/1464-1474; H05K
 7/1479; H05K 7/1481; H05K
 7/1485-1488; H05K 7/1411; H05K
 2201/09745; H05K 2201/09754; H05K
 2201/09763; H05K 2201/09772; H05K
 2201/098; H05K 2201/09818; H05K
 2201/10; H05K 2201/10007; H04N
 2201/216; H04B 1/38; H04B 1/3827;
 H04B 1/3833; H04B 1/385; H04B
 1/3888; H04B 1/3838; H04B 2001/3844;
 H04B 2001/3855; H04B 2001/3861

See application file for complete search history.

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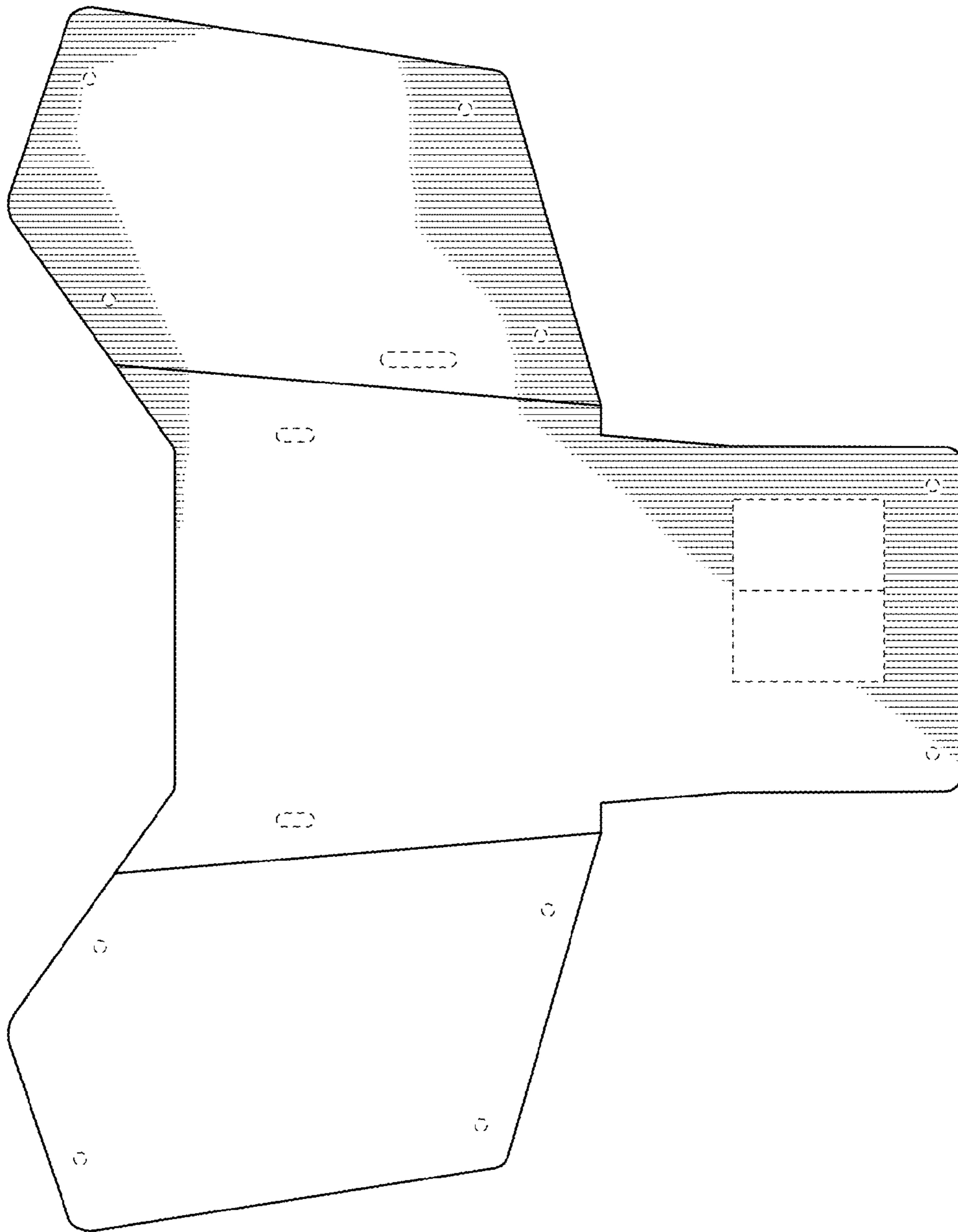


FIG. 1

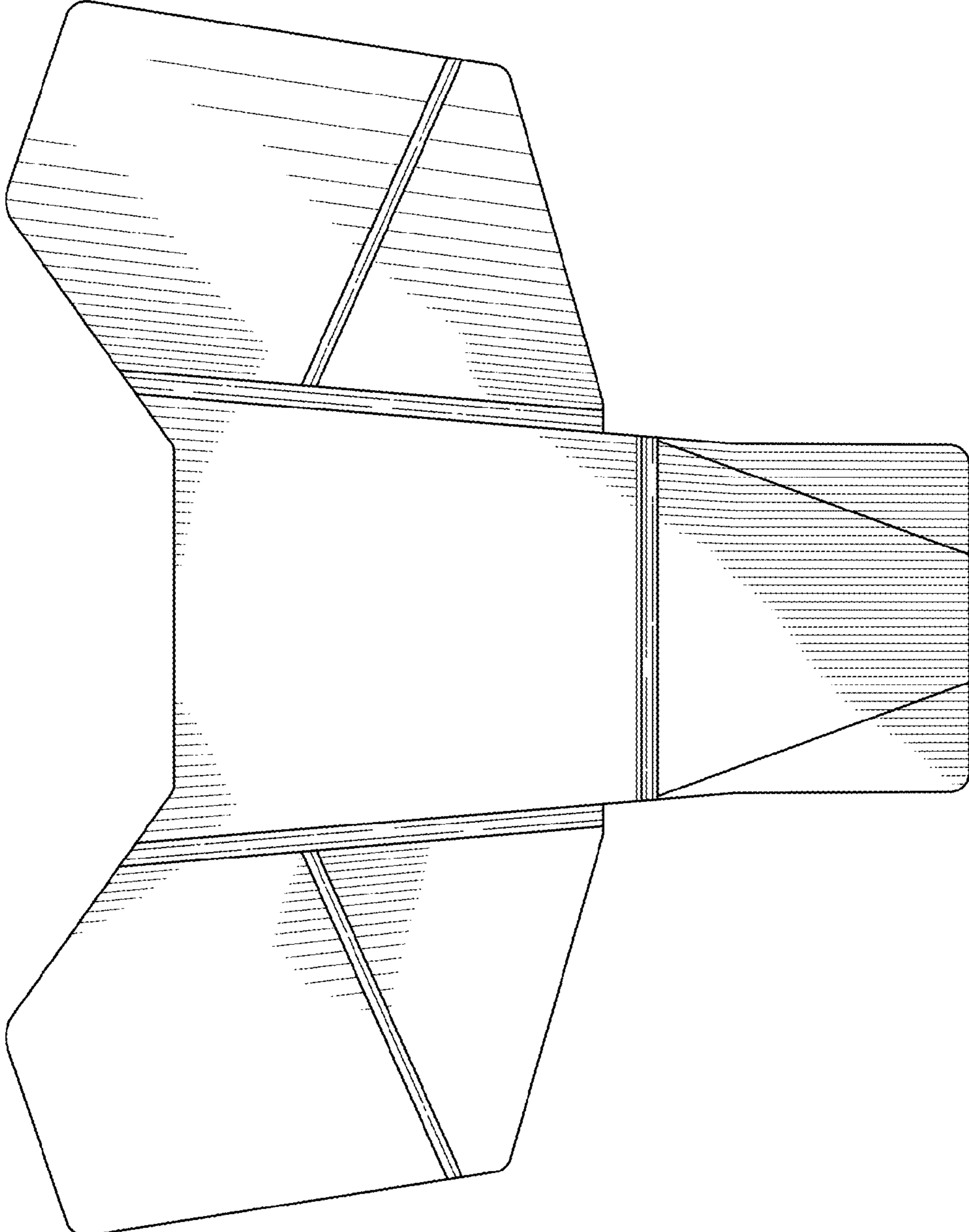


FIG. 2

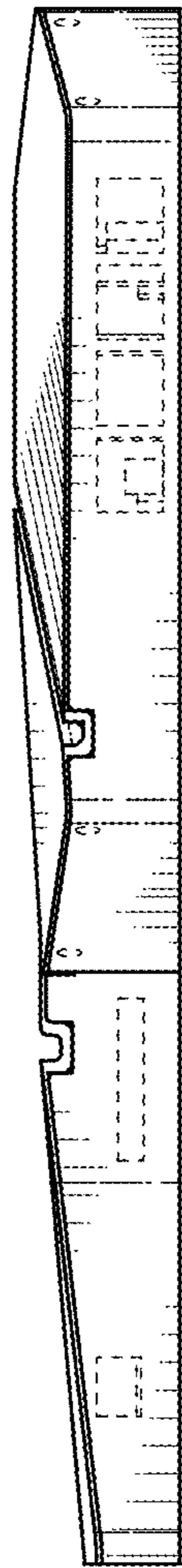


FIG. 3

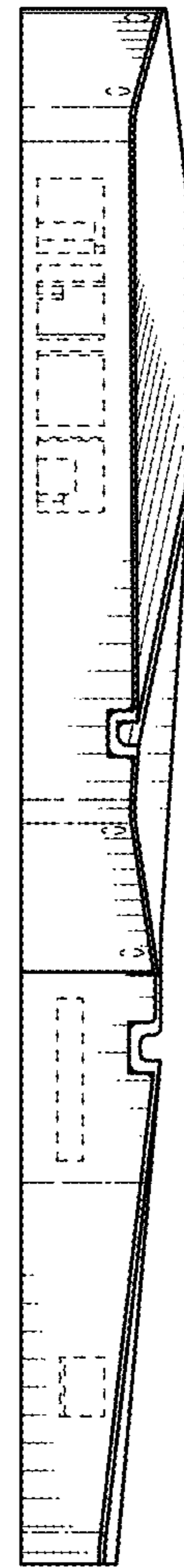


FIG. 4

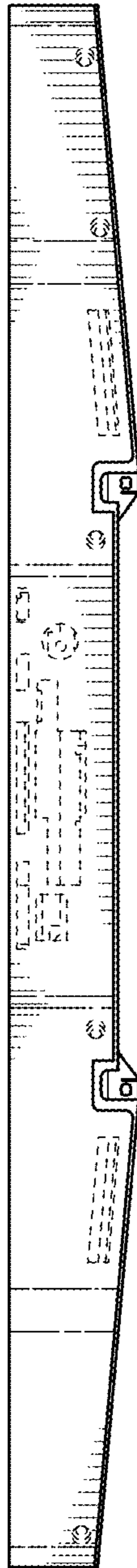


FIG. 5

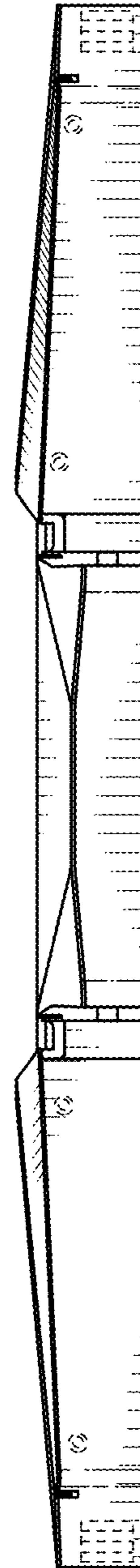


FIG. 6

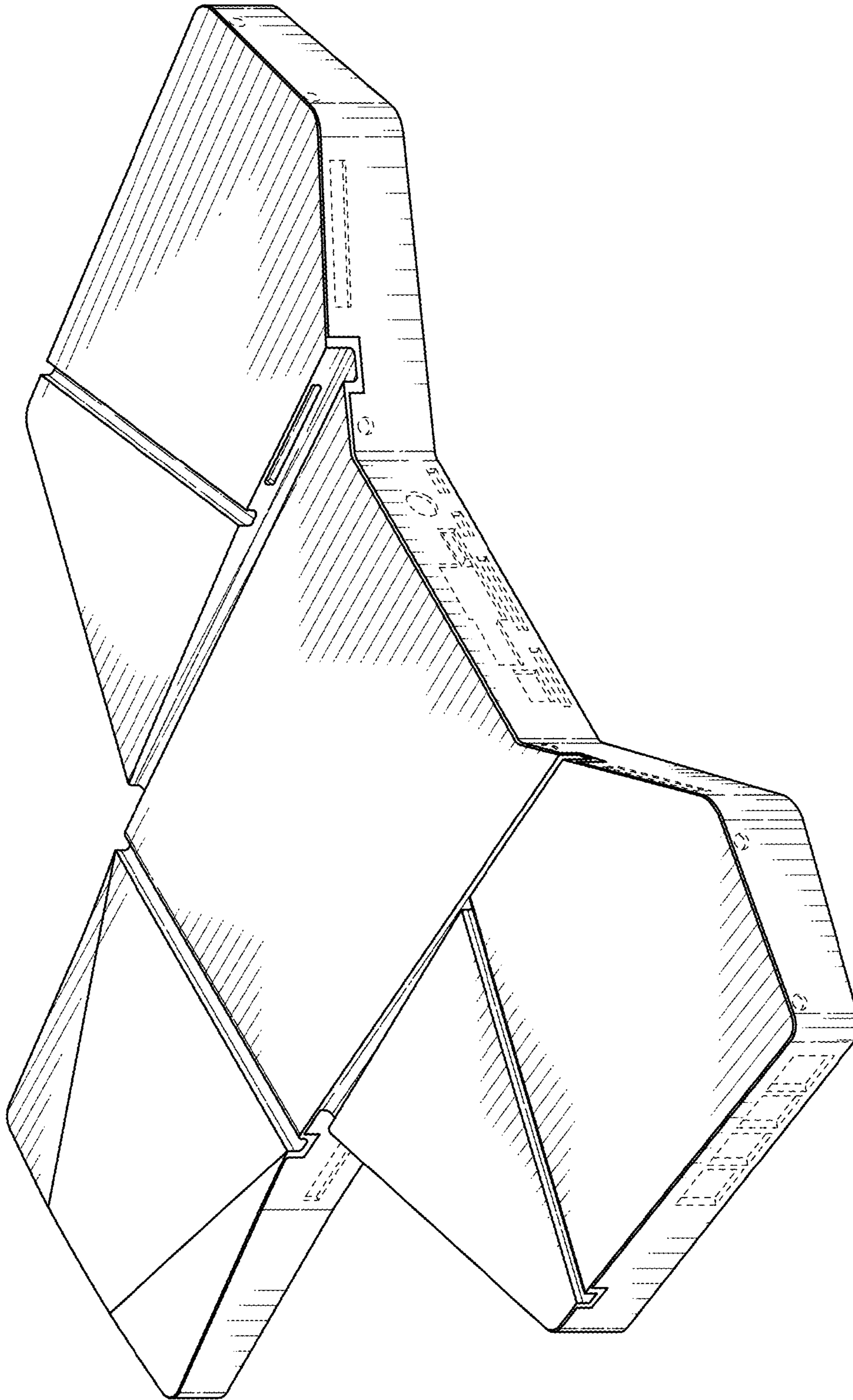


FIG. 7

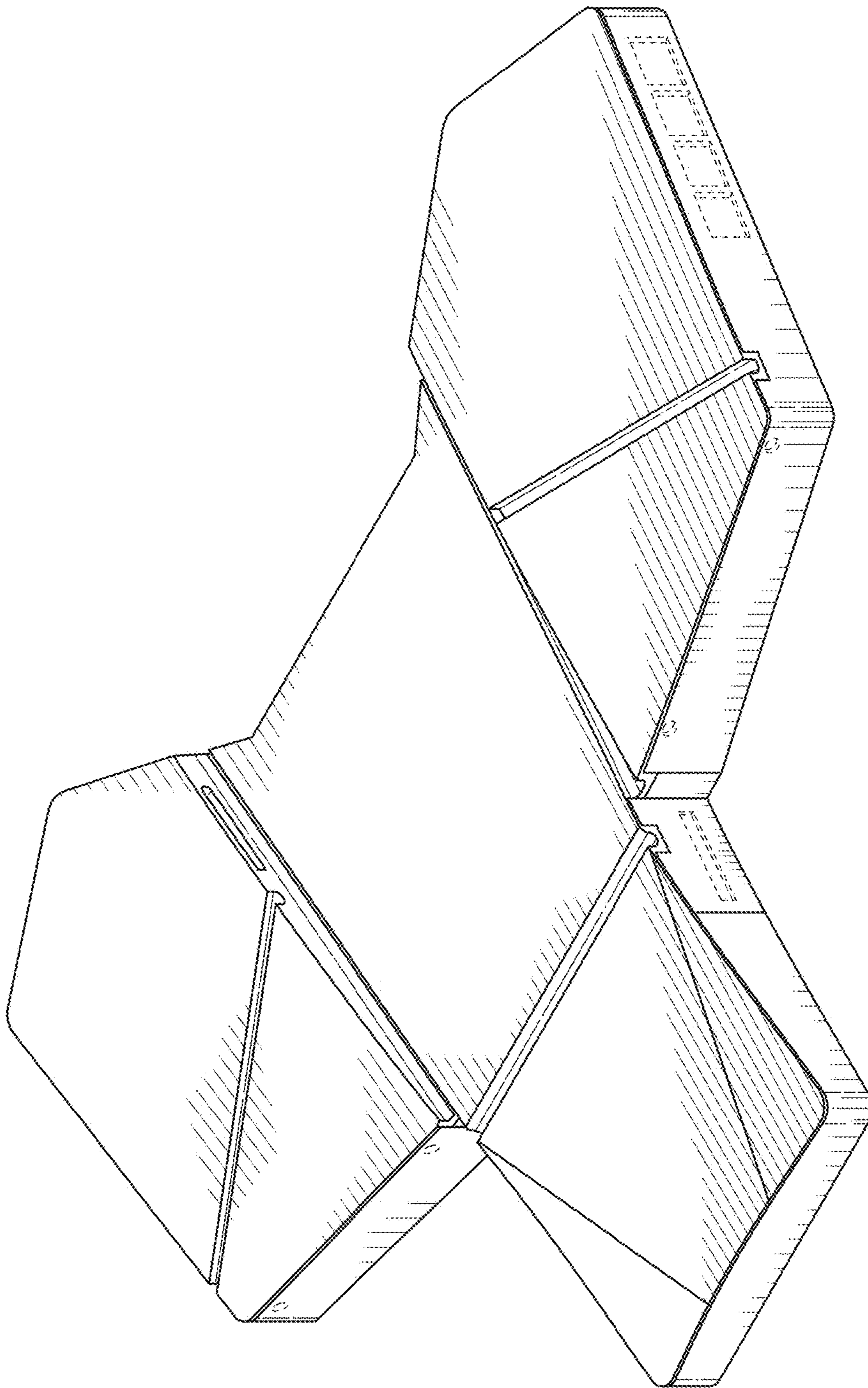


FIG. 8

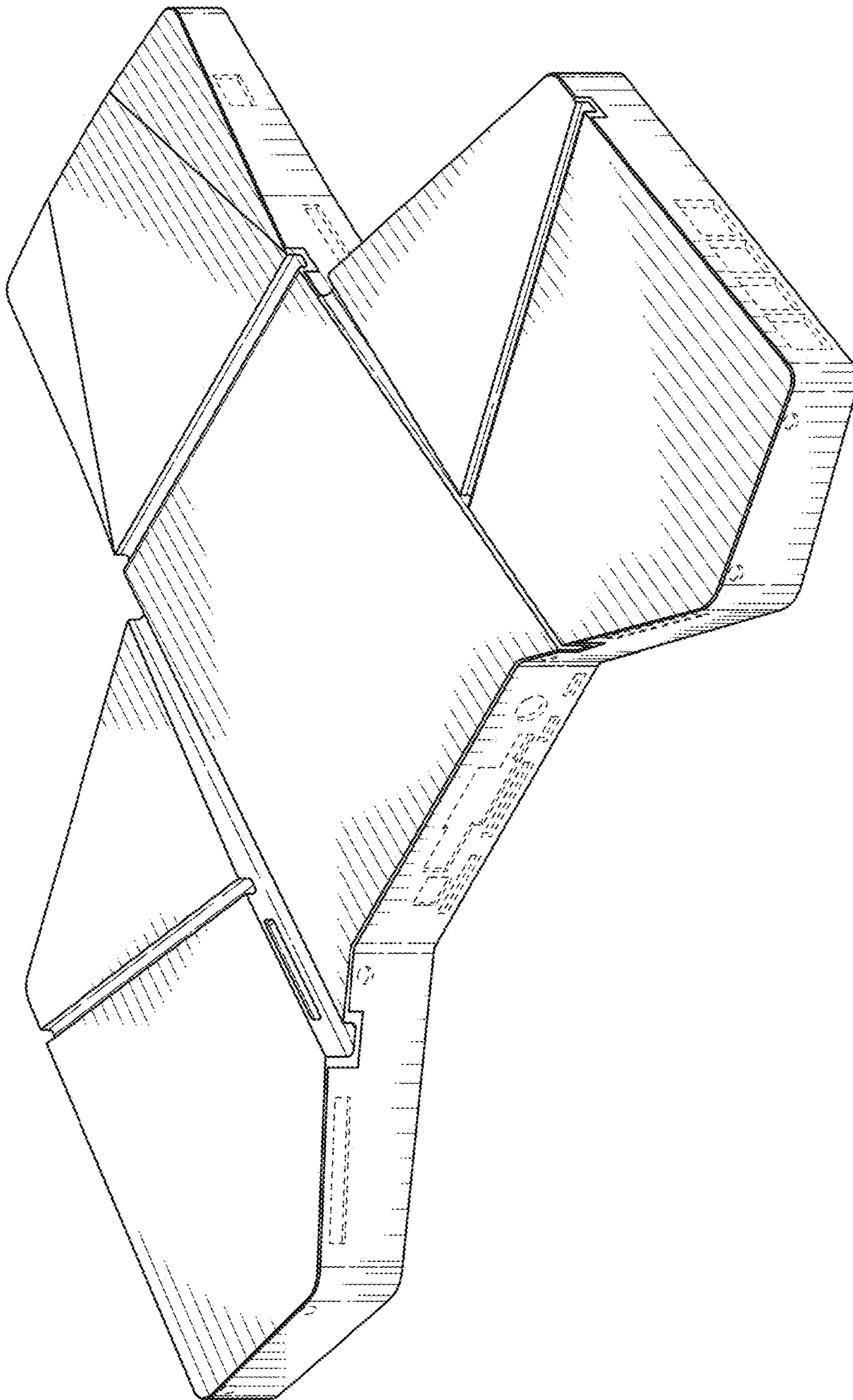


FIG. 9

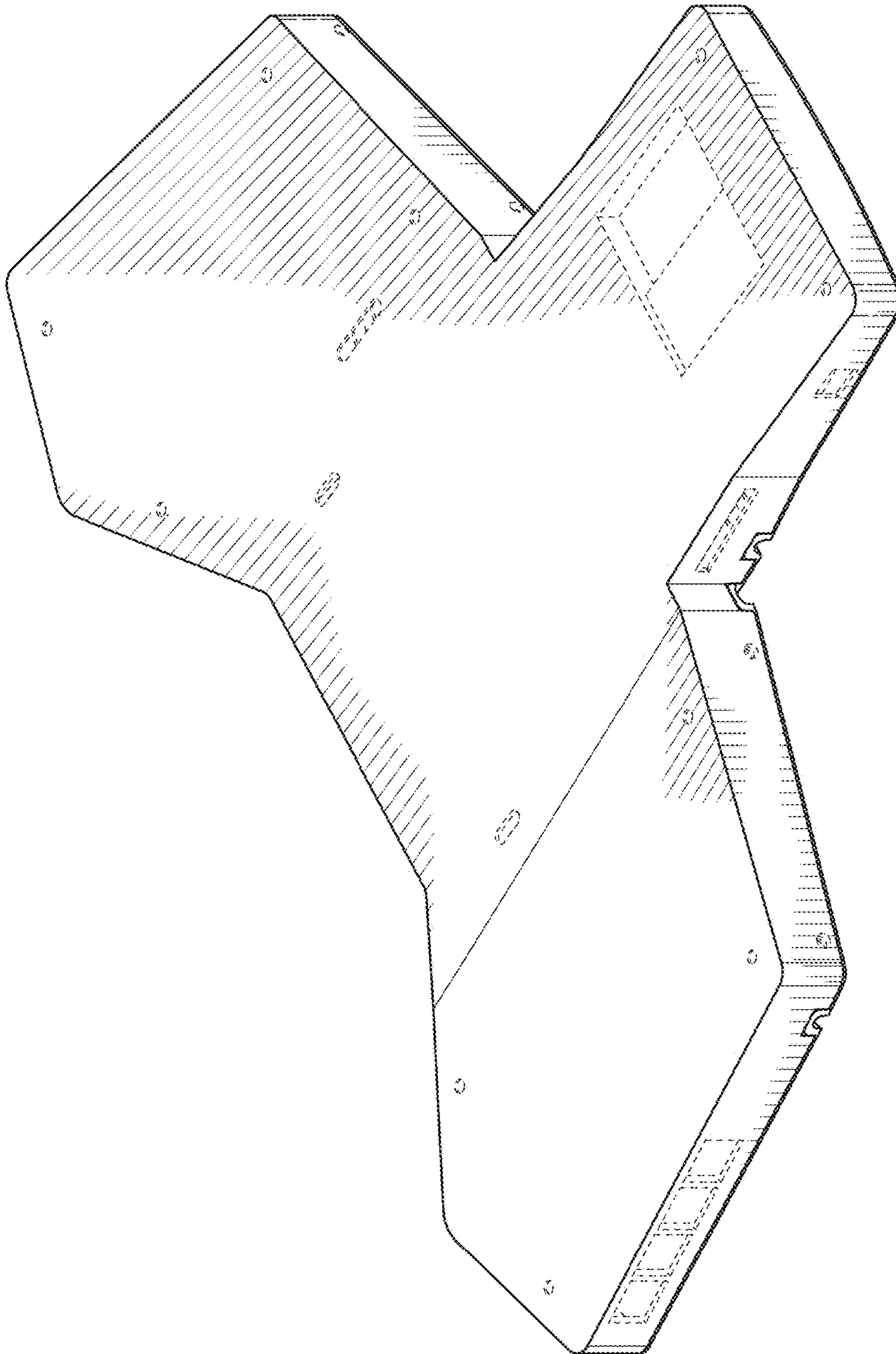


FIG. 10