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(12) **United States Design Patent**  
**Sakamoto**

(10) **Patent No.:** **US D863,238 S**  
(45) **Date of Patent:** **\*\* Oct. 15, 2019**

- (54) **LIGHT EMITTING DIODE CHIP**
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- (\*\*) Term: **15 Years**
- (21) Appl. No.: **29/638,198**
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- (51) **LOC (12) Cl.** ..... **13-03**
- (52) **U.S. Cl.**  
USPC ..... **D13/180**
- (58) **Field of Classification Search**  
USPC ..... D13/180; D26/1  
CPC ..... H01L 25/167; H01L 25/0753; H01L 27/0248; H01L 27/15; H01L 27/156; H01L 33/00; H01L 33/04; H01L 33/08; H01L 33/10; H01L 33/20; H01L 33/38; H01L 33/42; H01L 33/48; H01L 33/62; H01L 33/483; H01L 33/486  
See application file for complete search history.

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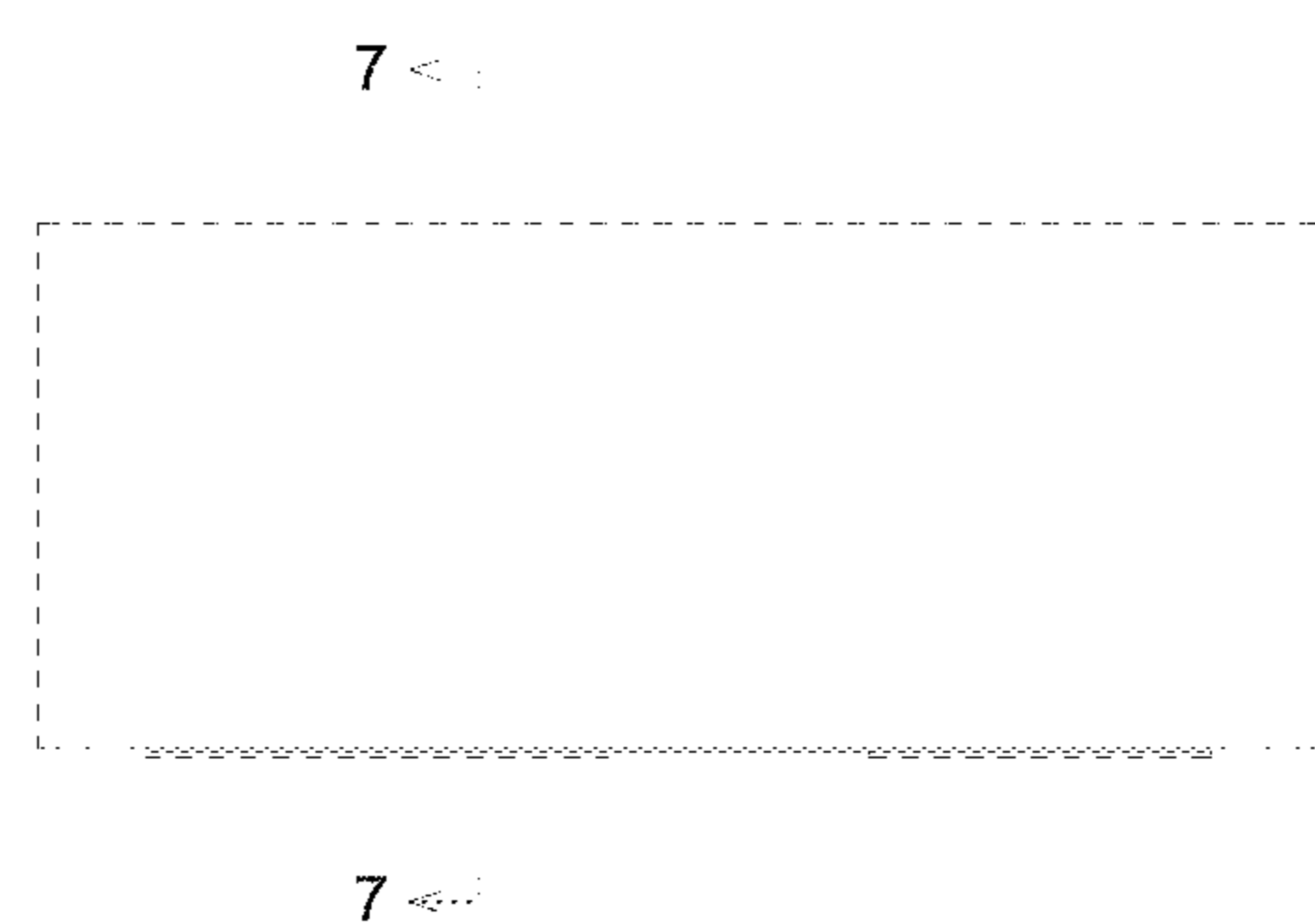
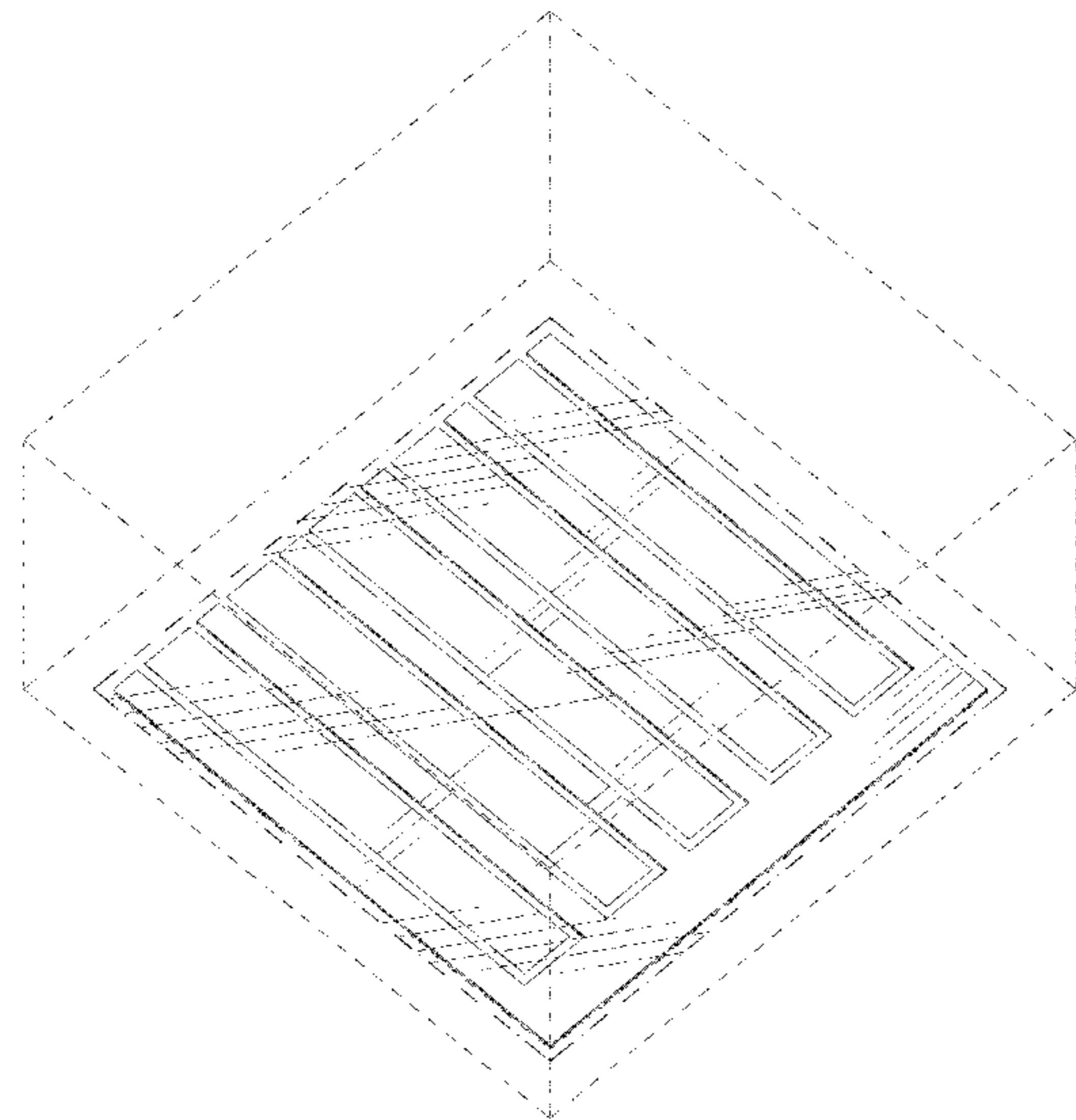
(57) **CLAIM**  
The ornamental design for a light emitting diode chip, as shown and described.

**DESCRIPTION**

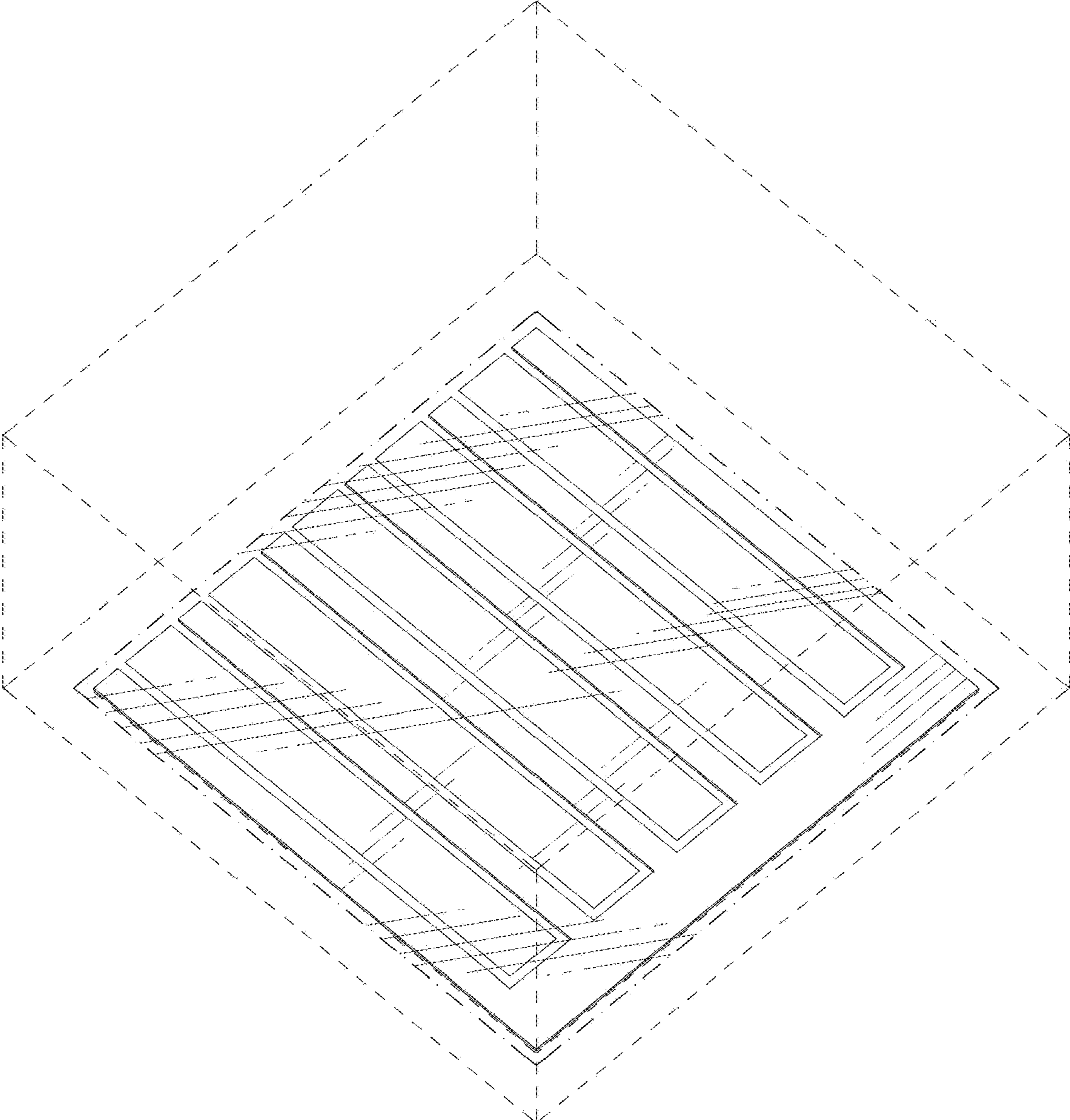
FIG. 1 is a front perspective view of a light emitting diode chip showing my new design;  
FIG. 2 is a front view thereof;  
FIG. 3 is a top view thereof;  
FIG. 4 is a right side view thereof;  
FIG. 5 is a left side view thereof;  
FIG. 6 is a bottom view thereof;  
FIG. 7 is a cross-sectional view taken along line 7-7 in FIG. 2; and,  
FIG. 8 is an enlarged partial view of a circled portion 8 of FIG. 7.

The broken lines shown in the drawings are illustrative purpose only and form no part of the claimed design. The dash-dot-dash broken lines are used to show the boundary between unclaimed and claimed subject matter, and thus form no part of the claimed design. The top layer is substantially transparent or translucent.

**1 Claim, 8 Drawing Sheets**



*FIG. 1*



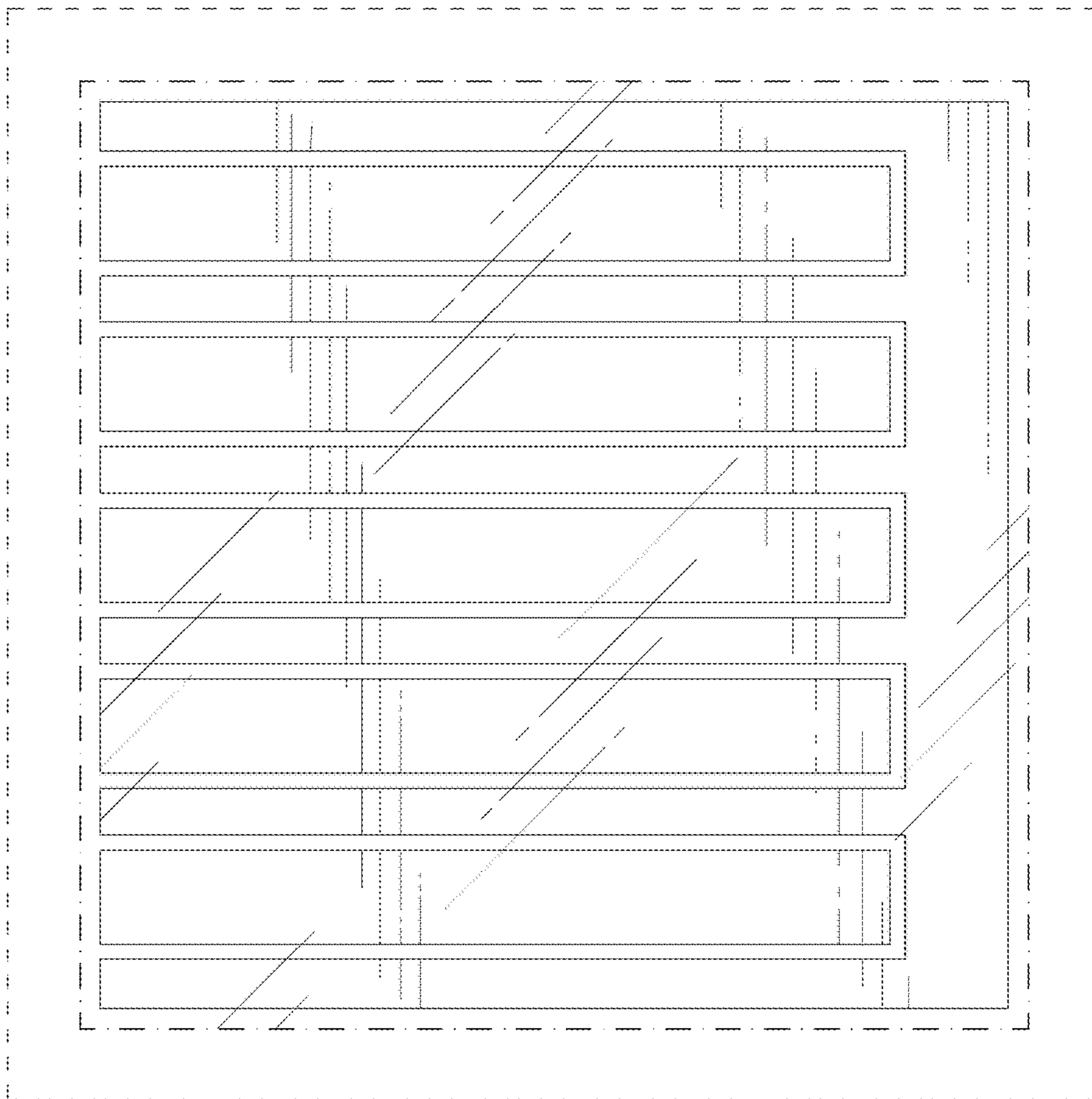
*FIG. 2*

7 ←



7 ←

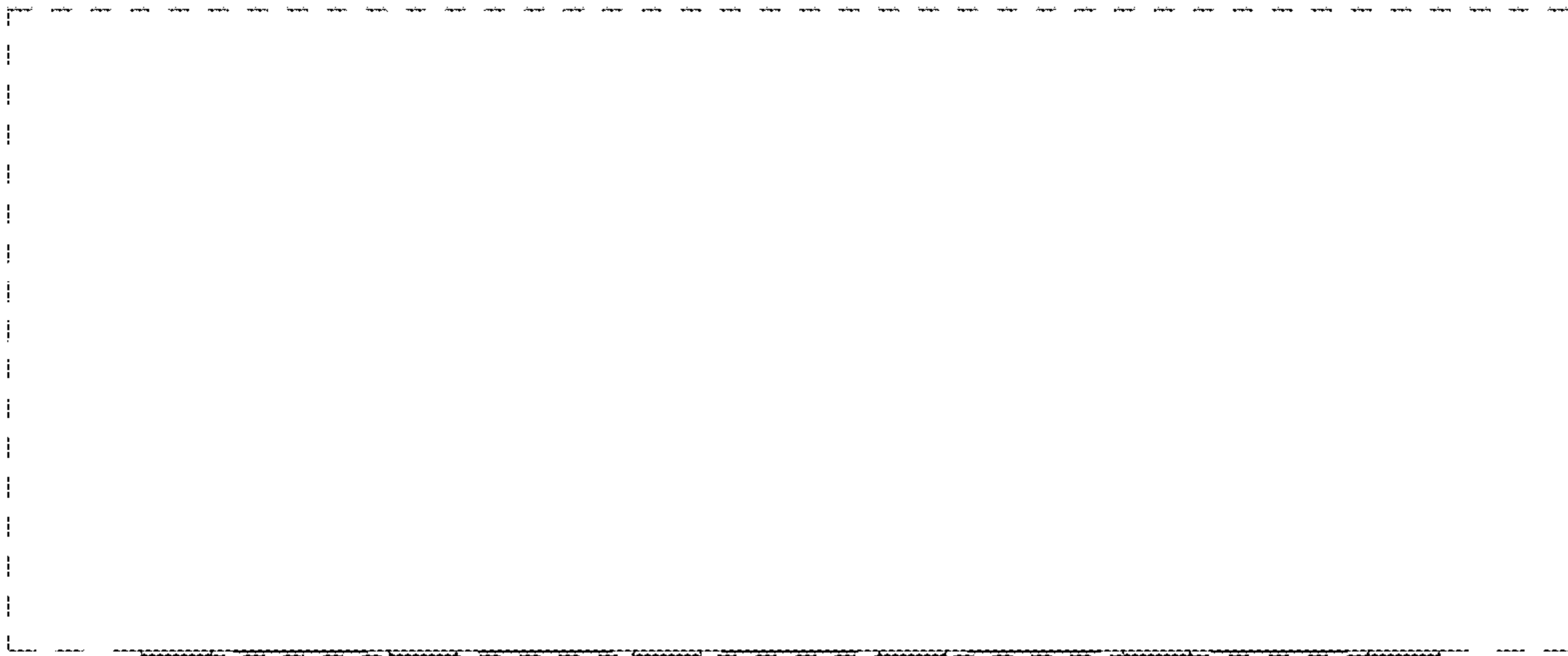
*FIG. 3*



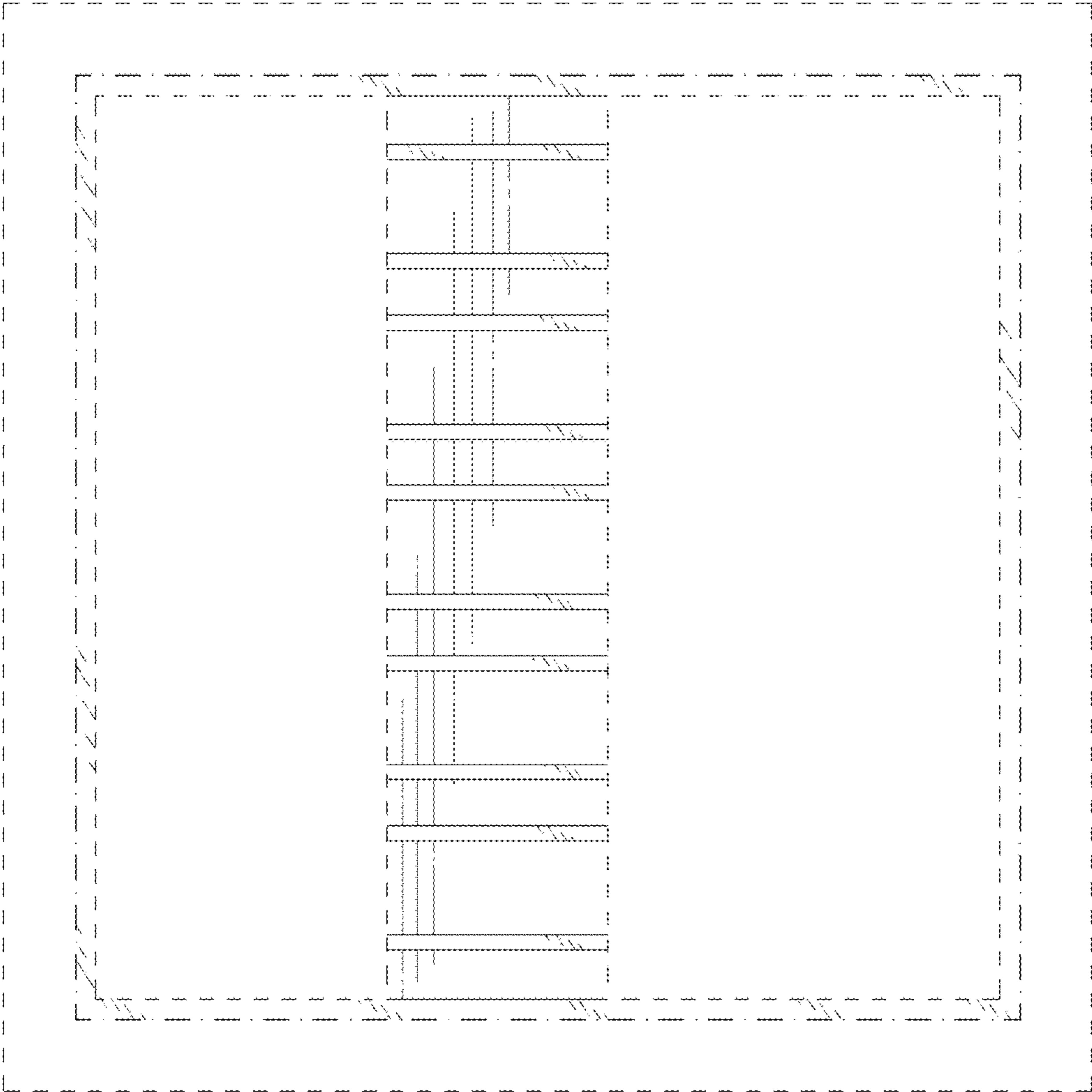
*FIG. 4*



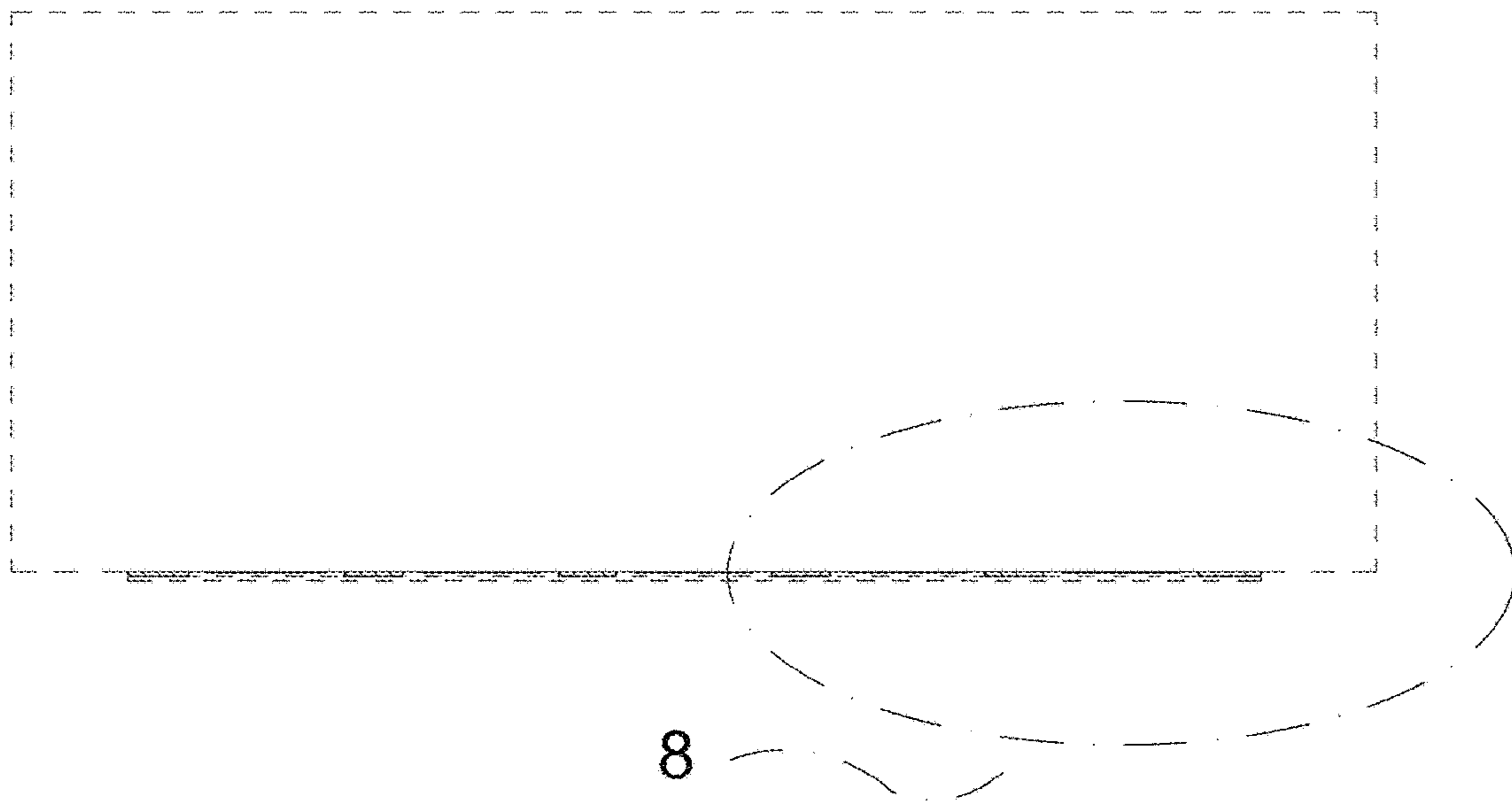
*FIG. 5*



*FIG. 6*



*FIG. 7*





*FIG. 8*

