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(12) **United States Design Patent** (10) **Patent No.:** **US D860,135 S**
Narita et al. (45) **Date of Patent:** **** Sep. 17, 2019**

(54) **ELECTRODE FOIL FOR CAPACITOR**

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(**) Term: **15 Years**

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(51) **LOC (12) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/121; D13/182**

(58) **Field of Classification Search**
USPC D13/101, 110, 121, 133, 182, 199;
118/500, 728, 729; 156/345.51, 345.52,
156/345.53; D5/53, 60
CPC H01L 21/68707; H01L 21/68721; H01L
21/68728; H01L 21/68735; H01L
21/68785; H01L 21/67144; H01L
21/67309; C23C 16/45565; C23C
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H01M 10/0436

See application file for complete search history.

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(57) **CLAIM**

The ornamental design for an electrode foil for a capacitor, as shown and described.

DESCRIPTION

FIG. 1 is a front elevational view of an electrode foil for capacitor showing our new design;

FIG. 2 is a top plan view thereof;

FIG. 3 is a right side elevational view thereof;

FIG. 4 is a left side elevational view thereof;

FIG. 5 is a rear elevational view thereof; and

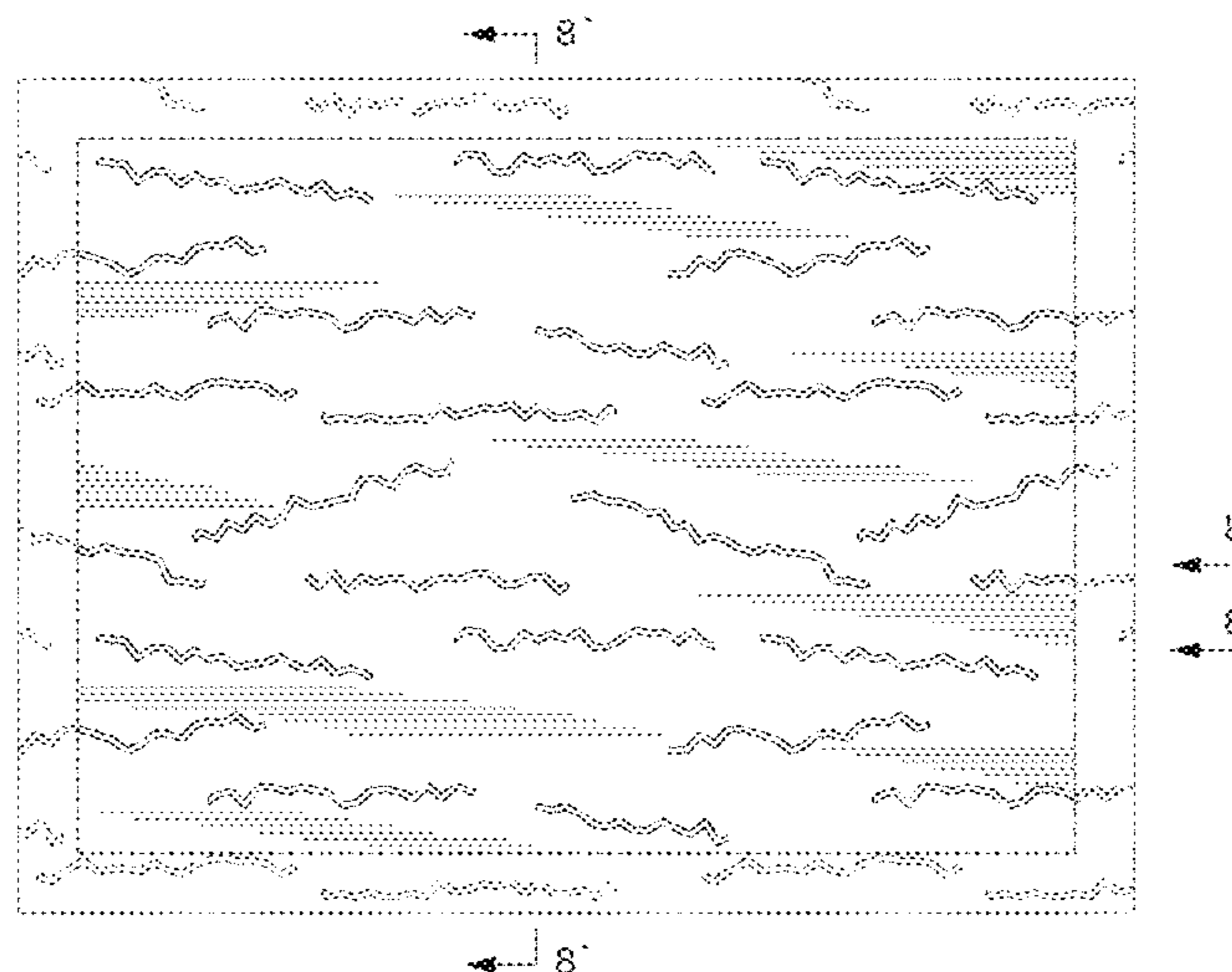
FIG. 6 is a bottom plan view thereof.

FIG. 7 is a partially enlarged top plan view thereof taken along lines 7-7 and 7'-7' of FIG. 2; and,

FIG. 8 is a partially enlarged cross sectional view thereof taken along lines 8-8 and 8'-8' of FIG. 7.

The broken lines shown represent portions of the electrode foil for capacitor that form no part of the claim. Where the dot-dash broken lines about the shaped surface it is understood that those broken lines represent an unclaimed boundary between claimed and unclaimed surfaces. None of the broken lines form any part of the claimed design.

1 Claim, 8 Drawing Sheets



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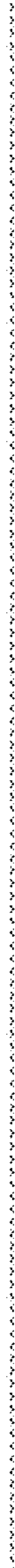


FIG. 1

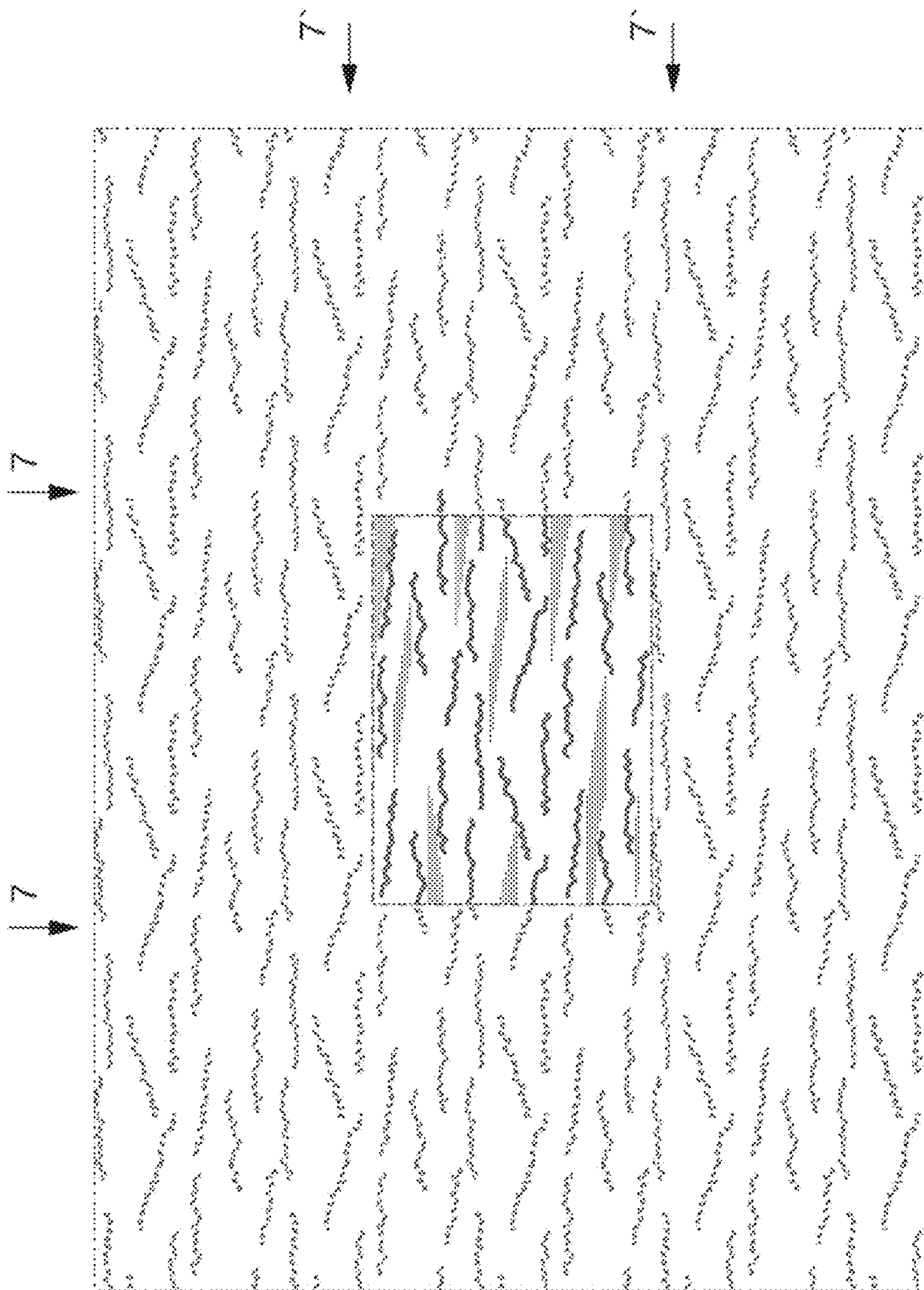


FIG. 2

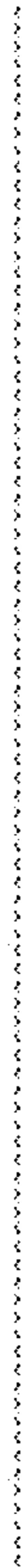


FIG. 3

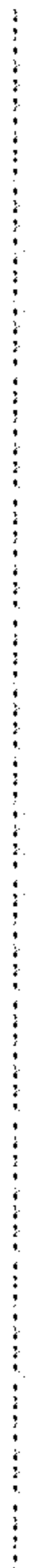


FIG.4

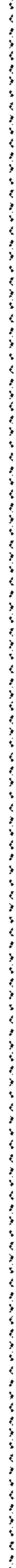


FIG.5

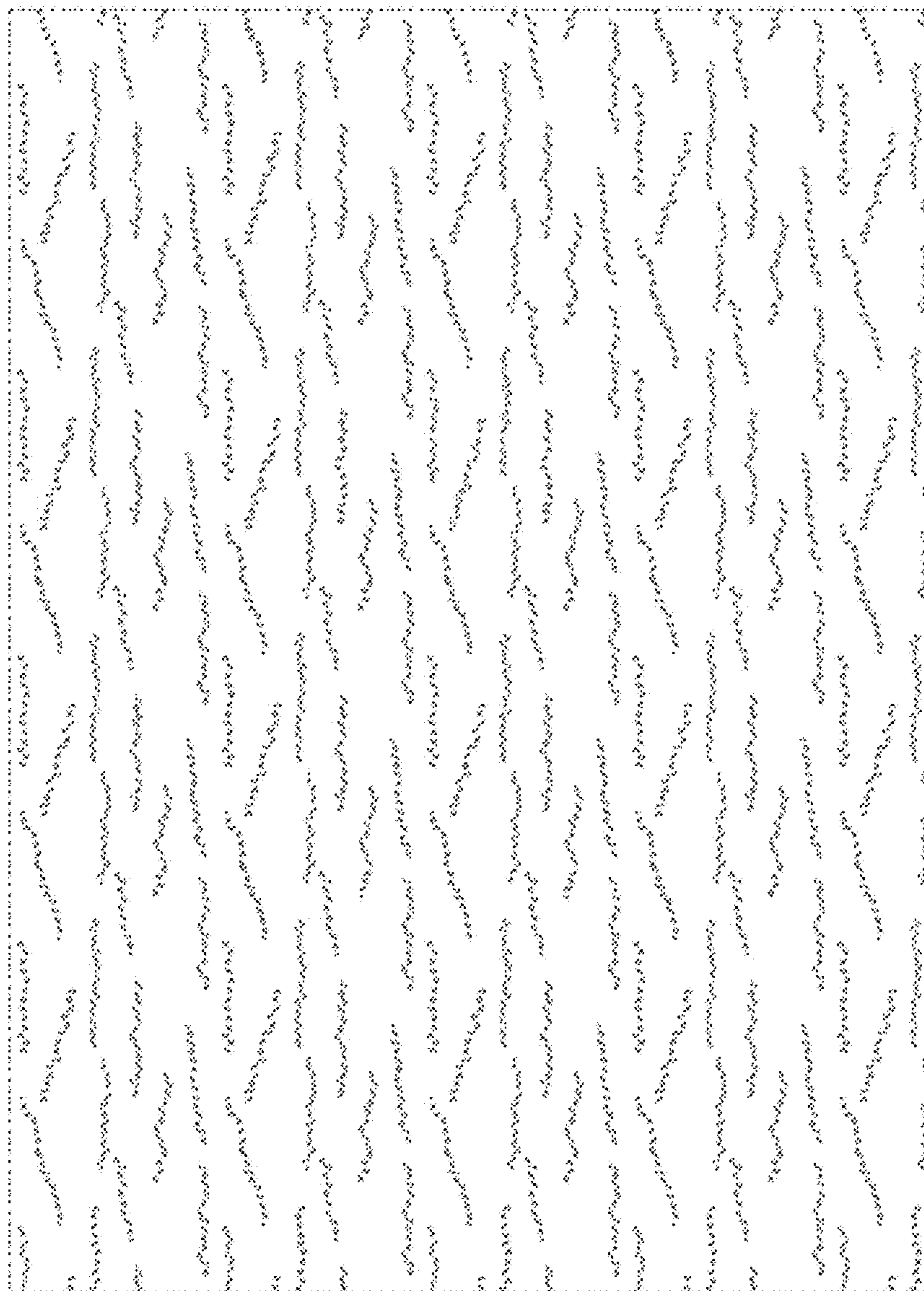


FIG.6

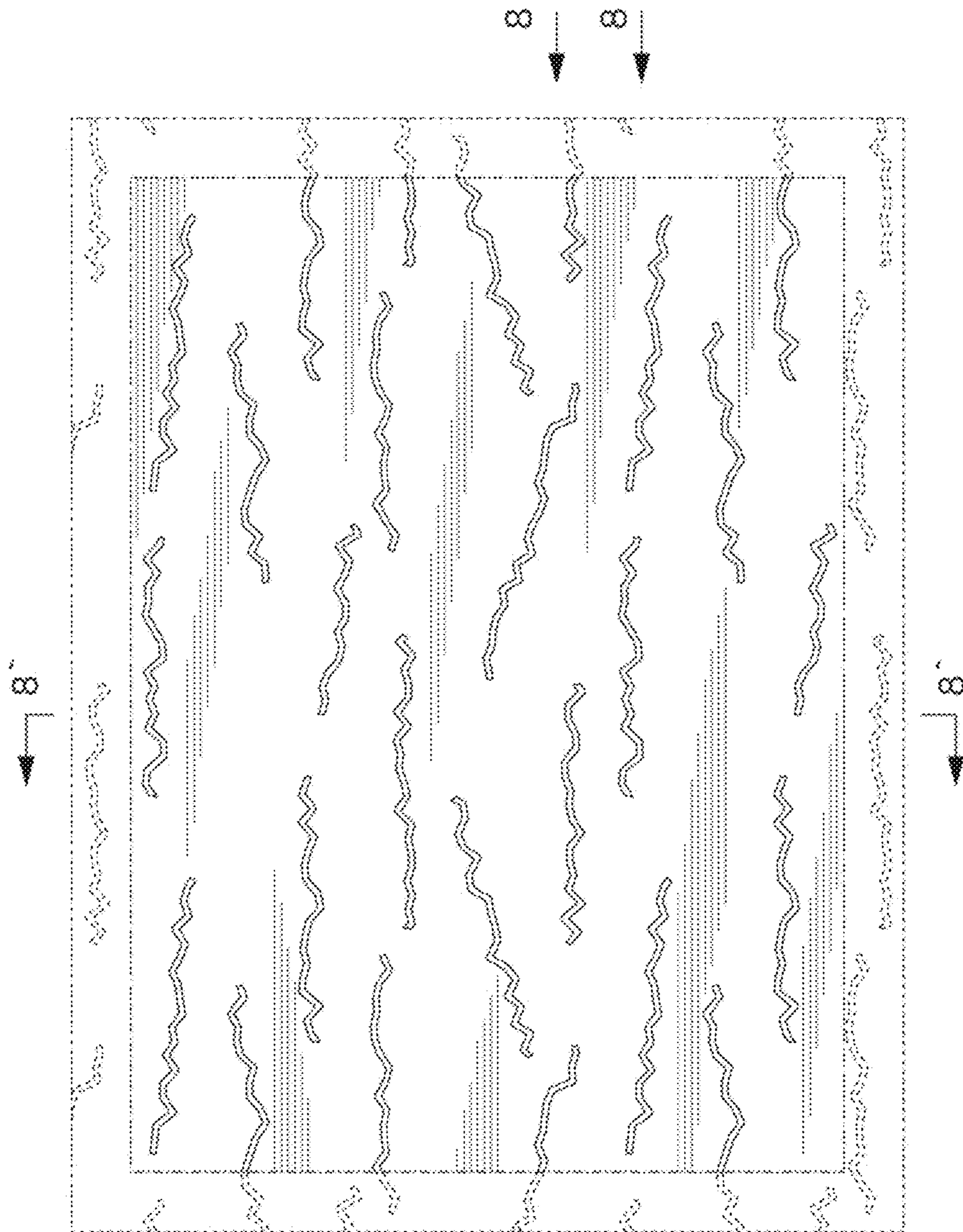


FIG.7

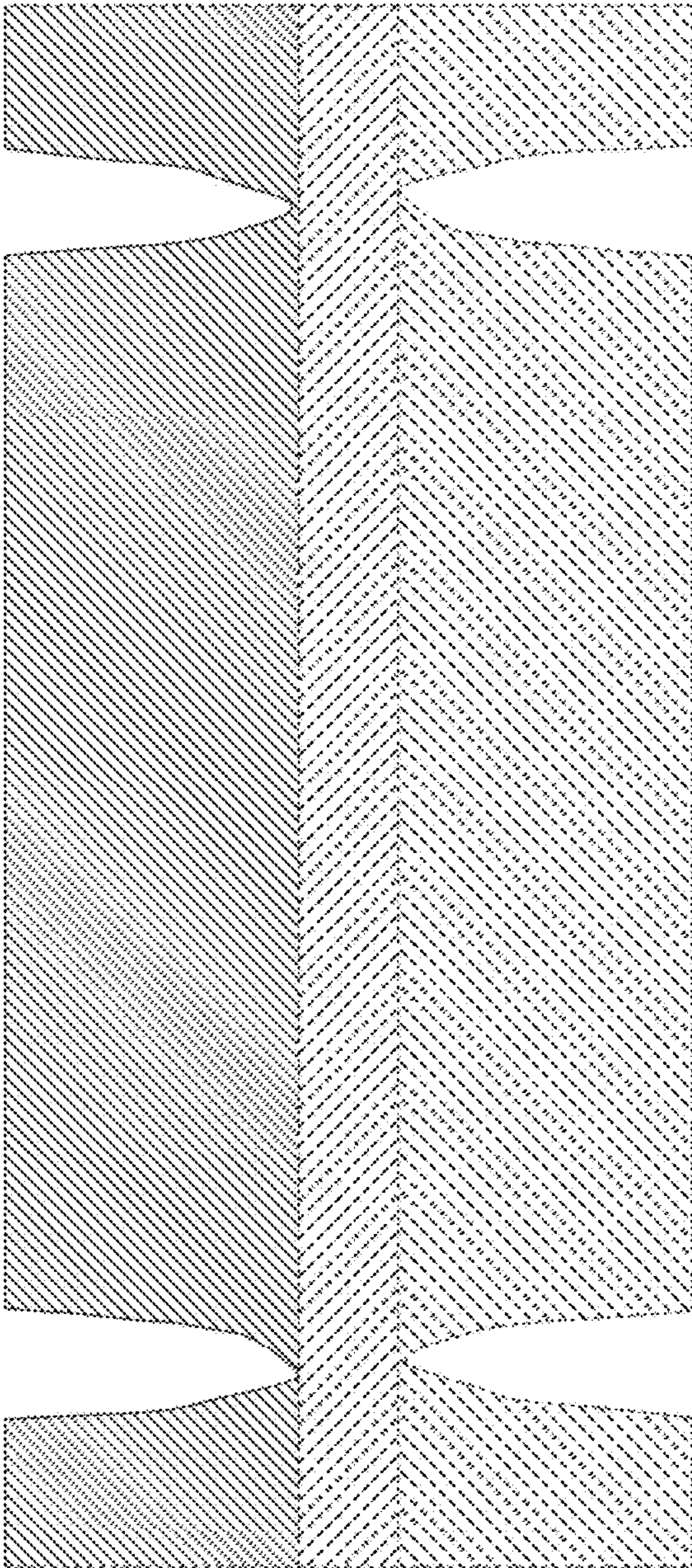


FIG. 8