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(12) **United States Design Patent** (10) **Patent No.: US D856,947 S**
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(54) **SEMICONDUCTOR DEVICE**

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(**) Term: **15 Years**

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(30) **Foreign Application Priority Data**

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(51) **LOC (12) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182
CPC H01L 21/00; H01L 21/02433; H01L 2224/42; H01L 2224/43; H01L 2021/00; H01L 2021/02; H01L 2021/04; H01L 21/4814; H01L 21/4846; H01L 21/4871; H01L 21/67144; H01L 23/12; H01L 23/13; H01L 23/14; H01L 23/147; H01L 2924/171; H01L 2924/1711; H01L 2924/1715; H01L 2924/17151; H01L 2924/181; H01L 2924/1811; H01L 2924/1815; H01L 2924/19042; H01L 2924/1905; H01L 2224/08054; H01L 23/58; H05B 41/14; H02B 6/4201; G02B 6/4256; G02B 6/4257; G02B 6/4261; G02B 6/4262; G02B 6/42; G02B 6/4281; H05K 1/14; H05K 1/141; H05K 1/142; H05K 1/144; H05K 1/18; H05K 1/181; H05K 1/182; H05K 1/026; H05K 1/0228; H05K 1/0245; H05K 1/0236; H05K 1/0263
See application file for complete search history.

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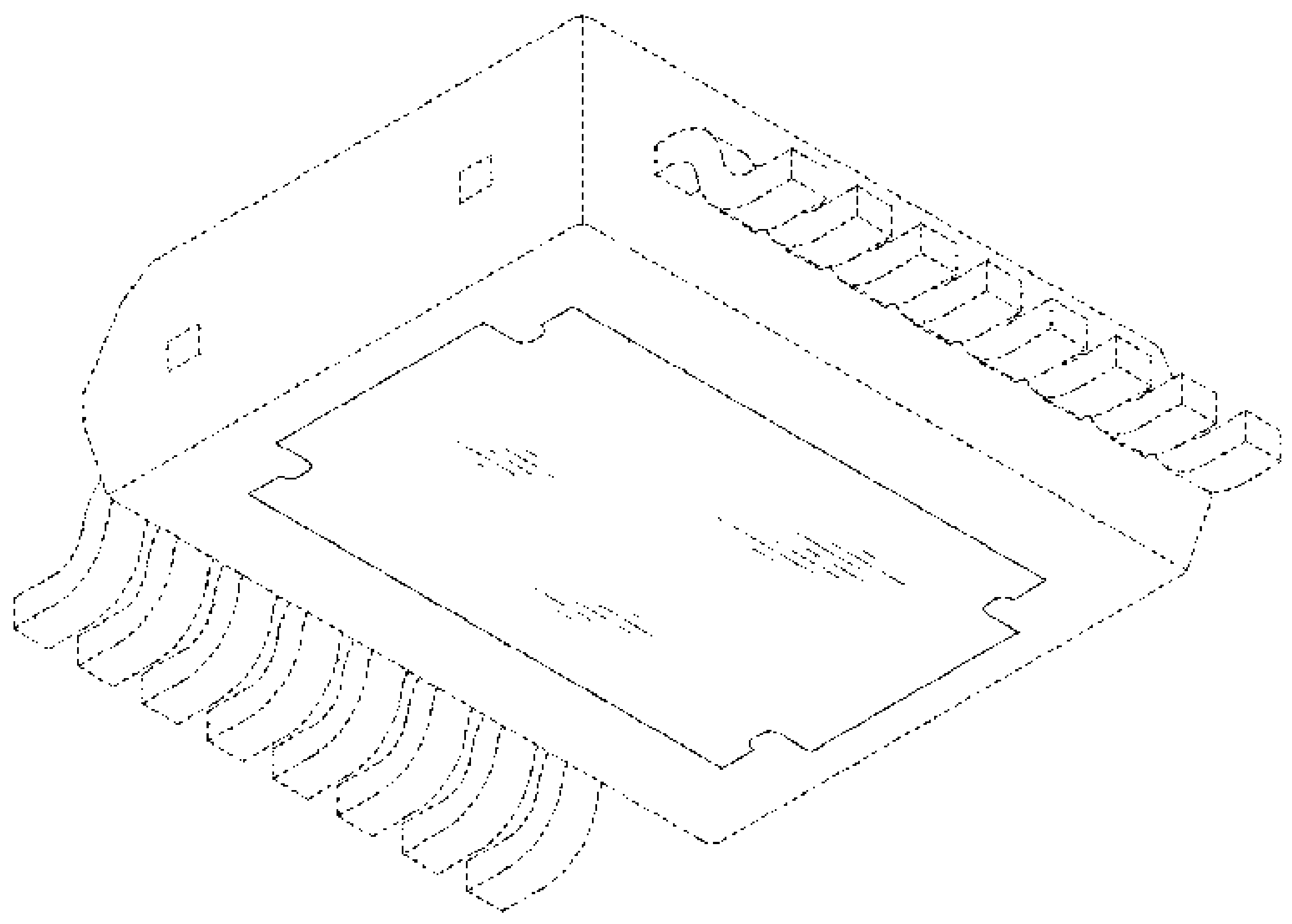
(57) **CLAIM**

The ornamental design for a semiconductor device, as shown and described.

DESCRIPTION

FIG. **1** is a perspective view of a semiconductor device showing my new design;
FIG. **2** is a front view thereof, the rear view being a mirror image of FIG. **2**;
FIG. **3** is a top plan view thereof;
FIG. **4** is a bottom plan view thereof;
FIG. **5** is a right side view thereof; and,
FIG. **6** is a left side view thereof.
The broken lines illustrate portions of the semiconductor device and form no part of the claimed design.

1 Claim, 6 Drawing Sheets



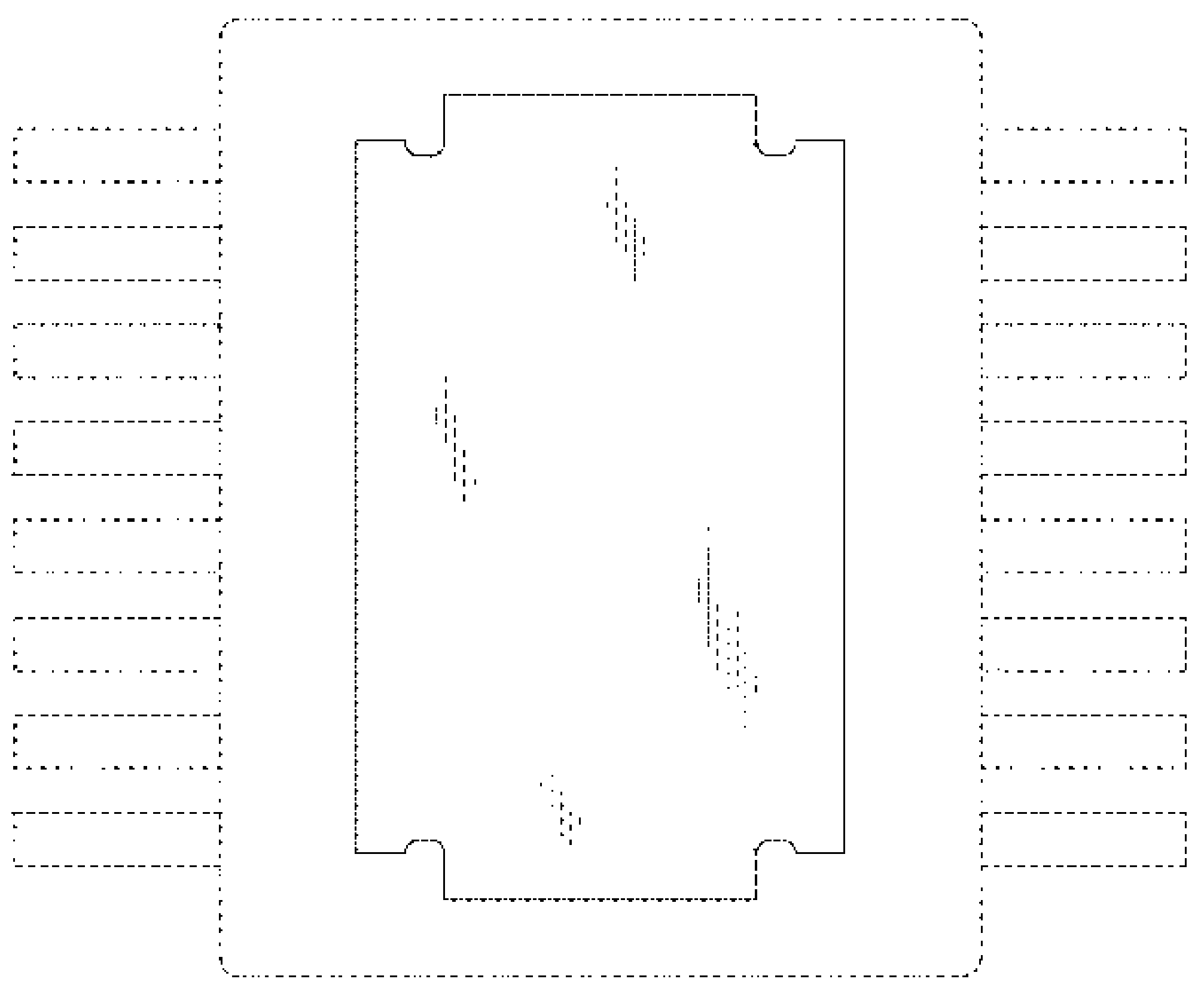


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FIG.1

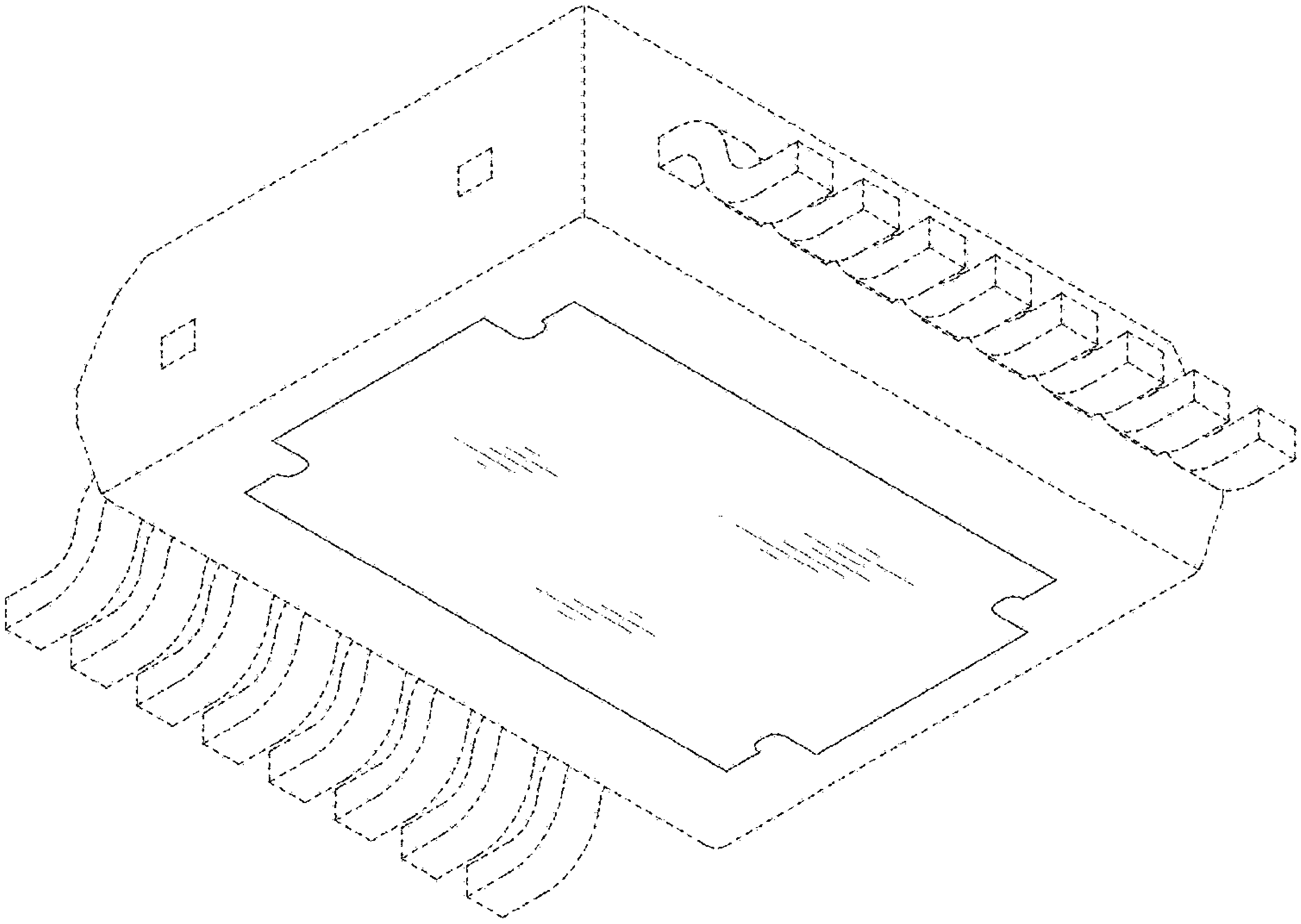

FIG.2

FIG.3

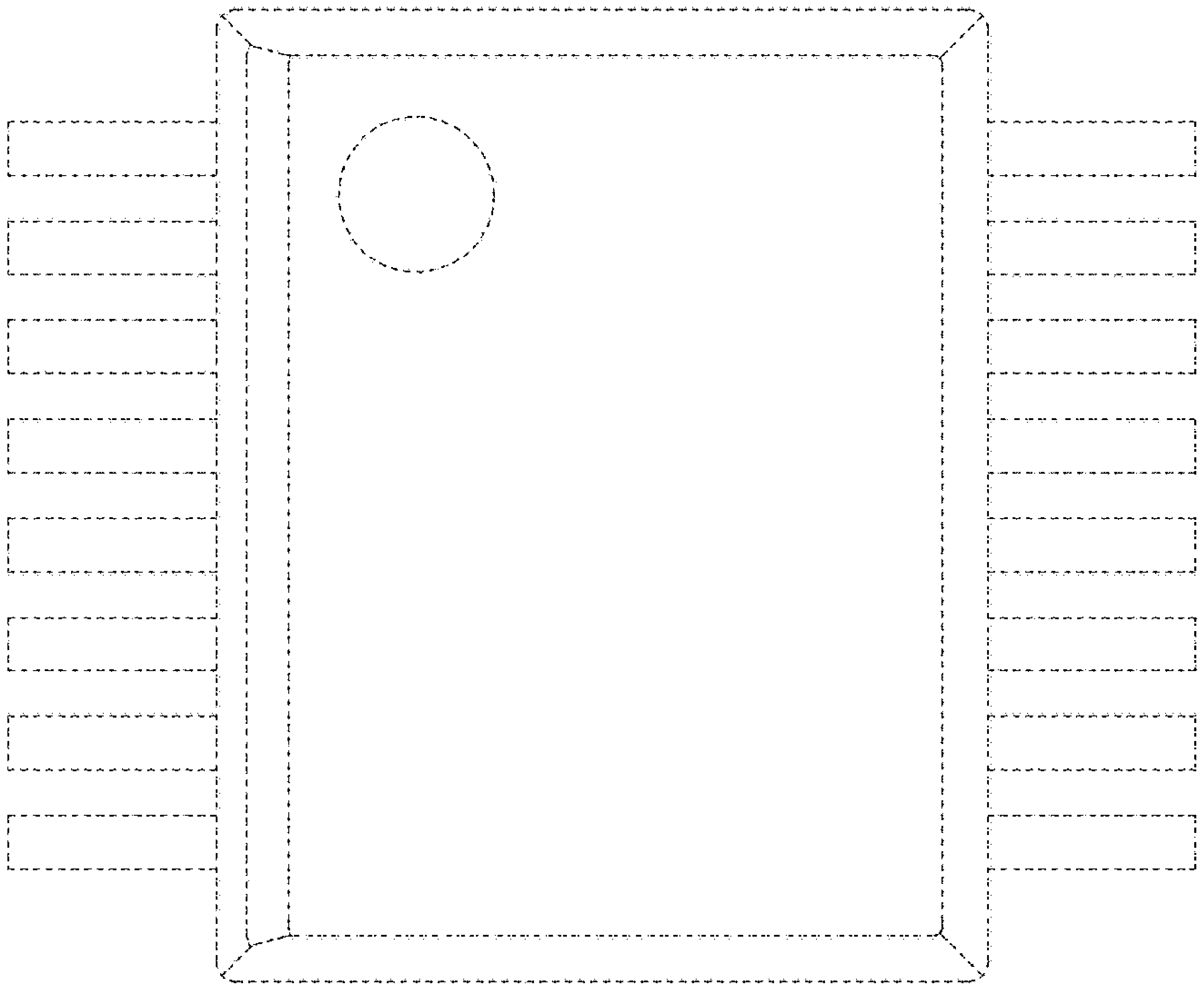

FIG.4

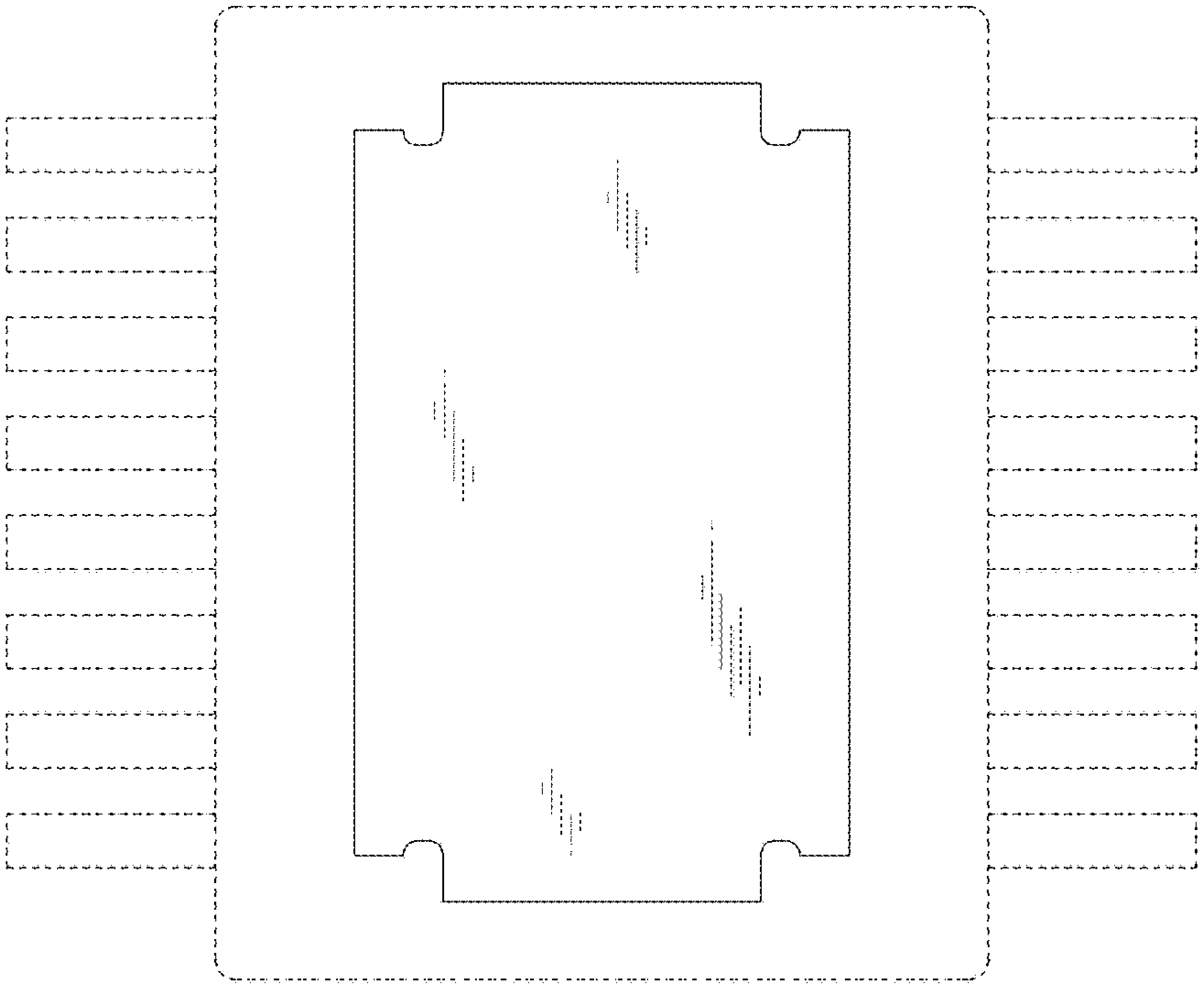

FIG.5

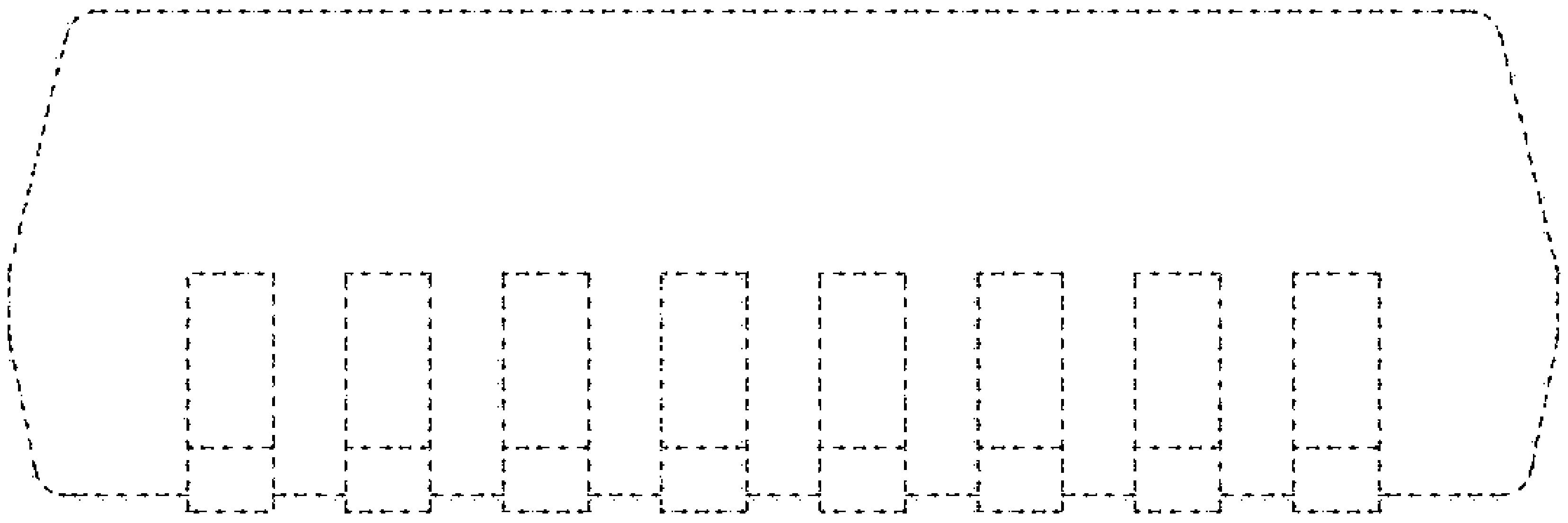

FIG.6