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(12) **United States Design Patent** (10) **Patent No.:** **US D855,621 S**  
**Elias et al.** (45) **Date of Patent:** **\*\* Aug. 6, 2019**

(54) **ELECTRONIC DEVICE MOUNT**  
(71) Applicants: **James Harrison Elias**, Rosenheim (DE); **Eric Johnston**, Marion, NY (US)

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(\*\*) Term: **15 Years**

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(21) Appl. No.: **29/608,533**

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(22) Filed: **Jun. 22, 2017**

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**Related U.S. Application Data**

(63) Continuation-in-part of application No. 29/604,727, filed on May 19, 2017.

(51) **LOC (12) Cl.** ..... **08-07**

(52) **U.S. Cl.**  
USPC ..... **D14/447**

(58) **Field of Classification Search**  
USPC ..... D14/447, 432, 434, 439, 440, 451, 452, D14/457, 239; D8/363, 373, 380; D6/406.3, 406.4, 406.5, 406.6; D12/415; D16/214, 242, 244, 245  
CPC ..... A47B 21/04; A47B 2097/006; A47B 2097/005; A47B 2023/049; A45C 2011/002; A45C 2011/003; F16M 2200/00; F16M 13/00

See application file for complete search history.

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(57) **CLAIM**

The ornamental design for an electronic device mount, as shown and described.

**DESCRIPTION**

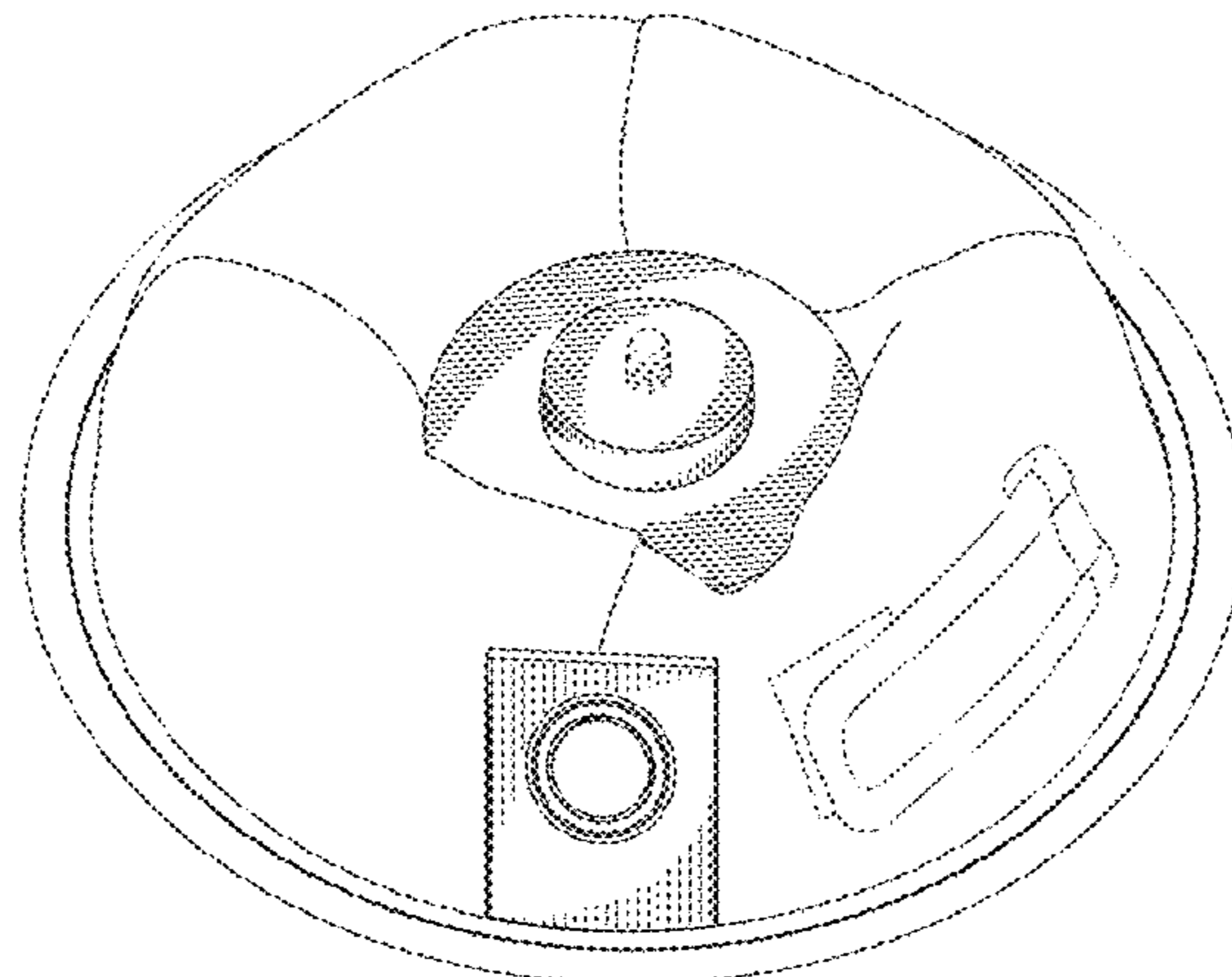
FIG. 1 is a perspective view of the top, front and right sides of an electronic device mount shown in a typical use configuration;  
FIG. 2 is a front view of the electronic device mount;  
FIG. 3 is a rear view of the electronic device mount;  
FIG. 4 is a left side view of the electronic device mount;  
FIG. 5 is right side view of the electronic device mount; and, FIG. 6 is a top view of the electronic device mount.  
The bottom of the electronic device mount is flat and devoid of surface ornamentation.  
The broken-lines in the above-described figures are for illustrative purposes only, and form no part of the claimed design.

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**1 Claim, 4 Drawing Sheets**



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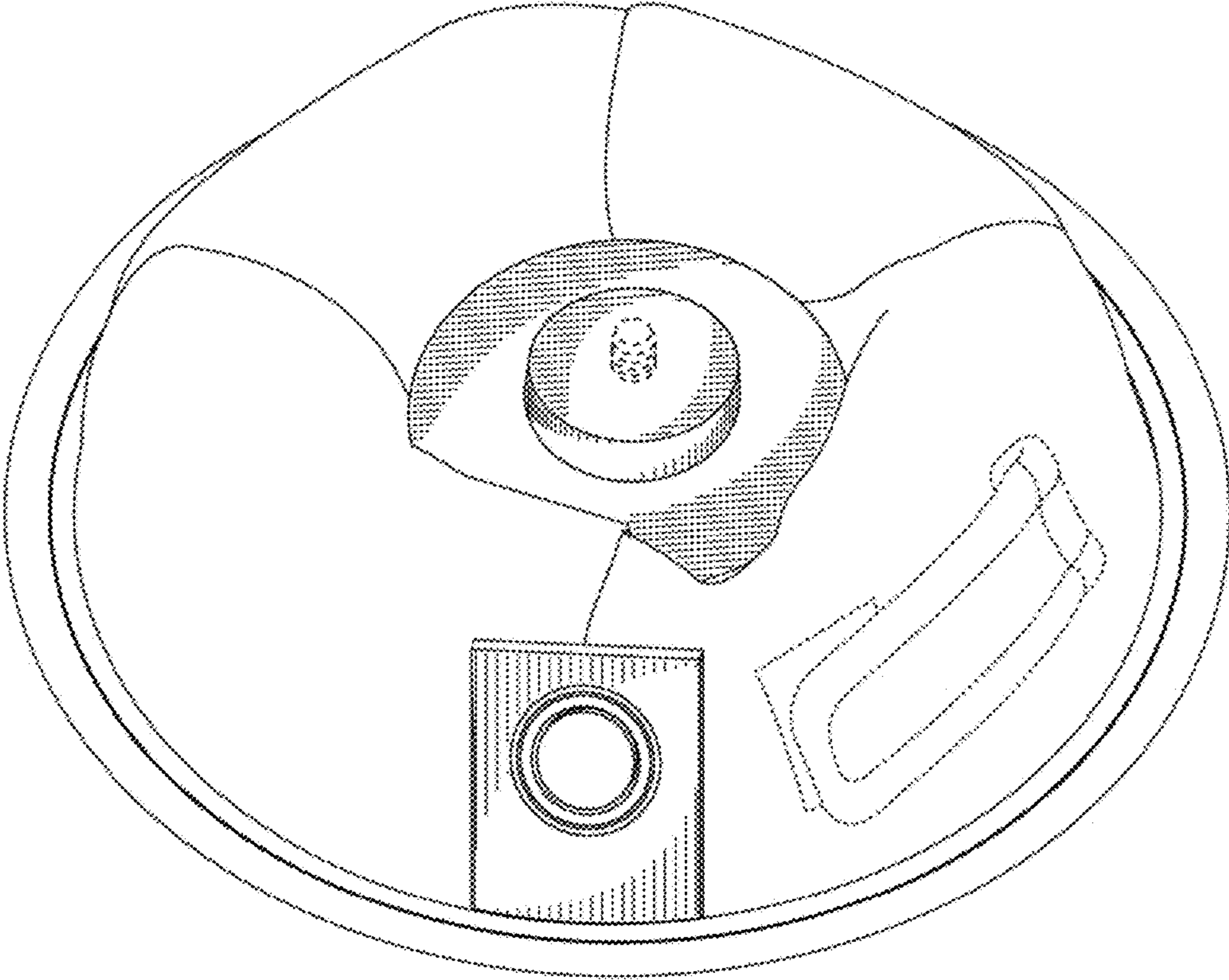


FIG. 1

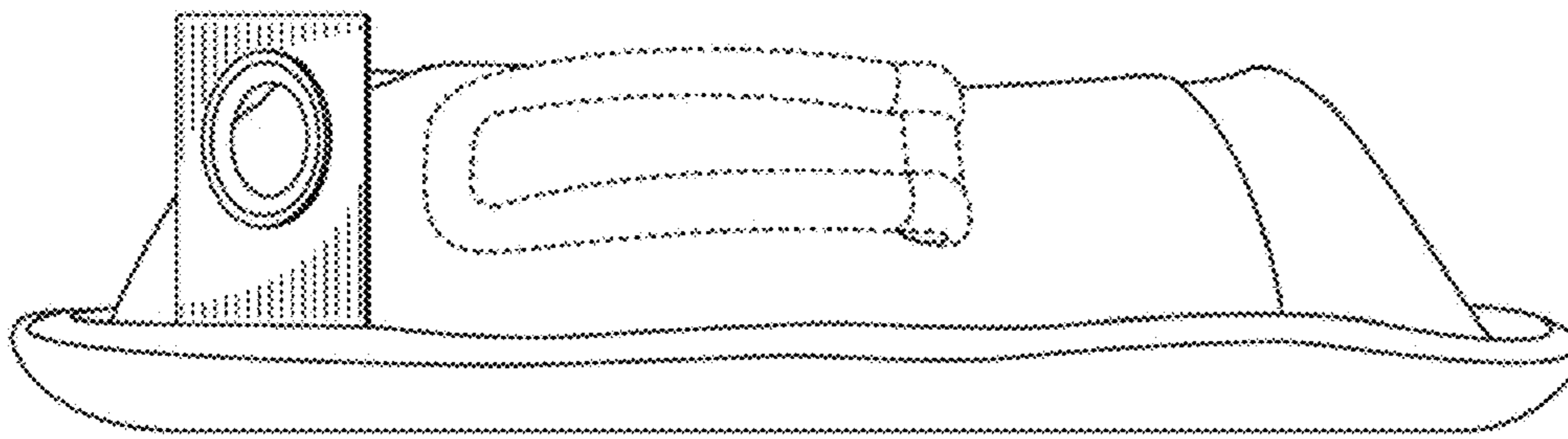


FIG. 2

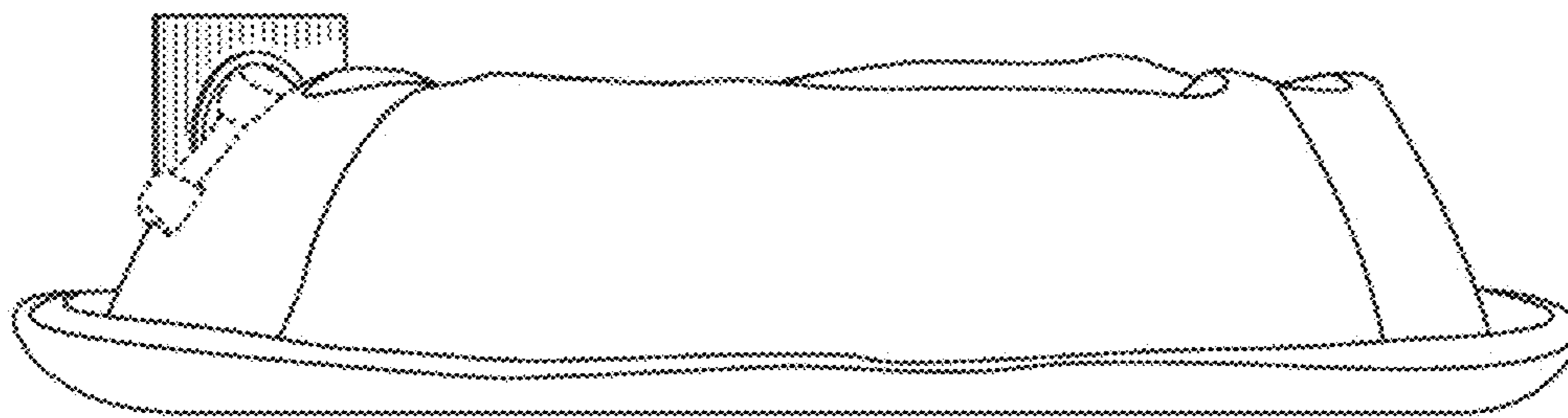


FIG. 3



FIG. 4

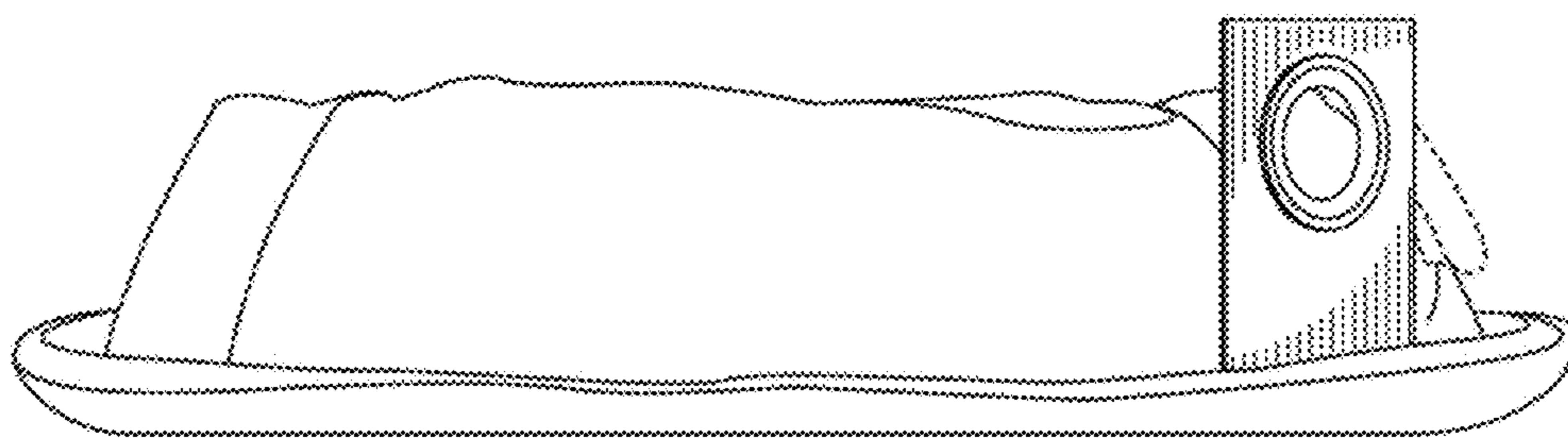


FIG. 5

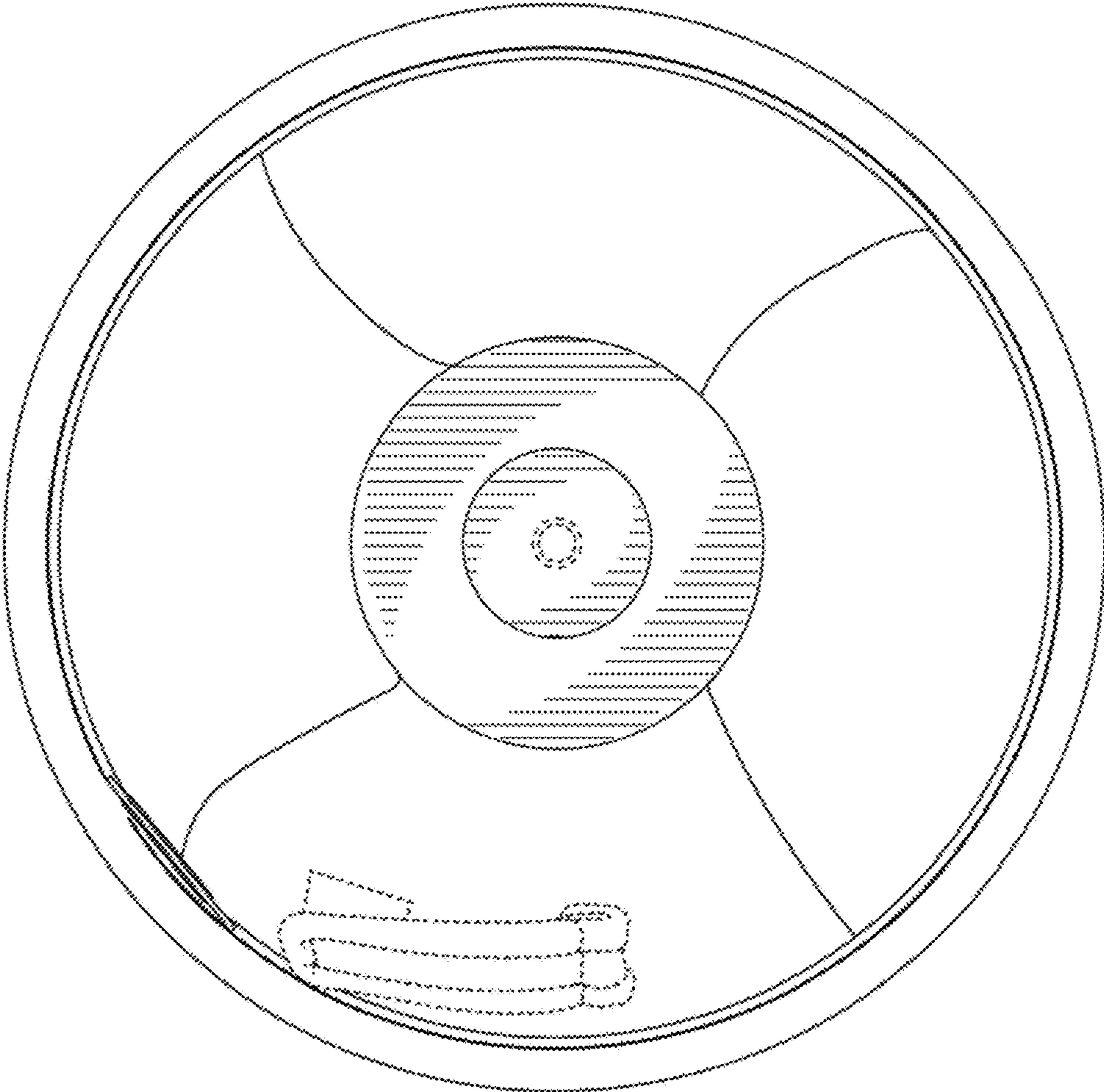


FIG. 6