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(12) United States Design Patent

Auer et al.

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(54) **HIGH-PERFORMANCE SEMICONDUCTOR MODULE**

(71) Applicant: **Infineon Technologies AG**, Neubiberg (DE)

(72) Inventors: **Thomas Auer**, Warstein (DE); **Andras Bertalan**, Warstein-Allagen (DE); **Jens Krugmann**, Paderborn (DE); **Christoph Messelke**, Arnsberg (DE)

(73) Assignee: **Infineon Technologies AG**, Neubiberg (DE)

(**) Term: **15 Years**

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(30) **Foreign Application Priority Data**

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(51) **LOC (11) Cl.** **13-03**

(52) **U.S. Cl.**

USPC **D13/182**

(58) **Field of Classification Search**

USPC D13/182; 257/678, 684, 690, 691; 361/679.01, 713, 728, 736, 760, 761, 772, 361/775, 783, 820; 174/250, 253; 438/15, 25, 26, 51, 55, 63, 64, 106

CPC . H01L 21/00; H01L 2224/42; H01L 2224/43; H01L 2021/00; H01L 2021/02; H01L 2021/04; H01L 21/4814; H01L 21/4846; H01L 21/4871; H01L 21/67144; H01L 23/02; H01L 23/13; H01L 23/14; H01L 23/147; H01L 2924/171; H01L 2924/1711; H01L 2924/1715; H01L 2924/17151; H01L 2924/181; H01L 2924/1811; H01L 2924/19042; H01L 2924/1905; H01L 2224/08054; H01L 23/85; H05B 41/14; H02B 6/4201; G02B 6/4256; G02B 6/4257; G02B 6/4261; G02B 6/4262; G02B 6/428; G02B 6/4281; H05K 1/14; H05K 1/141; H05K 1/142; H05K 1/144; H05K 1/18; H05K 1/181; H05K 1/182; H05K 1/026

See application file for complete search history.

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Primary Examiner — Elizabeth J Oswecki

(74) *Attorney, Agent, or Firm* — Murphy, Bilak & Homiller, PLLC

(57) **CLAIM**

The ornamental design for a high-performance semiconductor module, as shown and described.

DESCRIPTION

FIG. **1** is a top, front and right side perspective view of a high-performance semiconductor module showing our new design;

FIG. **2** is a bottom plan view thereof;

FIG. **3** is a front side elevational view thereof;

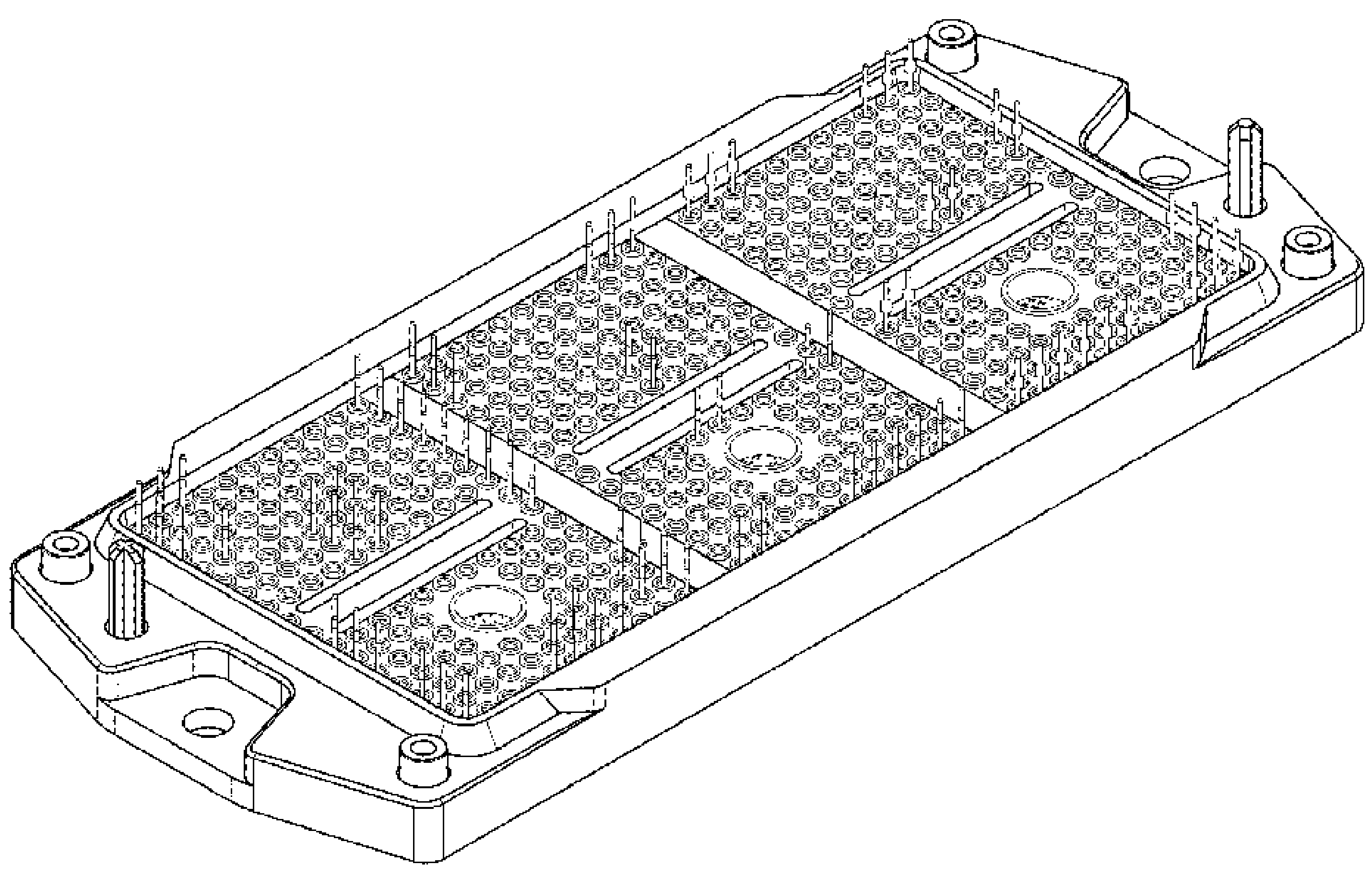
FIG. **4** is a right side elevational view thereof; and,

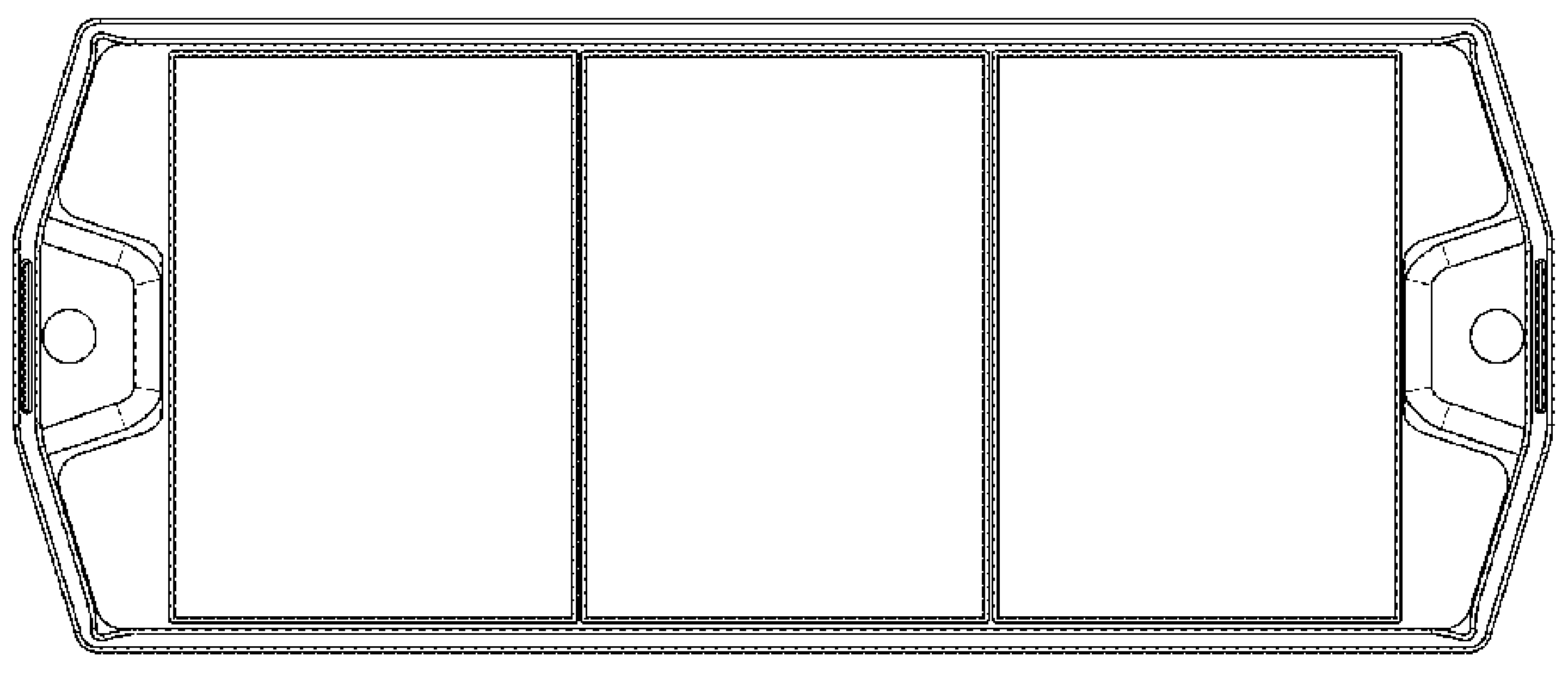
FIG. **5** is a top plan view thereof.

The broken line portions of the figure drawings are included to show portions of the article that form no part of the claimed design.

All surfaces not shown form no part of the claimed design.

1 Claim, 5 Drawing Sheets





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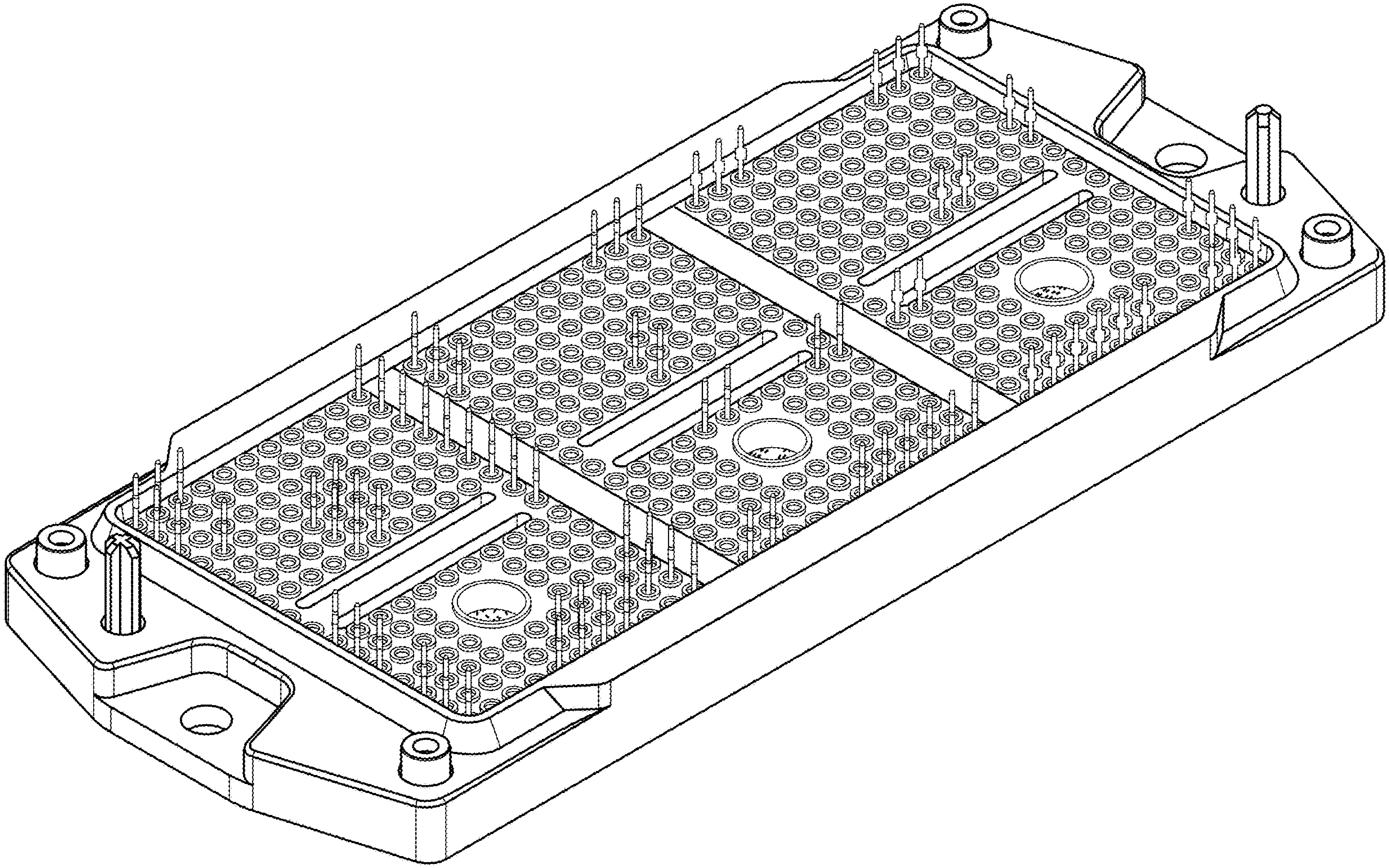

FIG. 1

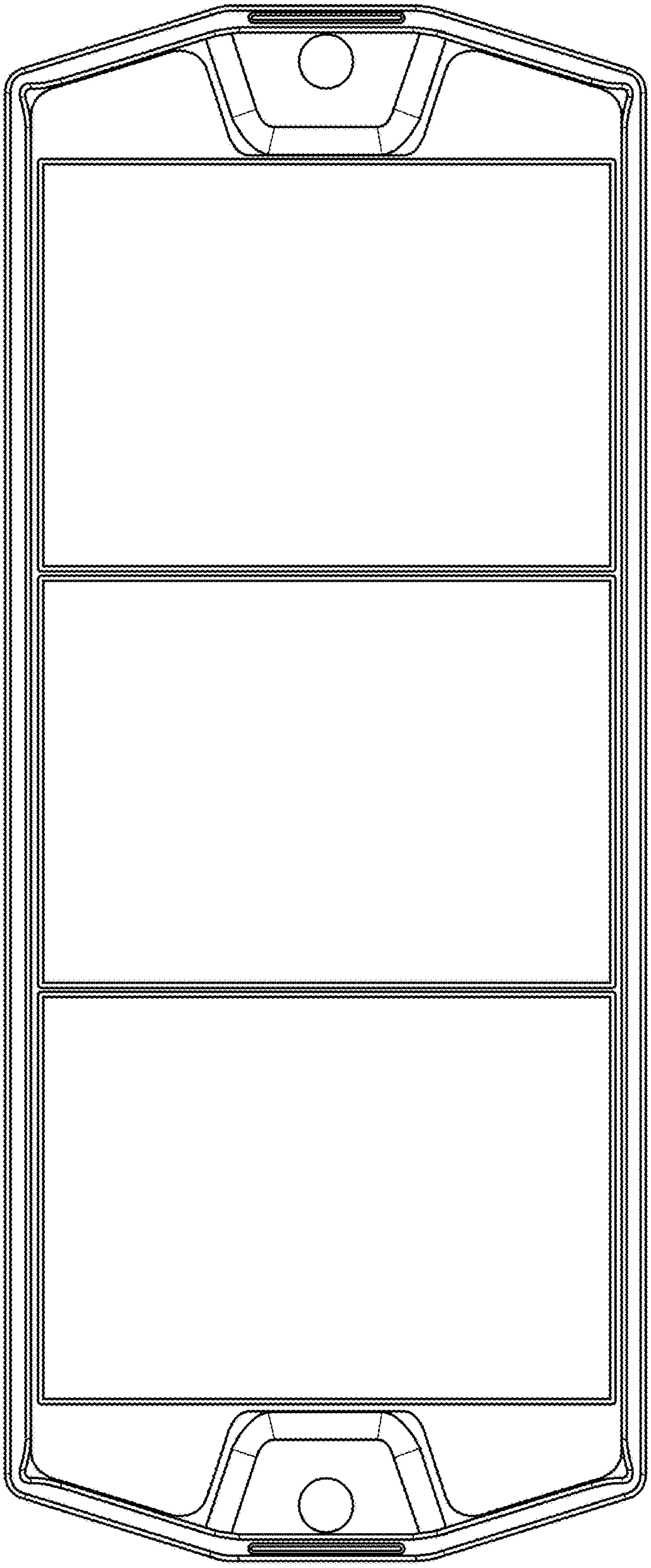

FIG. 2

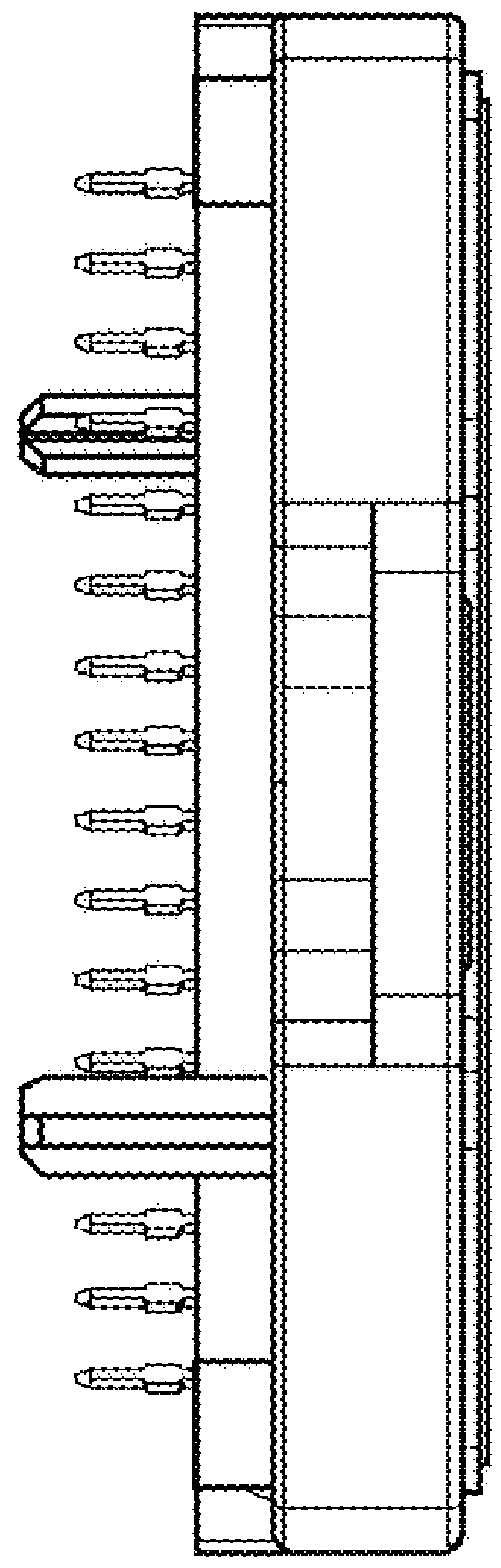

FIG. 3

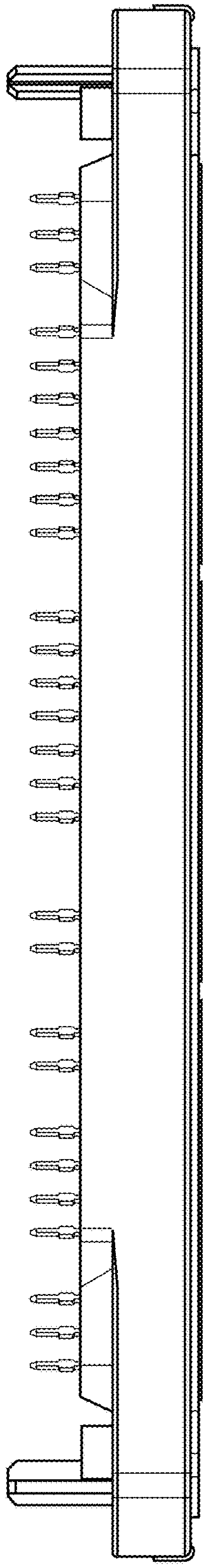

FIG. 4

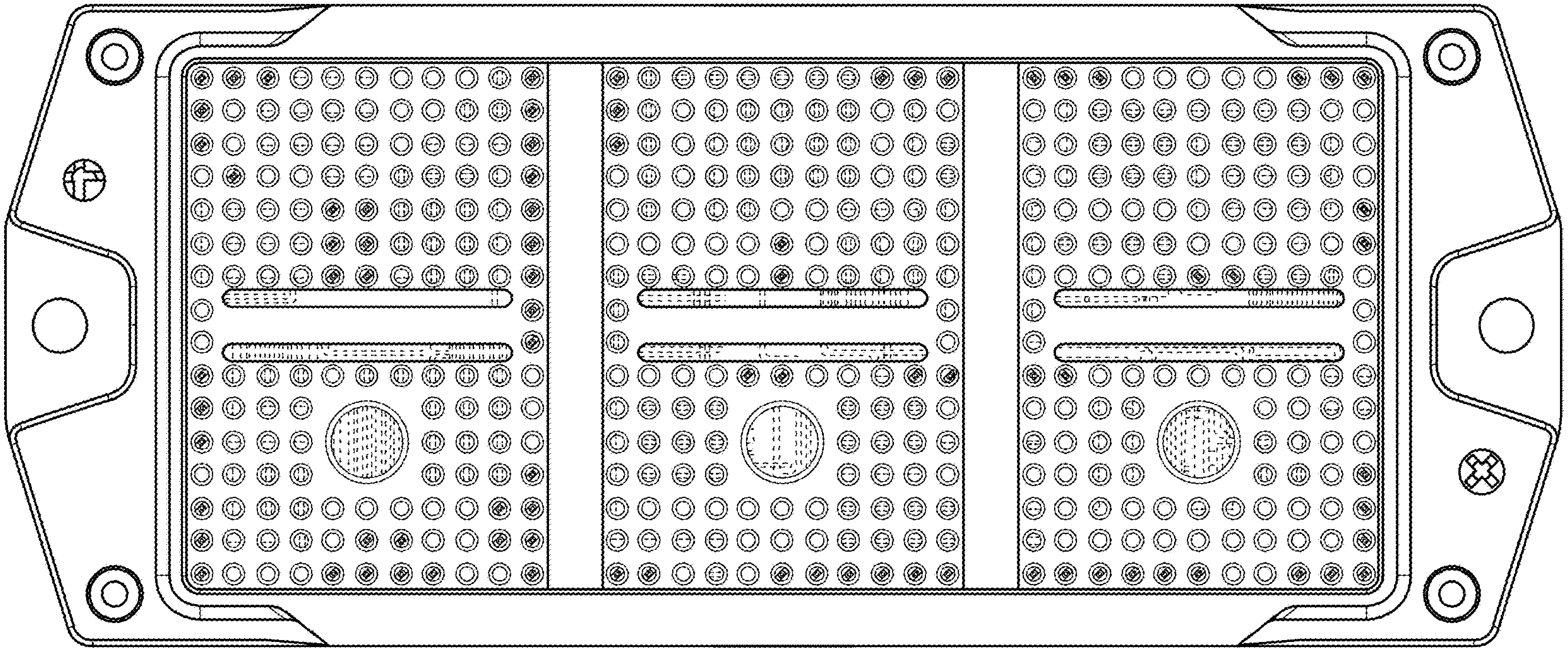

FIG. 5