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(12) **United States Design Patent**
Yamaki et al.

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(54) **ELASTIC MEMBRANE FOR SEMICONDUCTOR WAFER POLISHING**

(71) Applicant: **EBARA CORPORATION**, Tokyo (JP)

(72) Inventors: **Satoru Yamaki**, Tokyo (JP); **Makoto Fukushima**, Tokyo (JP); **Keisuke Namiki**, Tokyo (JP); **Osamu Nabeya**, Tokyo (JP); **Shingo Togashi**, Tokyo (JP); **Tomoko Owada**, Tokyo (JP); **Masahiko Kishimoto**, Tokyo (JP)

(73) Assignee: **EBARA CORPORATION**, Tokyo (JP)

(**) Term: **15 Years**

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Dec. 12, 2016	(JP)	2016-026914
Dec. 12, 2016	(JP)	2016-026915

(51) **LOC (11) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182; 451/66, 288, 289
CPC B24B 37/30; B24B 41/061; B24B 49/16
See application file for complete search history.

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Primary Examiner — Elizabeth J Oswecki
(74) *Attorney, Agent, or Firm* — Pearne & Gordon LLP

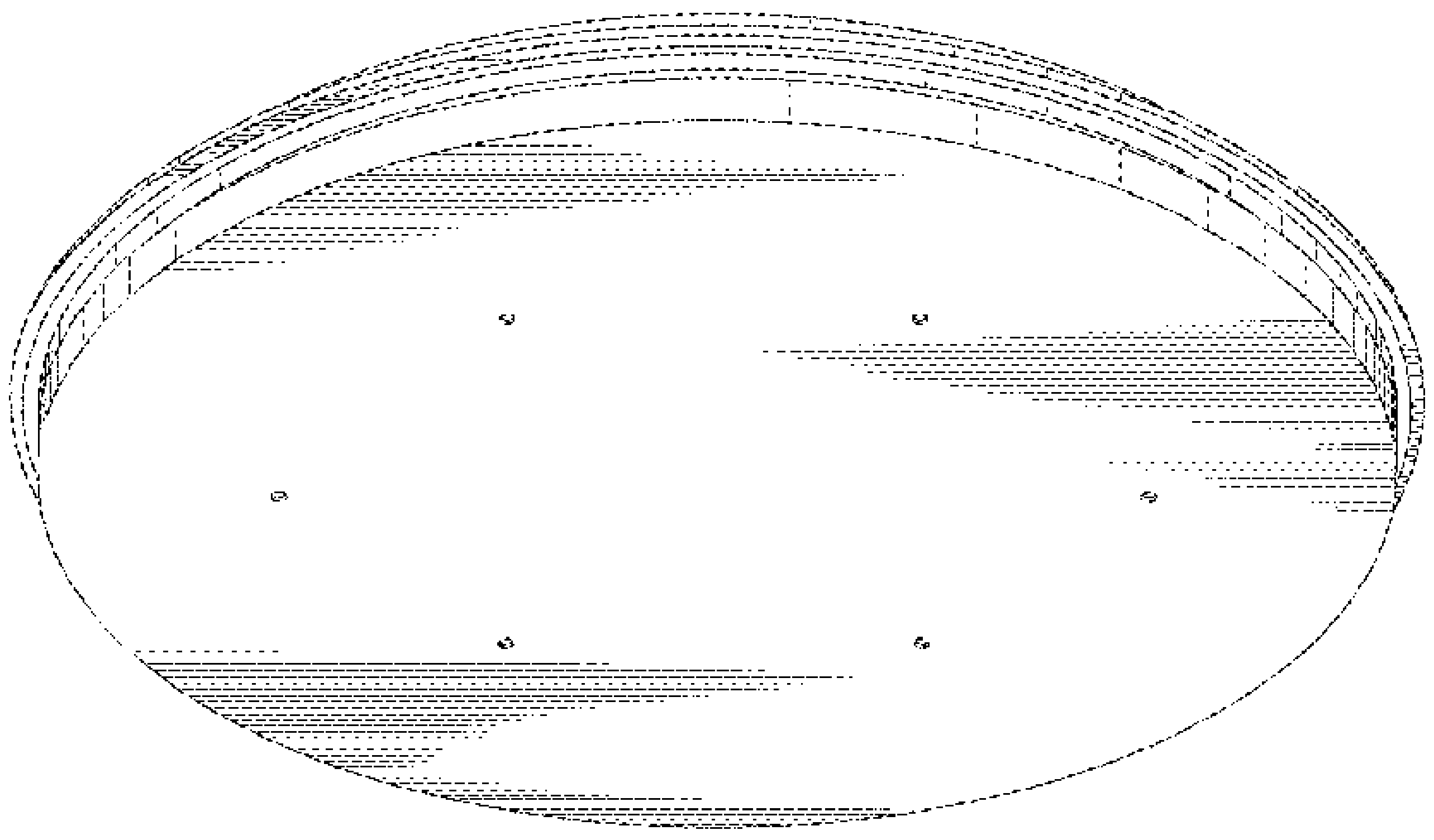
(57) **CLAIM**

The ornamental design for an elastic membrane for semiconductor wafer polishing, as shown and described.

DESCRIPTION

FIG. **1** is a bottom perspective view of an elastic membrane for semiconductor wafer polishing showing our new design;
FIG. **2** is a top perspective view thereof;
FIG. **3** is a bottom view thereof;
FIG. **4** is a top view thereof;
FIG. **5** is a front view thereof, a rear view being identical thereto;
FIG. **6** is a right-side view thereof, a left-side view being identical thereto;
FIG. **7** is a cross-sectional view taken along line **7**-**7** of FIG. **4**; and,
FIG. **8** is an enlarged portion view labeled FIG. **8** in FIG. **7**. The dash-dot lines in FIG. **7** represent the boundary line of the enlarged portion view shown in FIG. **8**.

1 Claim, 6 Drawing Sheets



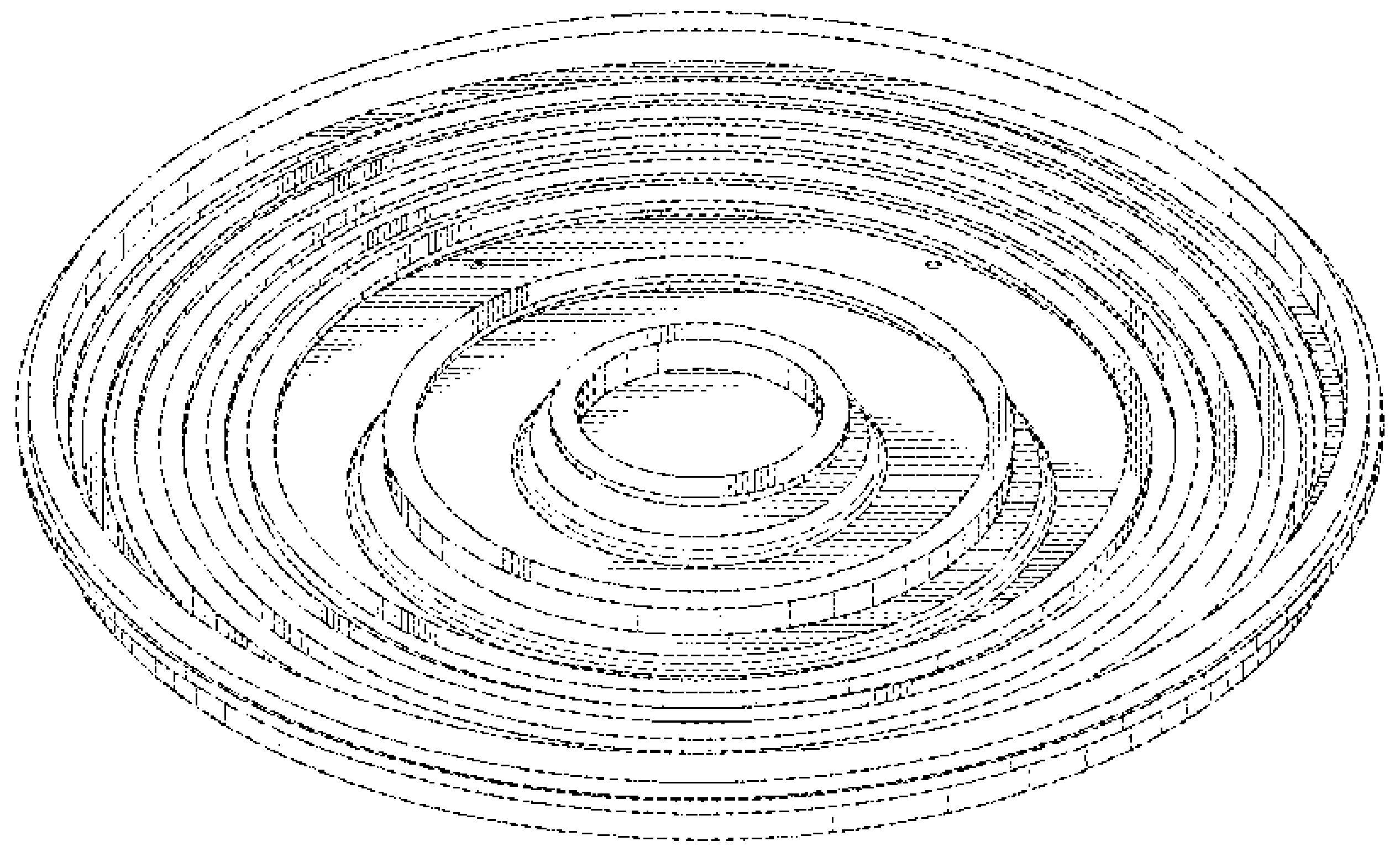


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FIG. 1

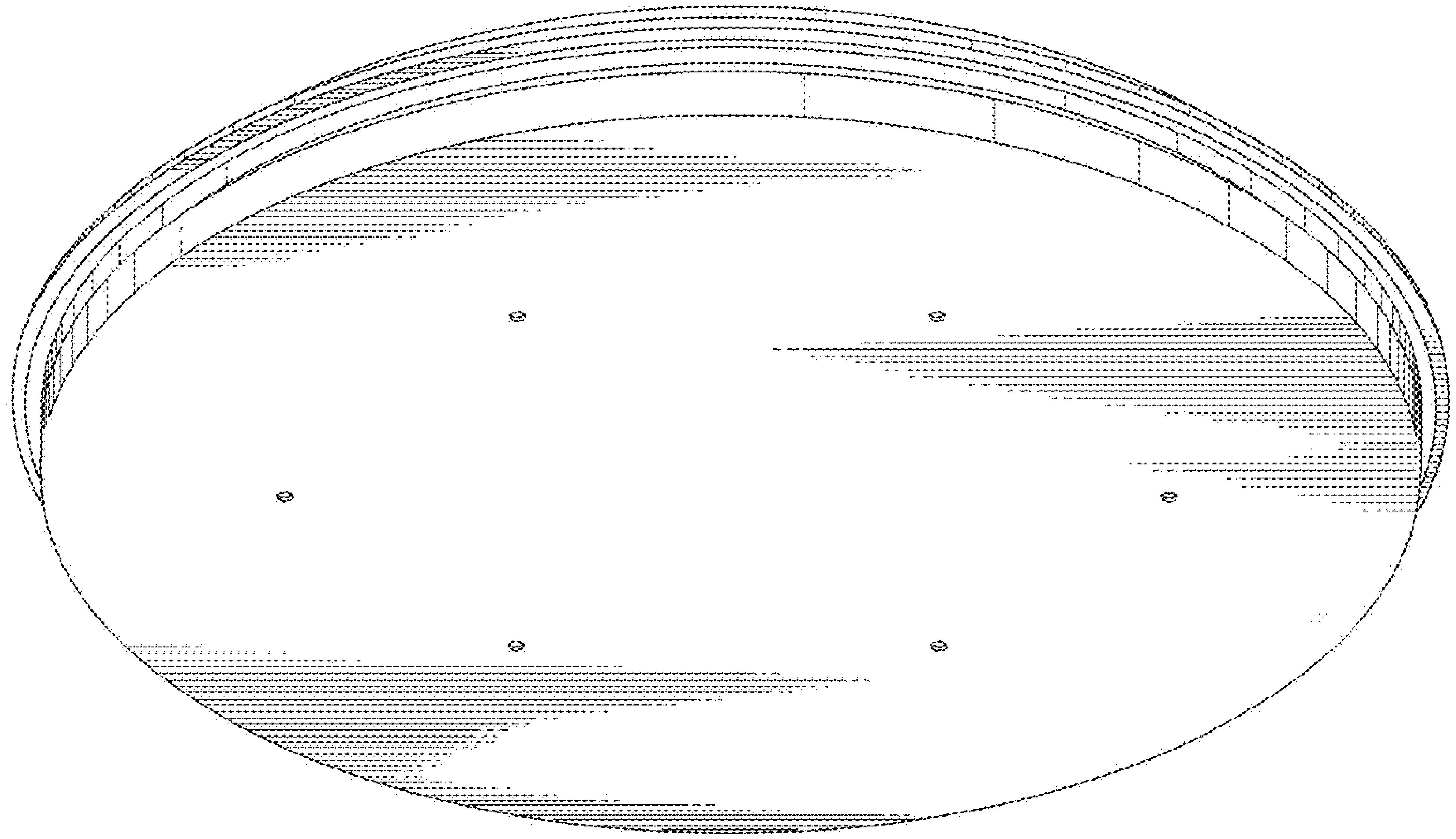

FIG. 2

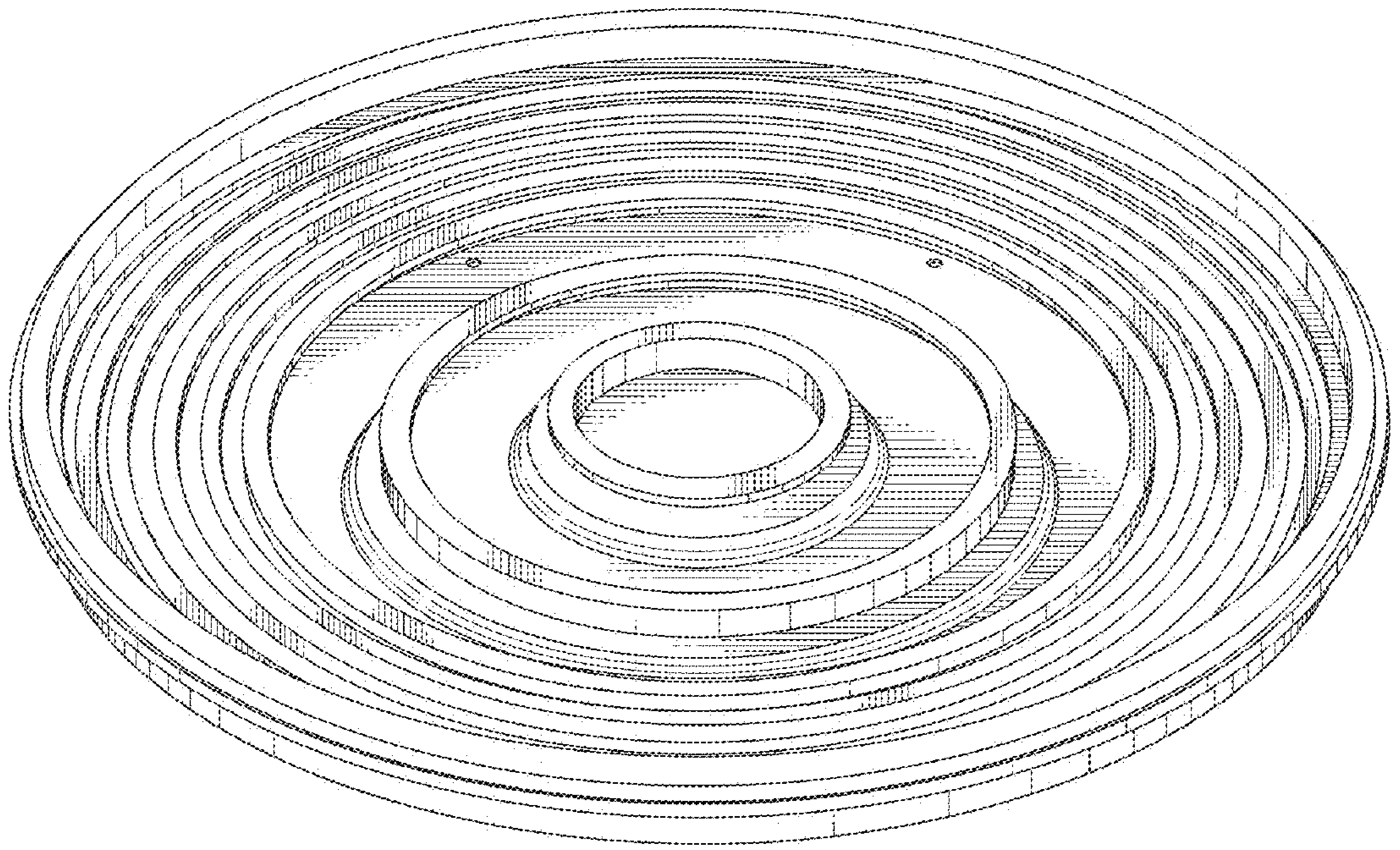

FIG. 3

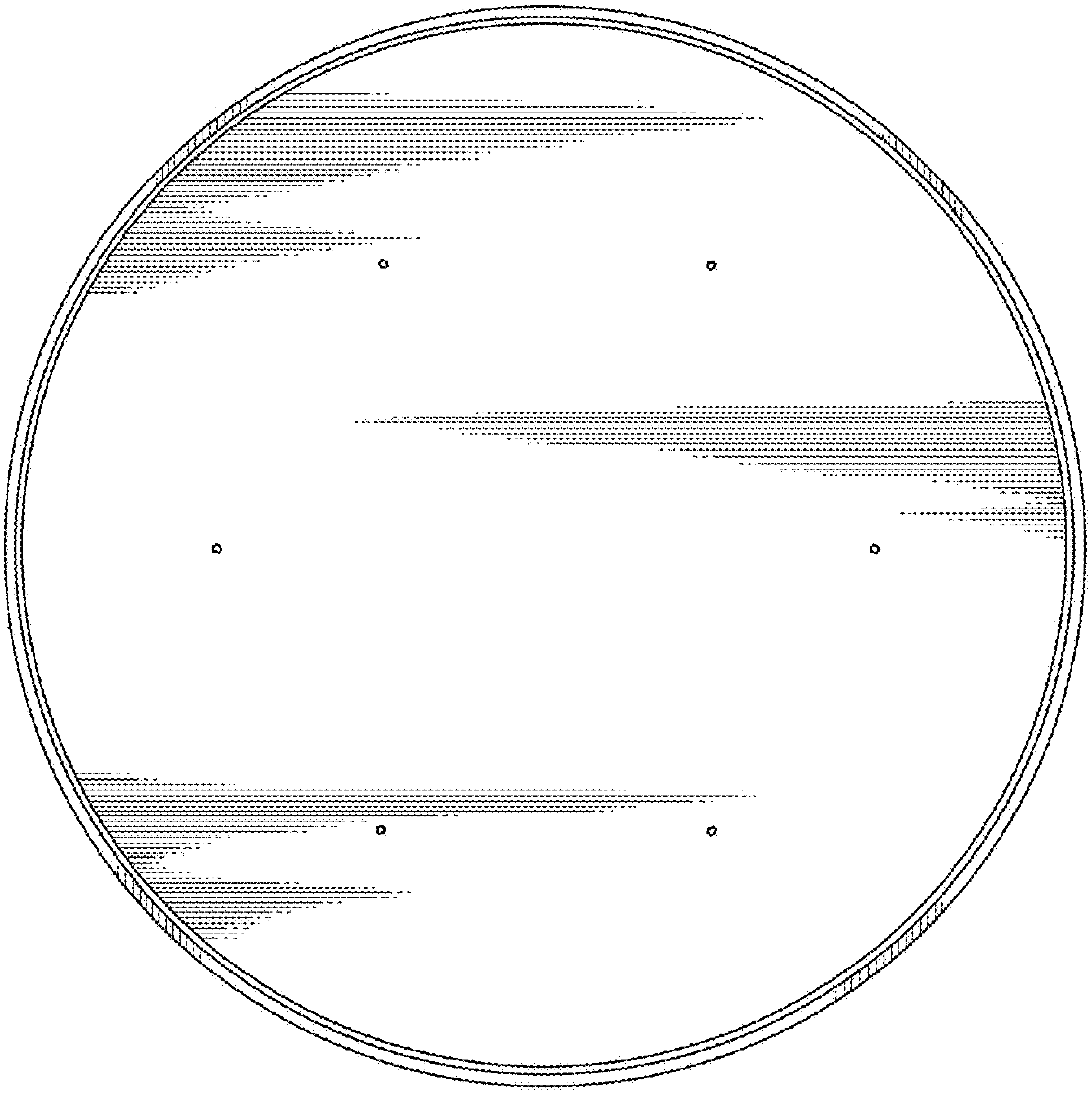

FIG. 4

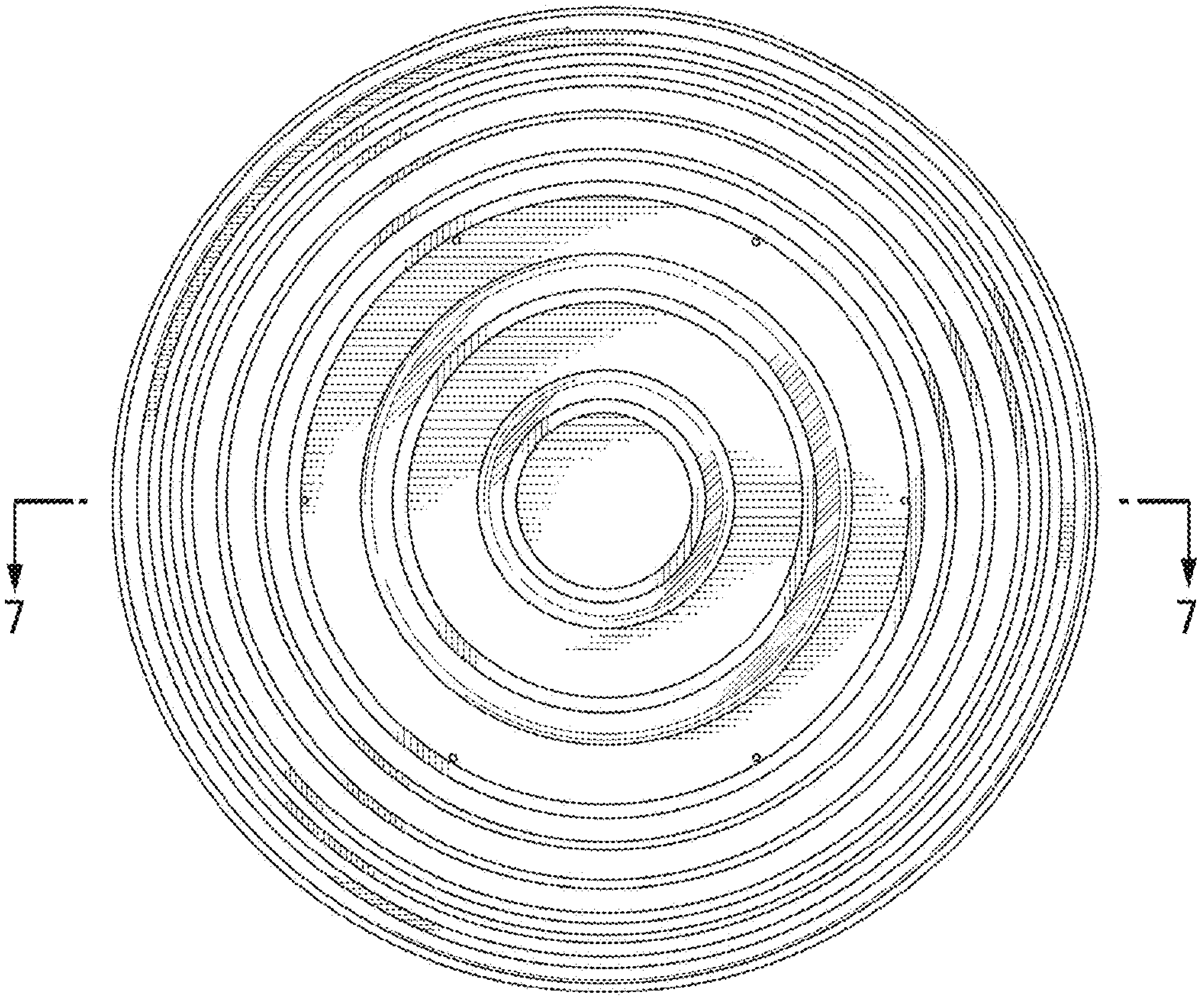

FIG. 5

FIG. 6

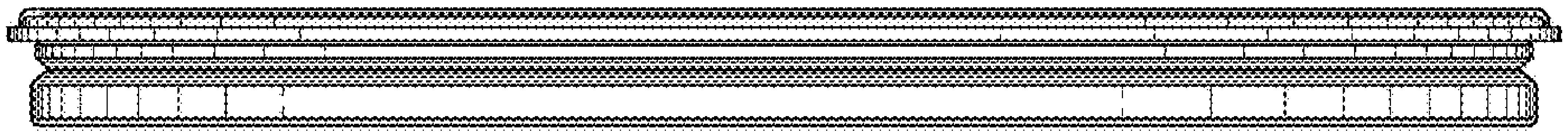

FIG. 7

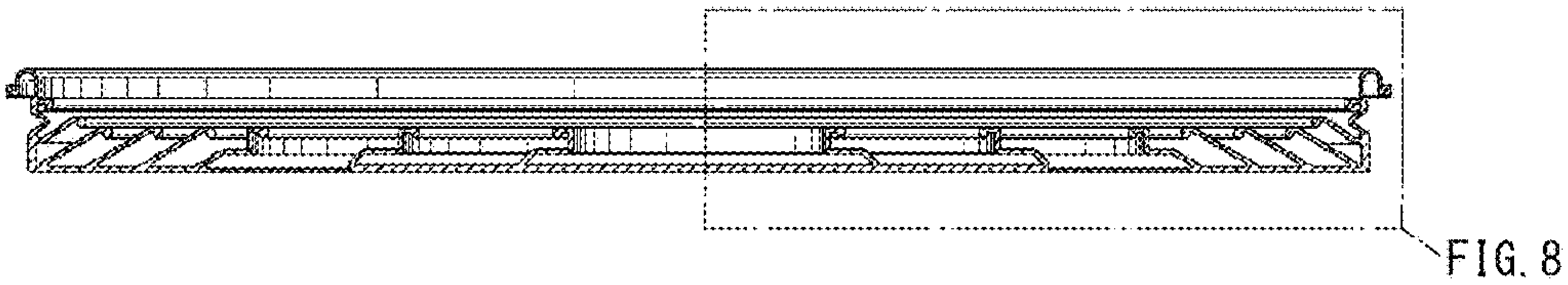

FIG. 8