

US00D834545S

(12) **United States Design Patent** (10) **Patent No.:** **US D834,545 S**  
**Kurz** (45) **Date of Patent:** **\*\* Nov. 27, 2018**

(54) **SEMICONDUCTOR MODULE** 7,397,668 B2 \* 7/2008 Sekine ..... H05K 7/1465  
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(71) Applicant: **Infineon Technologies AG**, Neubiberg D621,351 S \* 8/2010 Huang ..... D13/110  
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(\*\*) Term: **15 Years** 2012/0109343 A1 \* 5/2012 Shah ..... G05B 19/409  
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(21) Appl. No.: **29/541,146**

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(30) **Foreign Application Priority Data**

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(51) **LOC (11) Cl.** ..... **13-03**

(52) **U.S. Cl.**  
USPC ..... **D13/182**; D13/158

(58) **Field of Classification Search**  
USPC ..... D13/101, 110, 118, 123, 158–162, 173,  
D13/182, 184, 199  
CPC . G05B 15/00; H01H 9/00; H01H 9/02; H01H  
9/22; H01H 13/00; H01L 23/48; H01L  
23/49; H01L 23/52; H01L 25/07; H01R  
13/00; H01R 13/60; H02B 1/00  
See application file for complete search history.

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(57) **CLAIM**

The ornamental design for a semiconductor module, as shown and described.

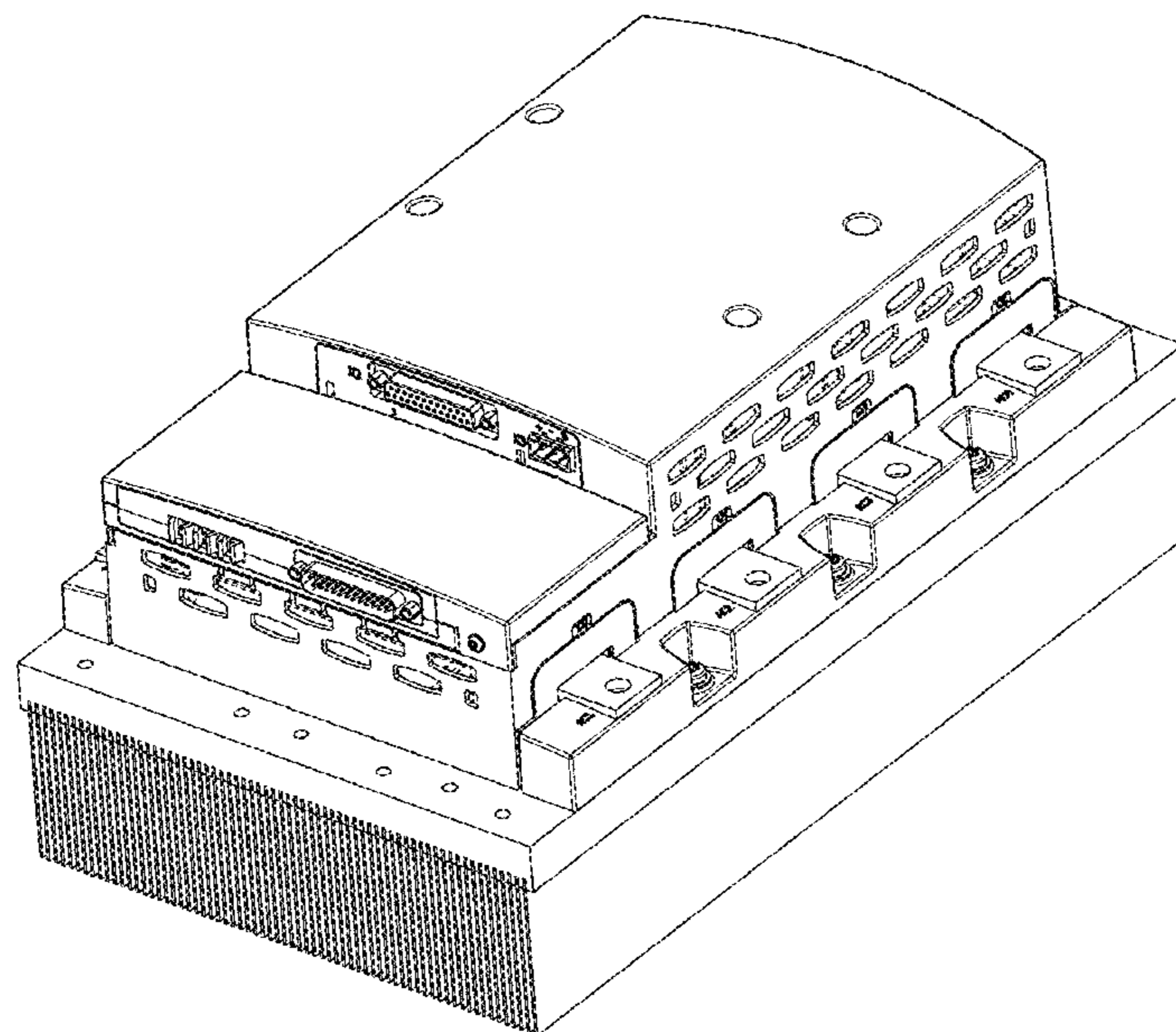
**DESCRIPTION**

FIG. 1 is a top, front and right side perspective view of the semiconductor module showing my new design; FIG. 2 is a back side elevational view thereof; FIG. 3 is a front side elevational view thereof; FIG. 4 is a left side elevational view thereof; FIG. 5 is a right side elevational view thereof; and, FIG. 6 is a top plan view thereof.

The broken line portion of the figure drawings is included to show portions of the article that form no part of the claimed design.

All surfaces not shown form no part of the claimed design.

**1 Claim, 6 Drawing Sheets**



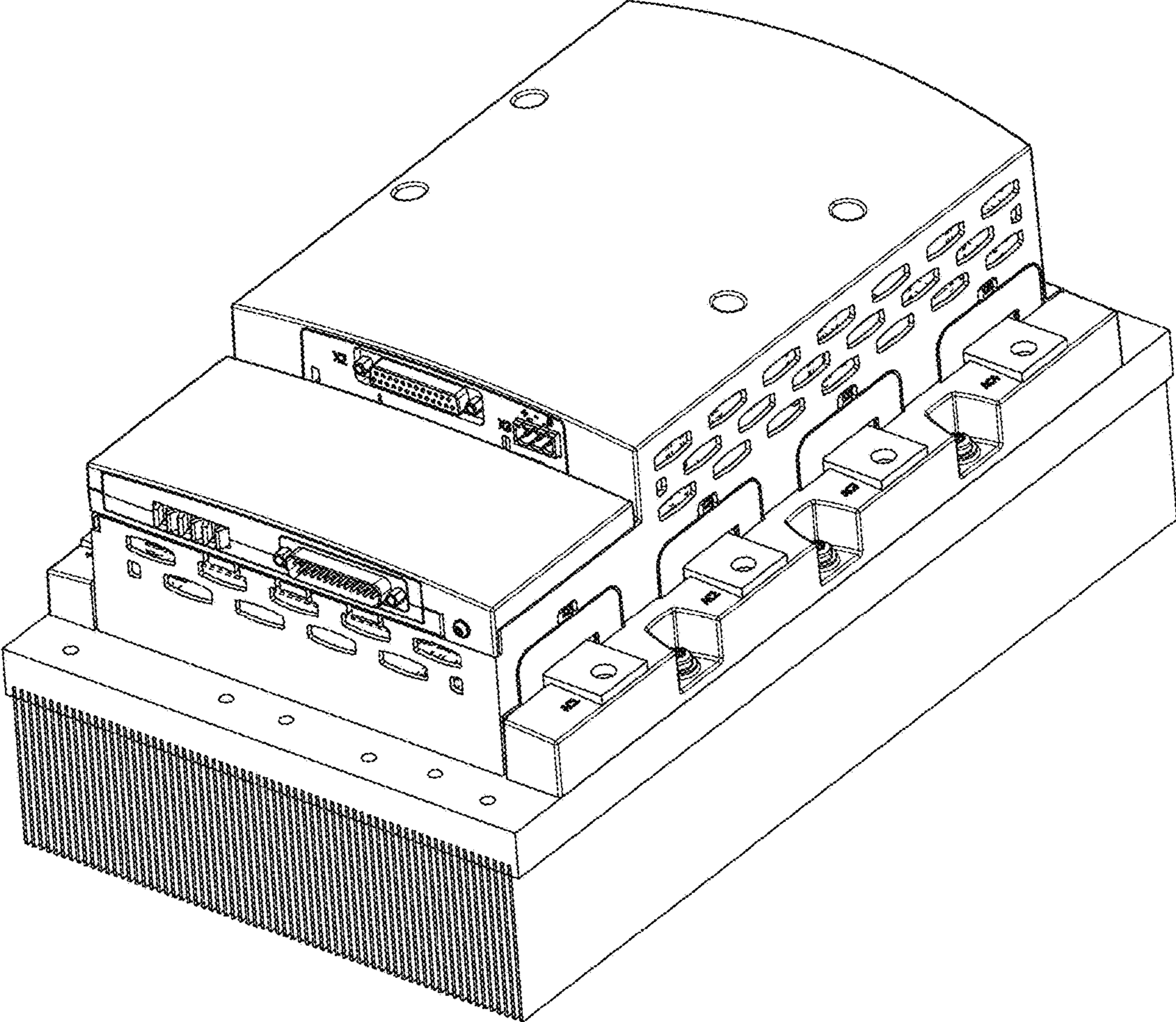


FIG. 1



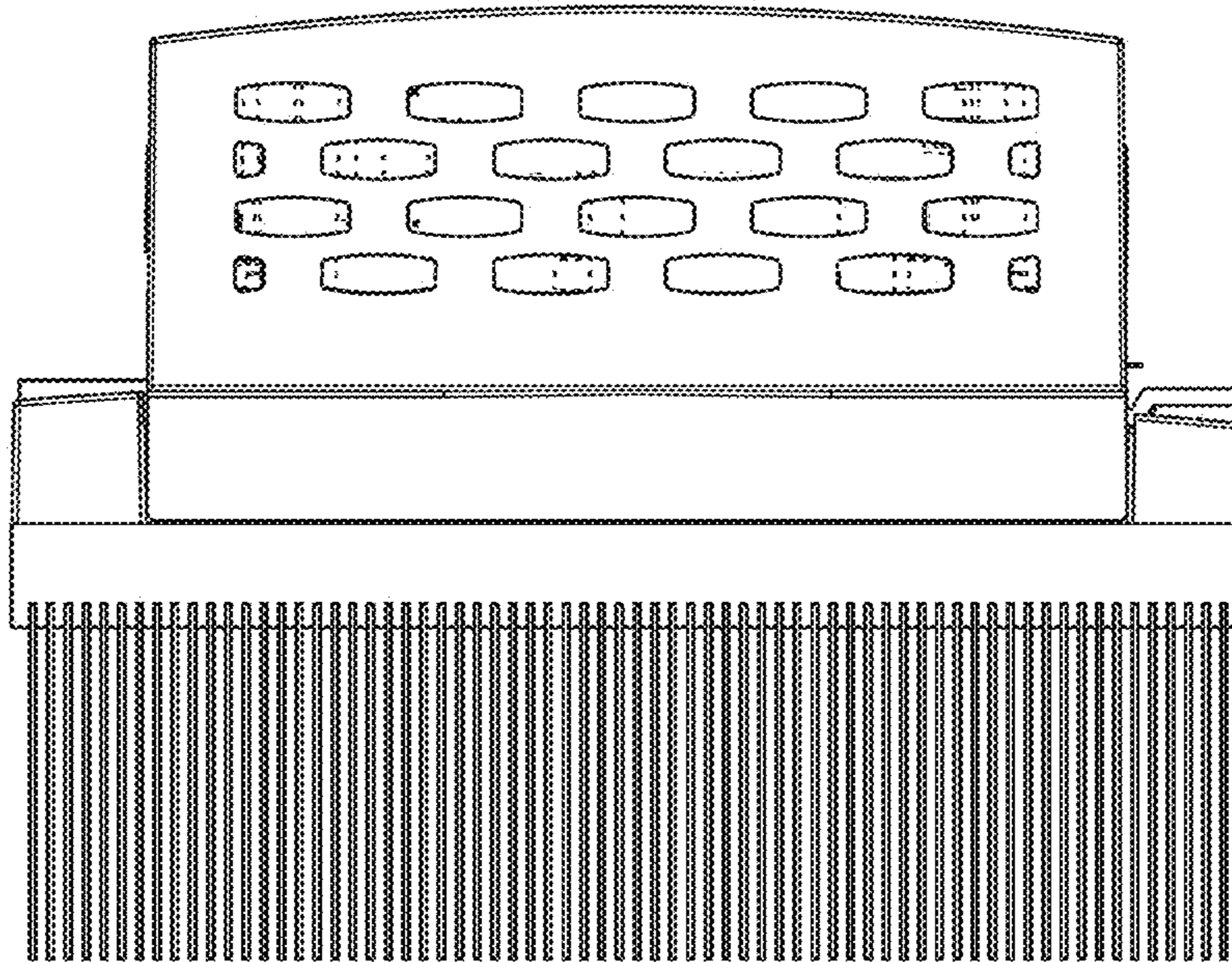


FIG. 2

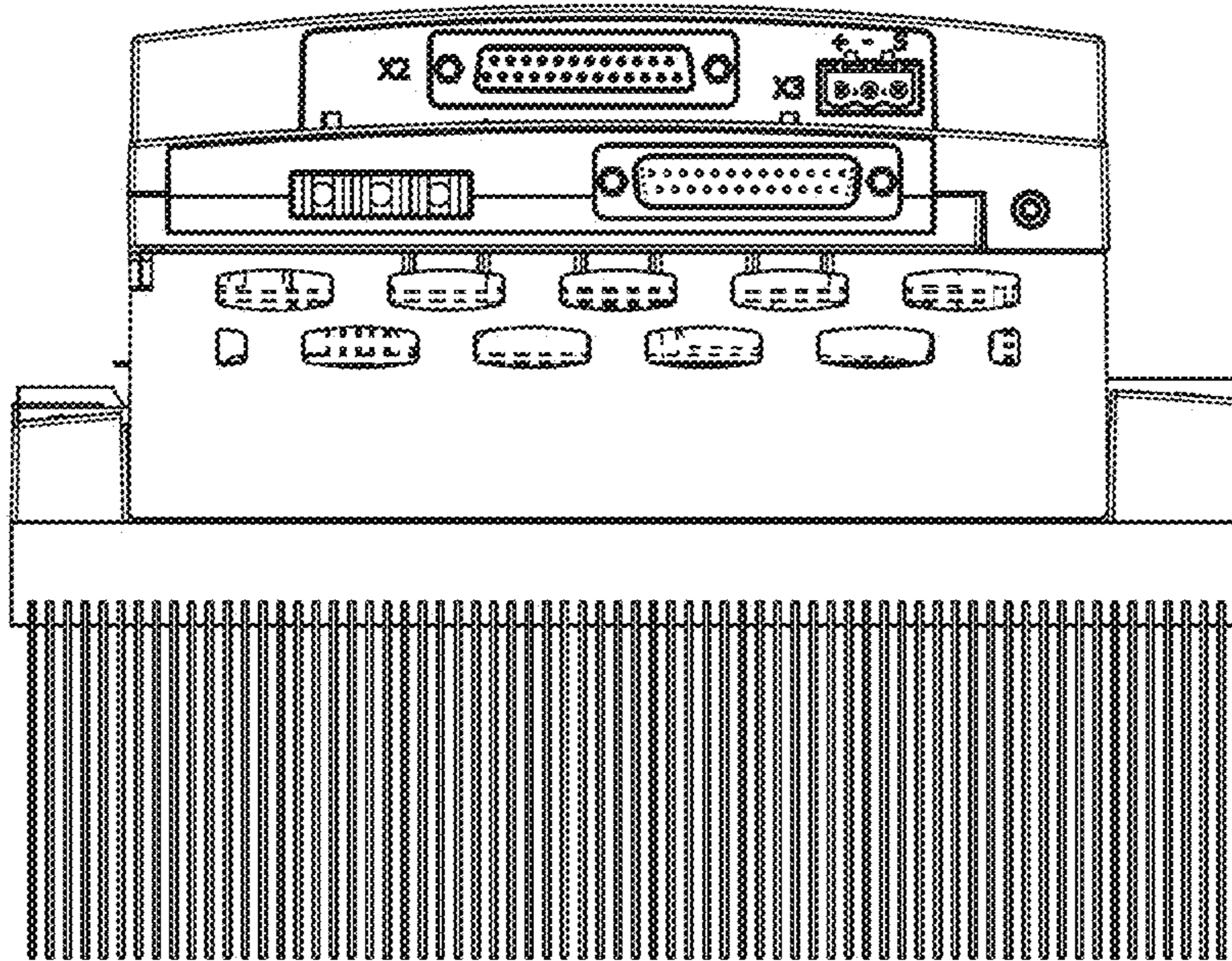


FIG. 3

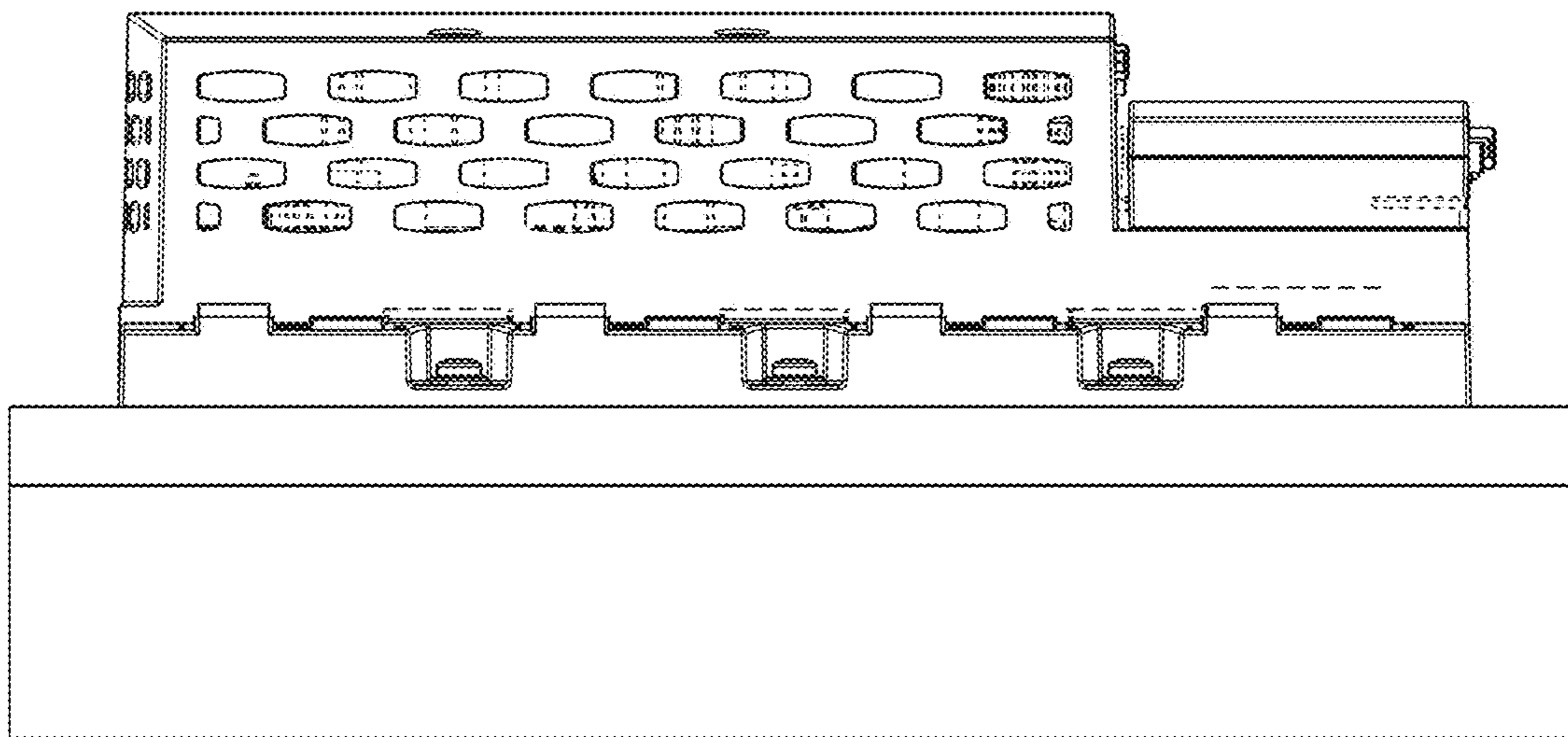


FIG. 4

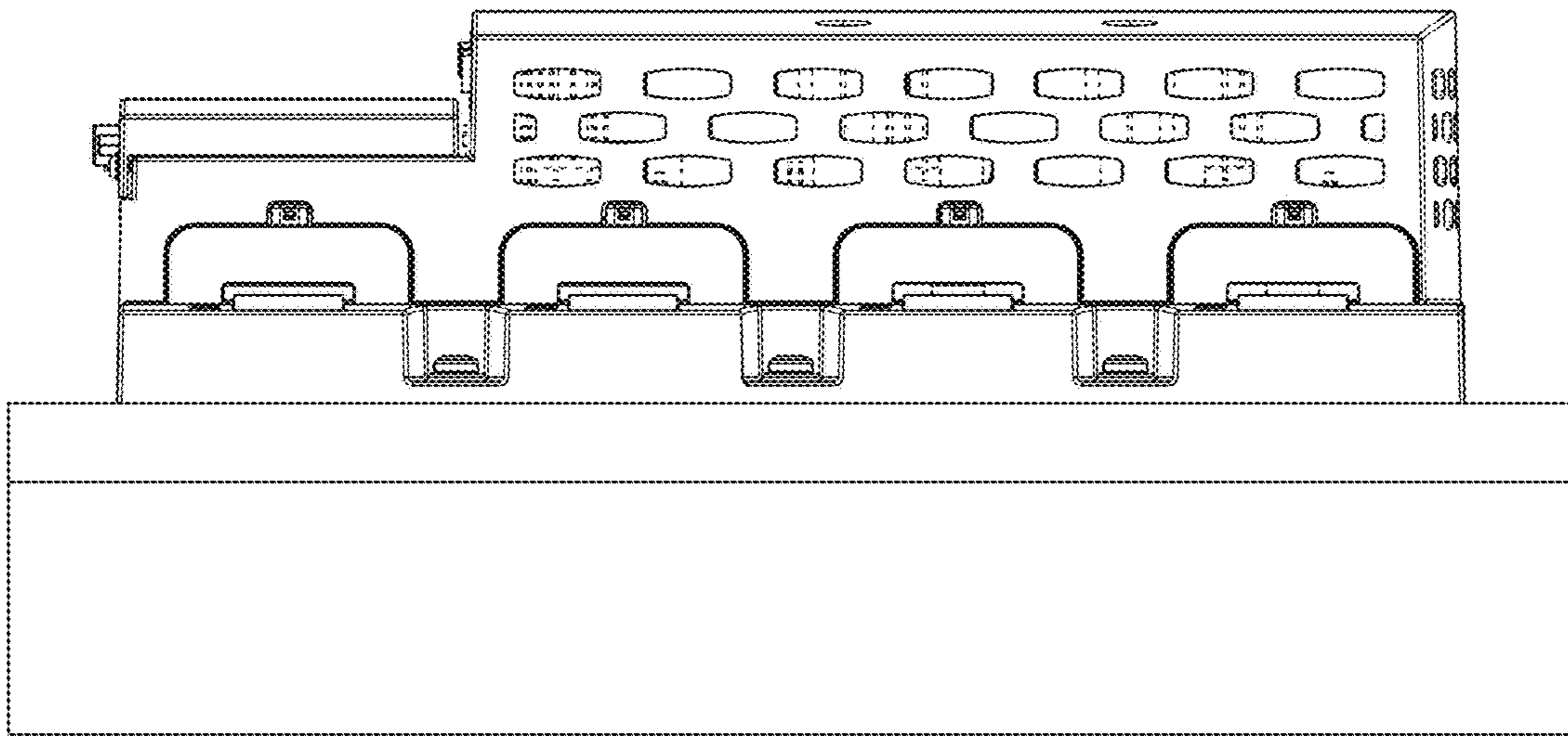


FIG. 5

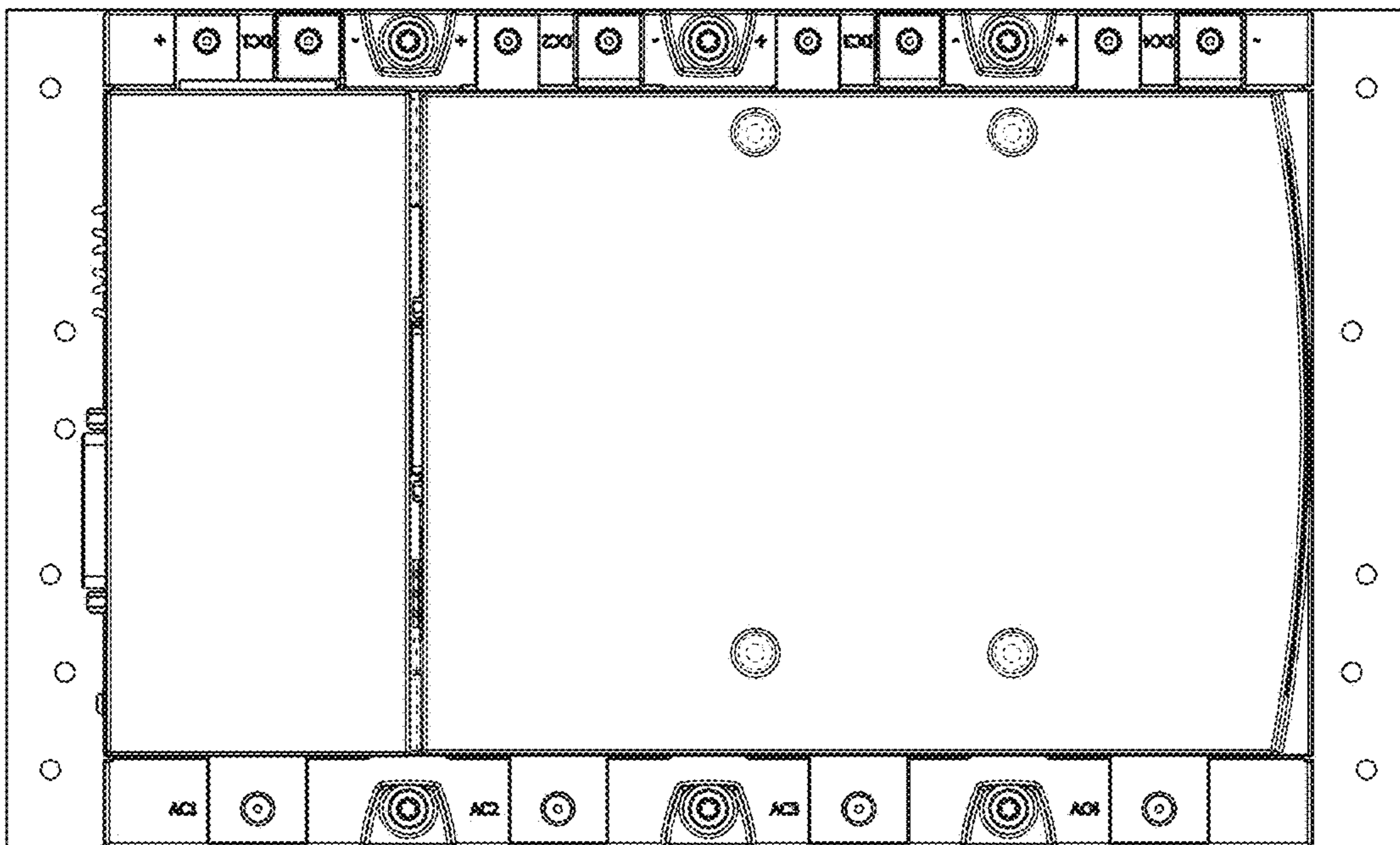


FIG. 6