



US00D827590S

(12) **United States Design Patent** (10) **Patent No.:** **US D827,590 S**
Hayashida et al. (45) **Date of Patent:** **** Sep. 4, 2018**

(54) **POWER SEMICONDUCTOR DEVICE**

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(**) Term: **15 Years**

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(30) **Foreign Application Priority Data**

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(51) **LOC (11) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182; D13/147**

(58) **Field of Classification Search**
USPC D13/133, 146, 147, 154, 155, 182, 184, D13/199
CPC H01L 21/0405; H01L 21/18; H01L 21/48; H01L 23/13; H01L 23/498; H01L 23/66; H01L 25/03; H01L 29/045; H01L 29/06; H01L 29/1608; H01L 29/63; H01L 29/872; H05K 3/34; H05K 9/00; H04B 10/02

See application file for complete search history.

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(57) **CLAIM**

The ornamental design for the power semiconductor device, as shown and described.

DESCRIPTION

FIG. 1 is a perspective view of the front, left and bottom sides of a power semiconductor device showing our new design;

FIG. 2 is a perspective view of the front, right and top sides thereof;

FIG. 3 is a front view thereof;

FIG. 4 is a rear view thereof;

FIG. 5 is a left side view thereof;

FIG. 6 is a right side view thereof;

FIG. 7 is a top view thereof;

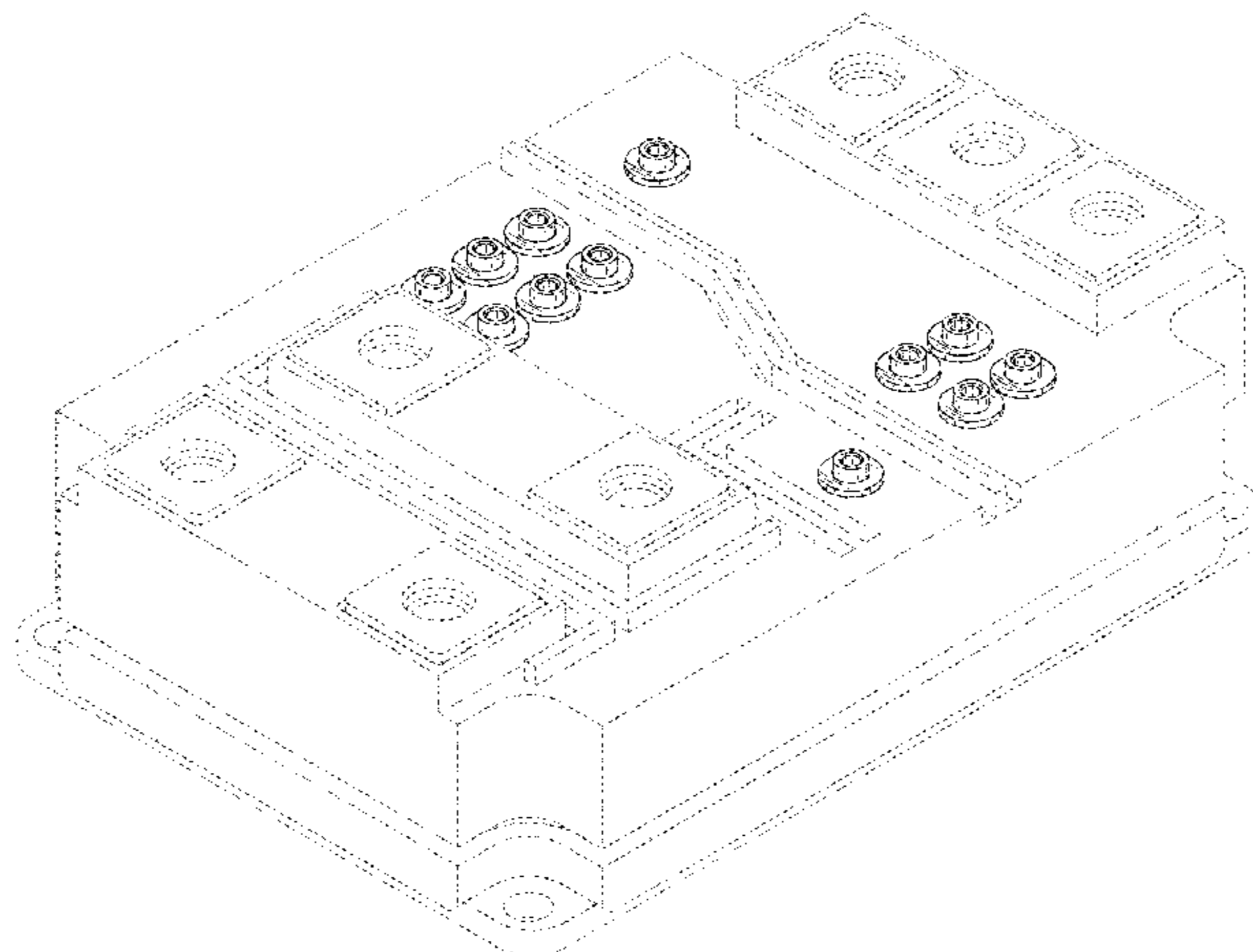
FIG. 8 is a bottom view thereof;

FIG. 9 is an end view of cutting part at 9-9, with omitting the interior mechanism thereof; and,

FIG. 10 is an end view of cutting part at 10-10, with omitting the interior mechanism thereof.

The broken line showing of unclaimed portion of the power semiconductor device is for the purpose of illustrating environmental structure only and forms no part of the claimed design.

1 Claim, 9 Drawing Sheets



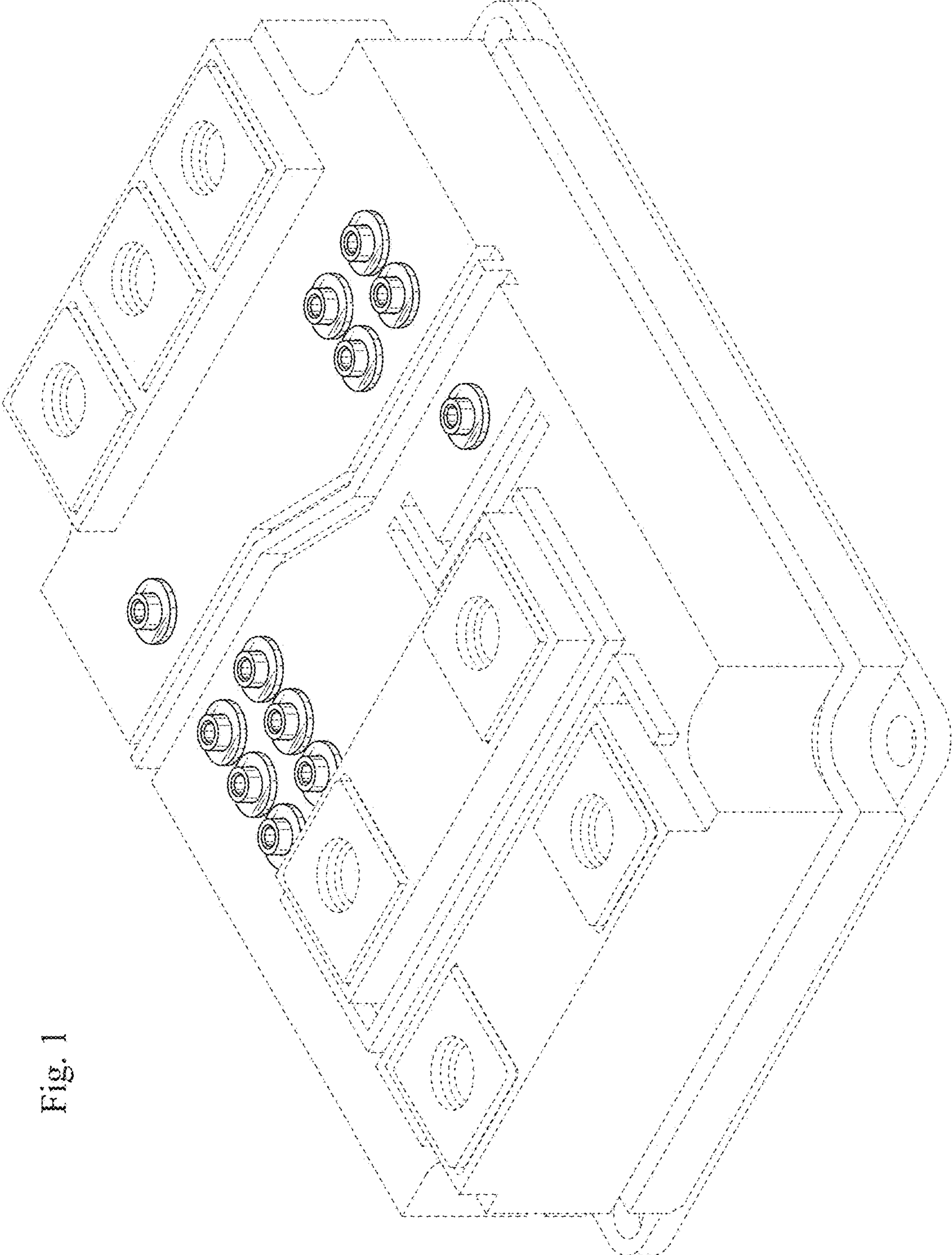


Fig. 1

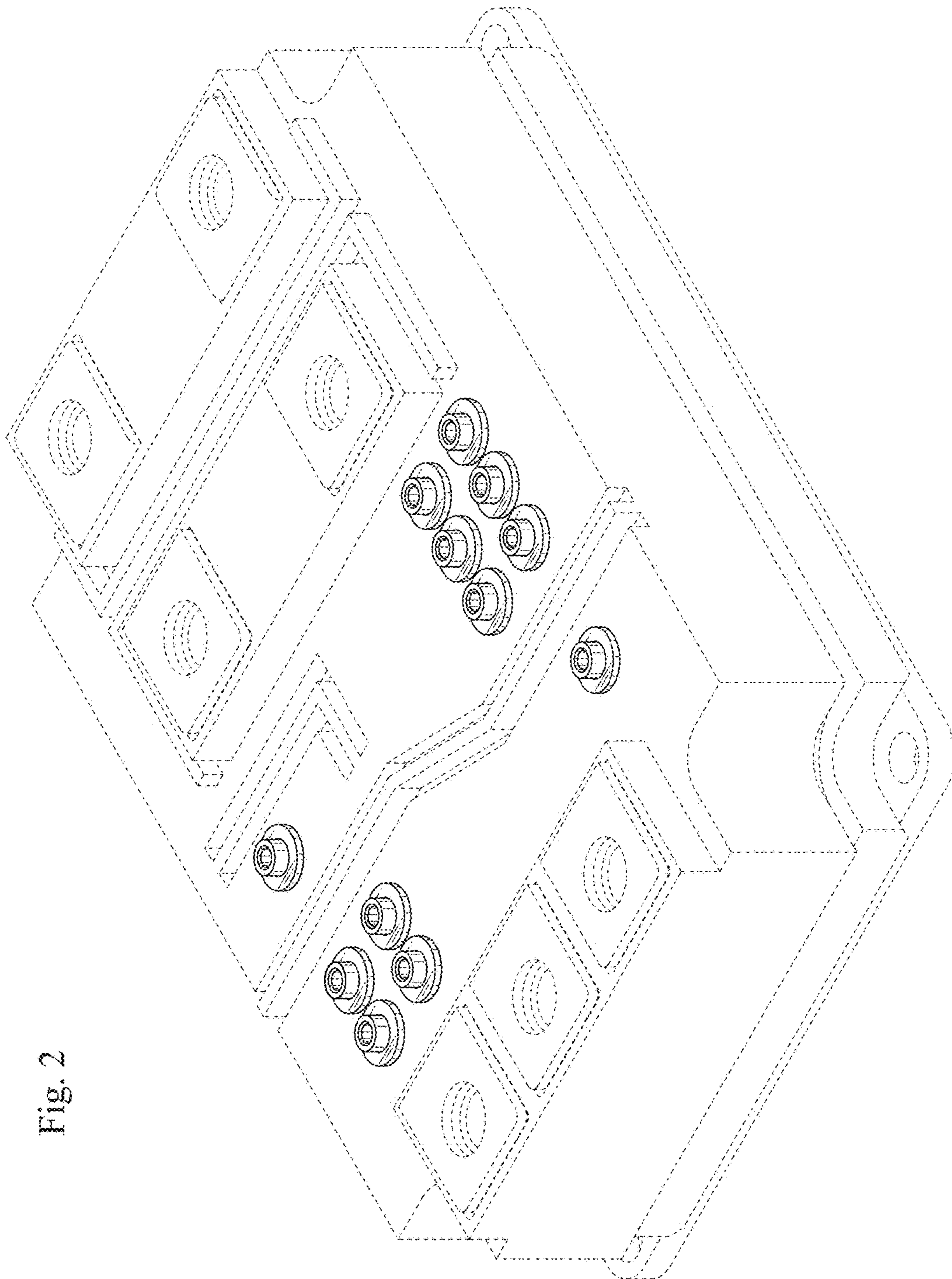


Fig. 2

Fig. 3

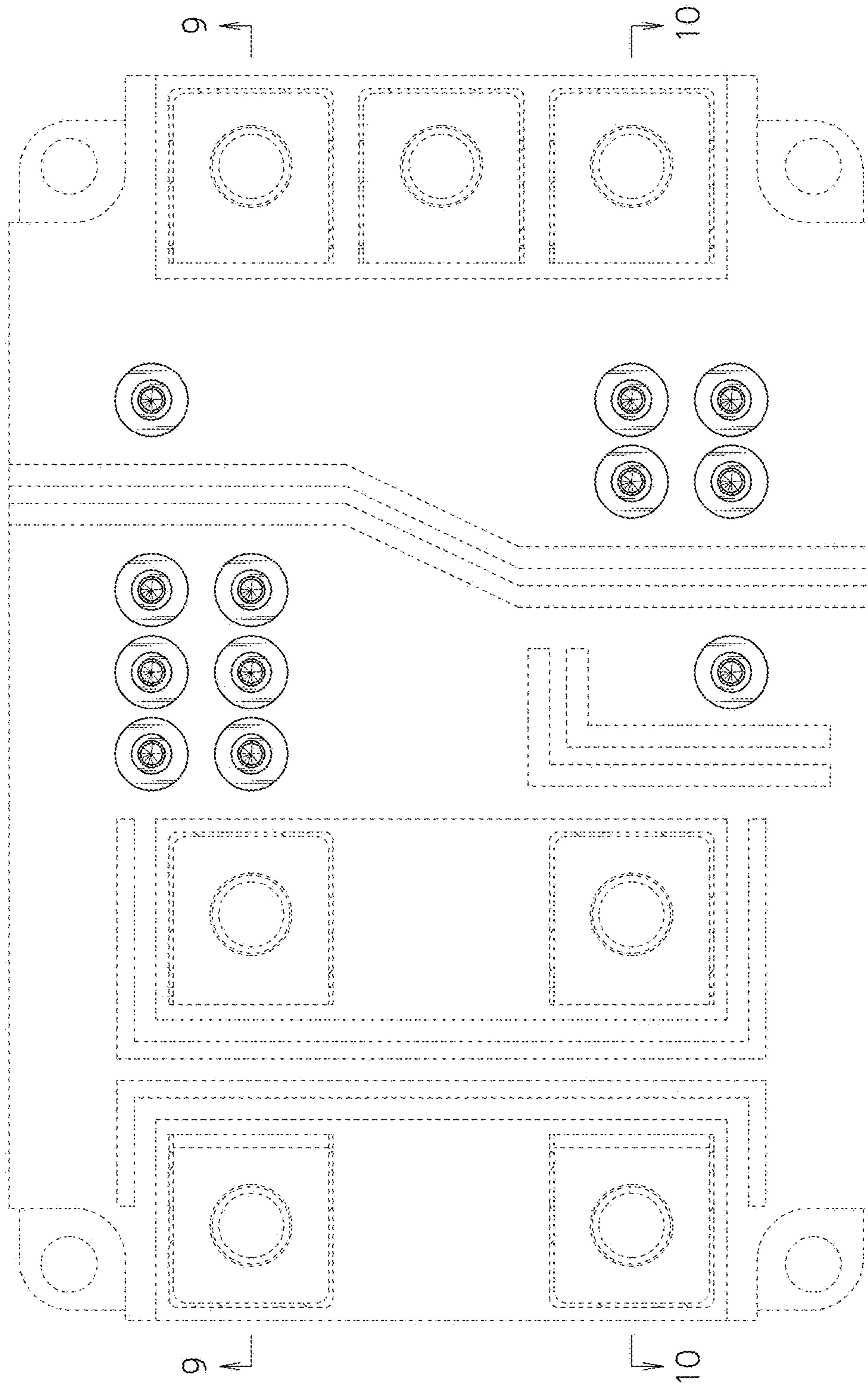


Fig. 4

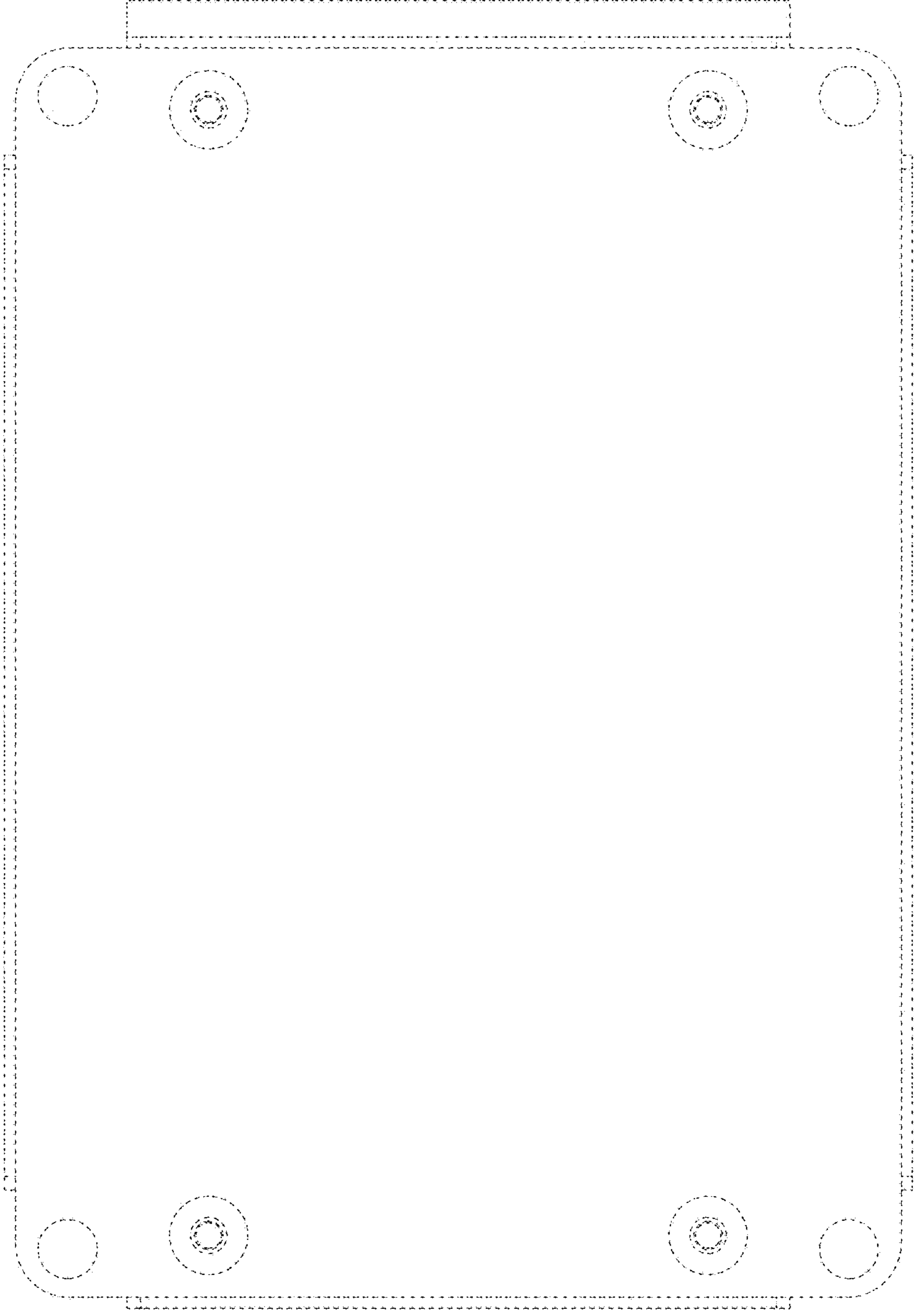


Fig. 6

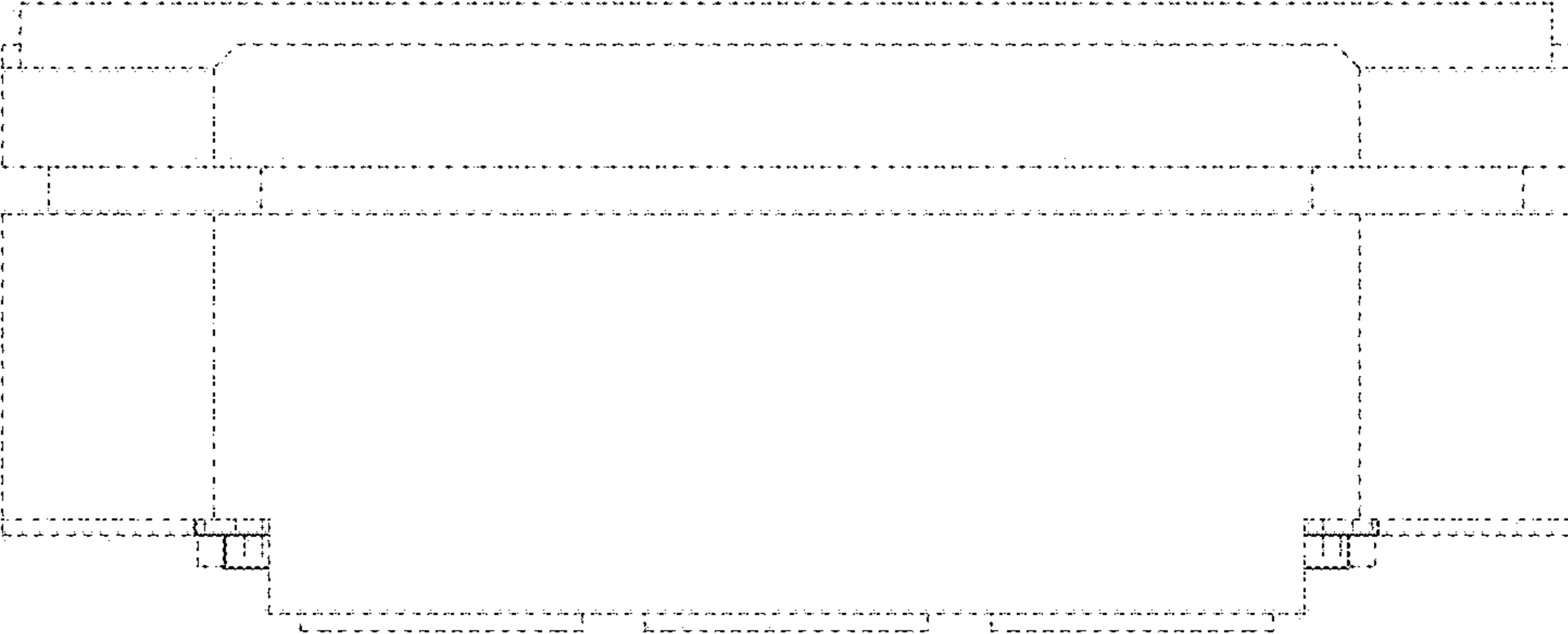


Fig. 5

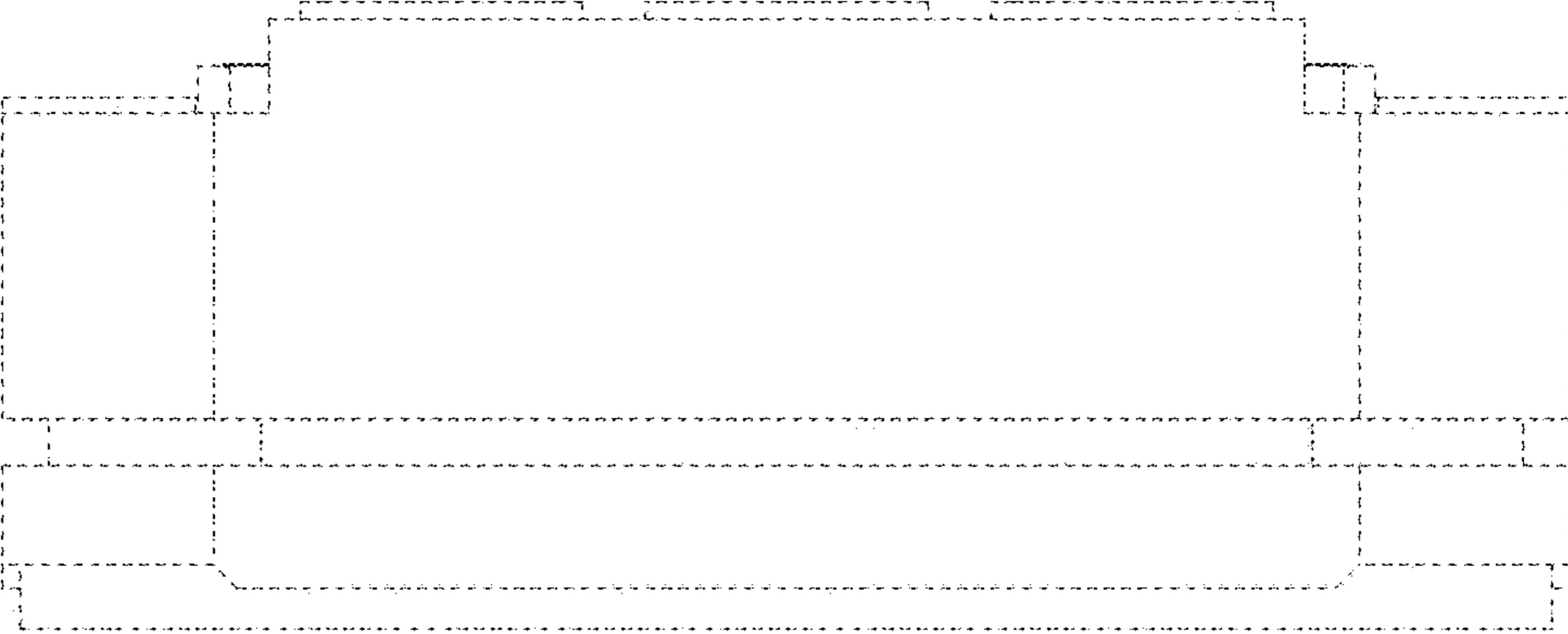


Fig. 7

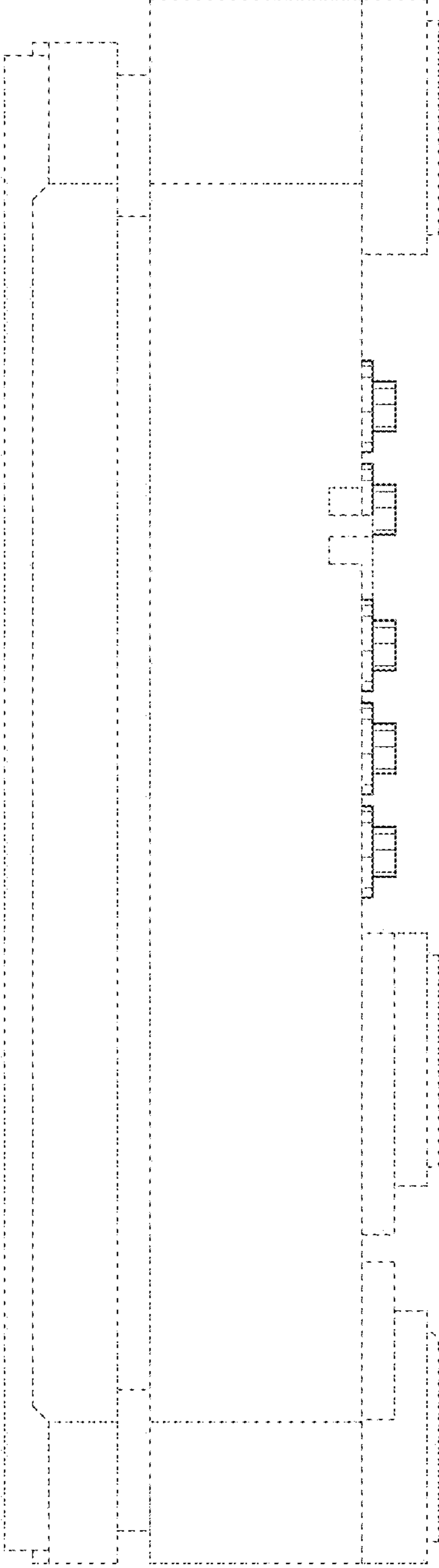
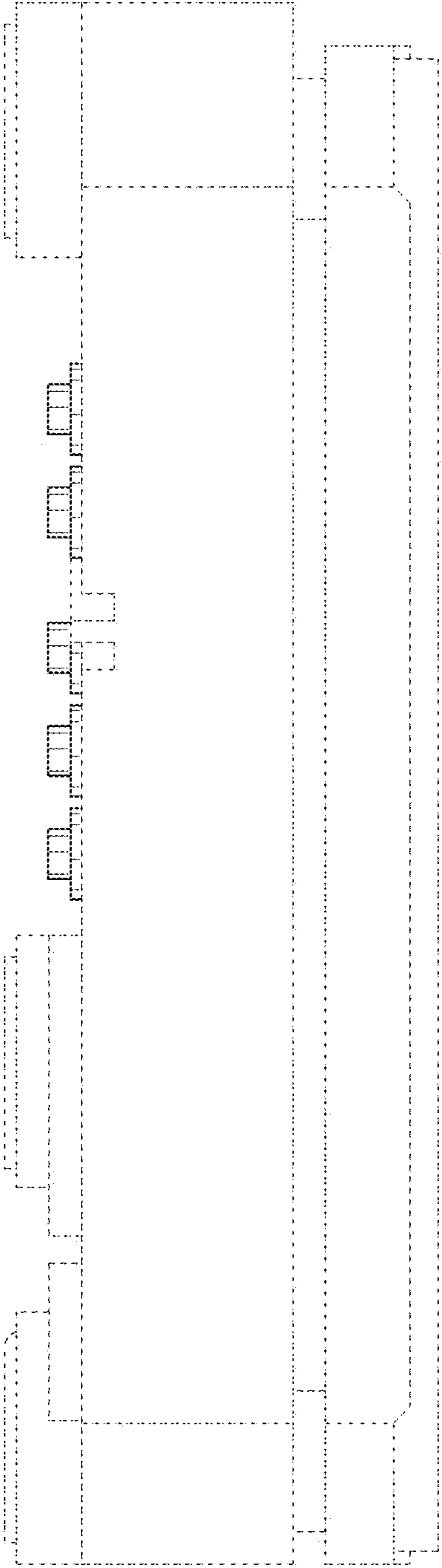


Fig. 8



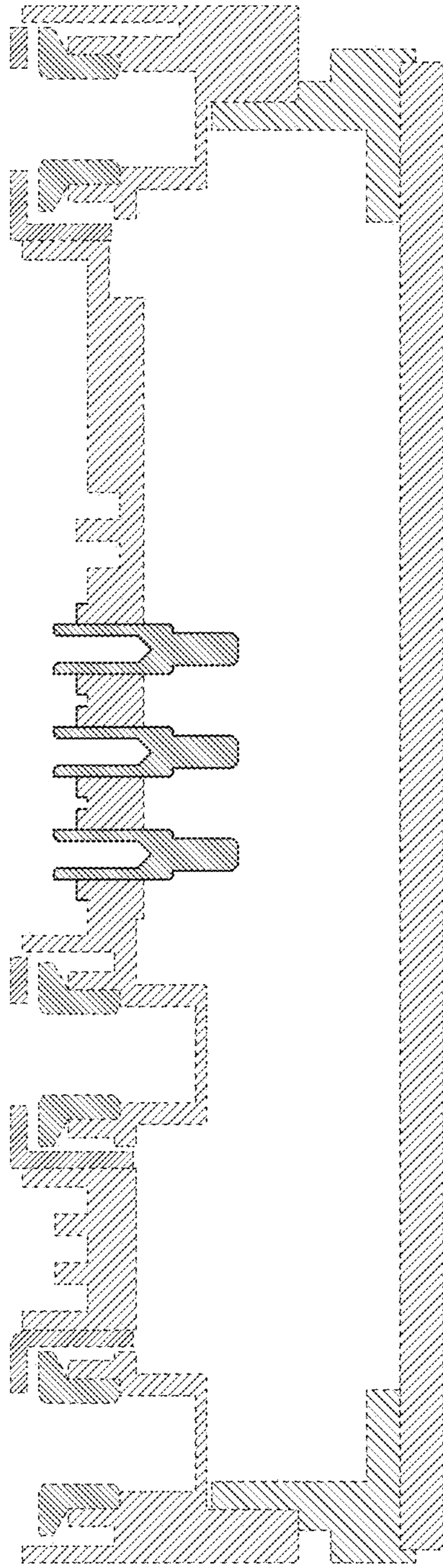


Fig. 9

Fig. 10

