US00D825472S

(12) United States Design Patent

Yamanaka et al.

(10) Patent No.: US D825,472 S
(45) Date of Patent: ** Aug. 14, 2018

(54) **INPUT/OUTPUT DEVICE**

(71) Applicant: **FANUC CORPORATION**, Yamanashi (JP)

(72) Inventors: **Masashi Yamanaka**, Yamanashi (JP); **Yuuma Ootsuka**, Yamanashi (JP)

(73) Assignee: **FANUC CORPORATION**, Yamanashi (JP)

(**) Term: **15 Years**

(21) Appl. No.: **29/579,272**

(22) Filed: **Sep. 29, 2016**

(30) **Foreign Application Priority Data**

Mar. 30, 2016 (JP) 2016-006990

(51) **LOC (11) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/147**; D13/155

(58) **Field of Classification Search**
USPC D13/133, 146, 147, 148, 154, 155, 158, D13/173, 182, 184, 199
CPC G02B 6/38; G02B 6/4416; G02B 6/4471; H01B 9/005; H02G 3/08; H02G 3/18; H01R 9/031; H01R 9/032; H01R 9/075; H01R 12/53; H01R 12/592; H01R 12/62; H01R 12/72; H01R 12/75; H01R 13/627; H01R 13/717
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

D433,998	S	*	11/2000	Ishitsuka	D13/123
D443,586	S	*	6/2001	Sakasegawa	D13/123
D443,587	S	*	6/2001	Sakasegawa	D13/123
D544,836	S	*	6/2007	Sichner	D13/123
2017/0141563	A1	*	5/2017	Islam	H02H 3/20

* cited by examiner

Primary Examiner — Daniel Bui
(74) *Attorney, Agent, or Firm* — RatnerPrestia

(57) **CLAIM**

The ornamental design for an input/output device, as shown and described.

DESCRIPTION

FIG. **1** is a front, right and bottom perspective view of a cable breakout enclosure design showing my new design;
FIG. **2** is a front elevational view thereof;
FIG. **3** is a rear elevational view thereof;
FIG. **4** is a left side elevational view thereof;
FIG. **5** is a right side elevational view thereof;
FIG. **6** is a bottom plan view thereof; and,
FIG. **7** is a top plan view thereof.
The broken lines shown in FIGS. **1**, **2**, **5** and **7** represent unclaimed environment only and form no part of the claimed design.

1 Claim, 5 Drawing Sheets

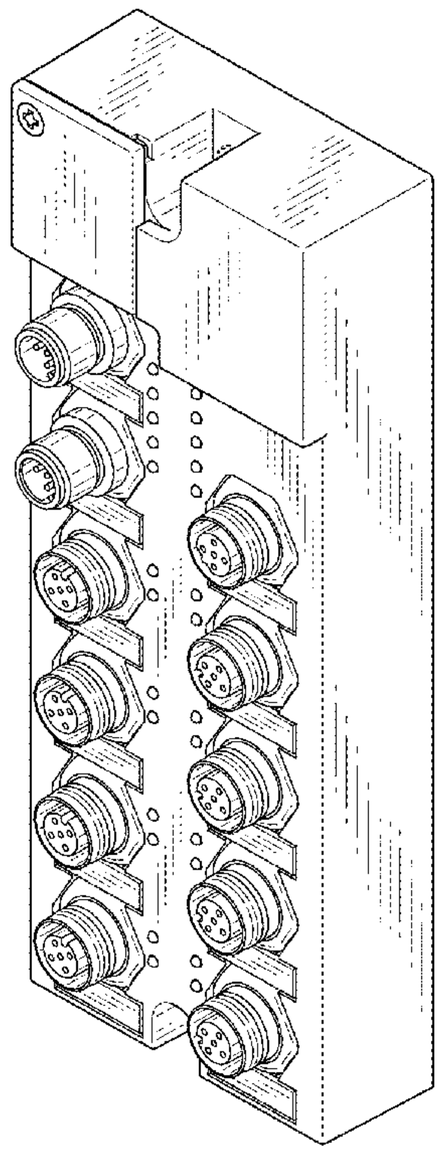


FIG. 1

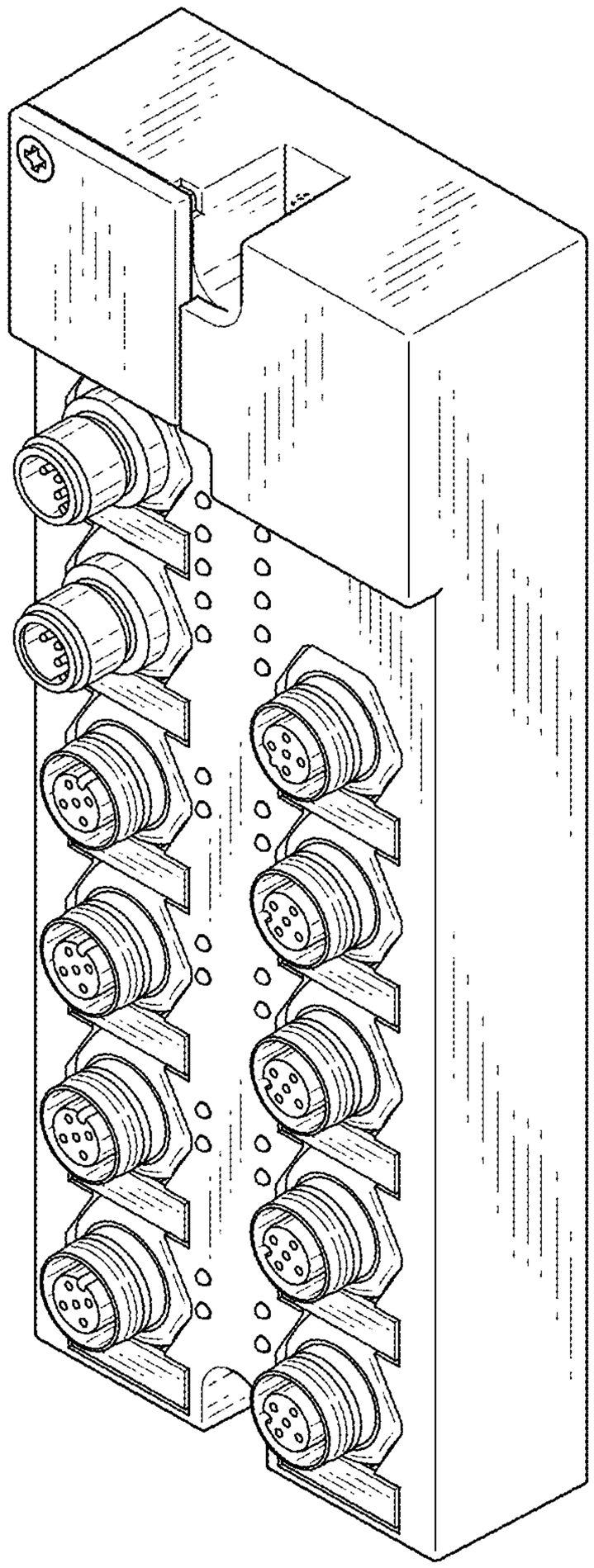


FIG. 2

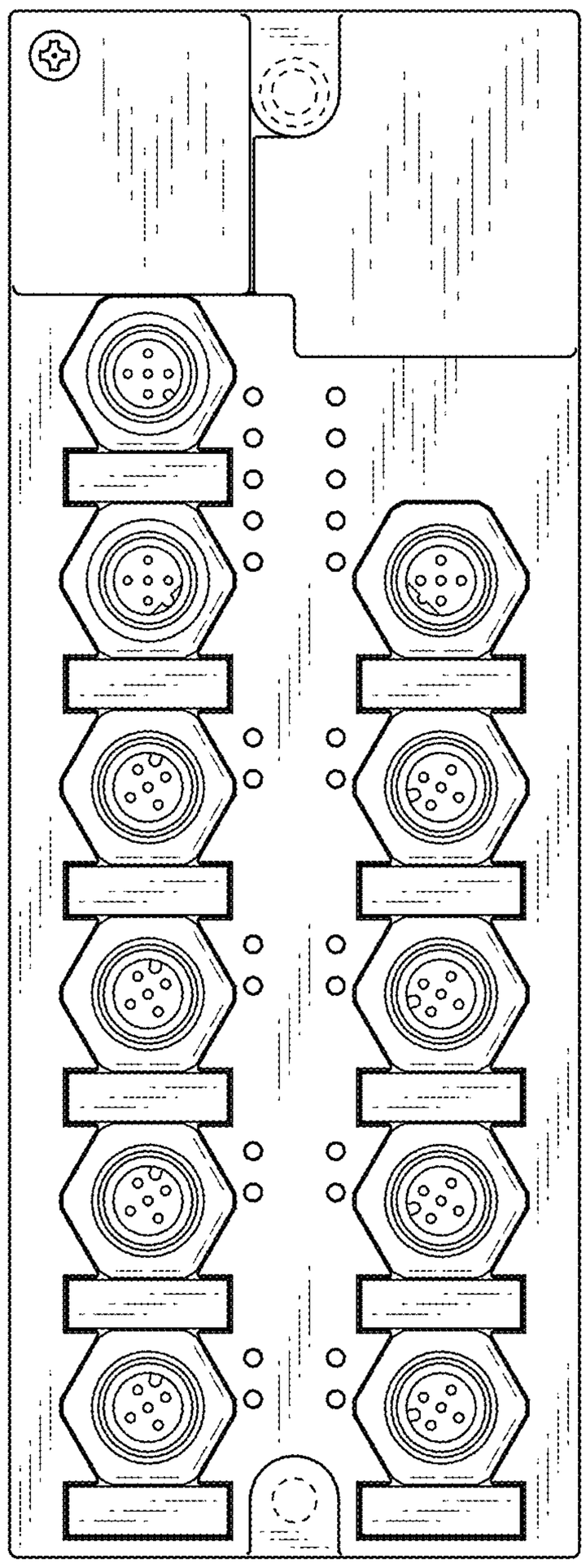


FIG. 3

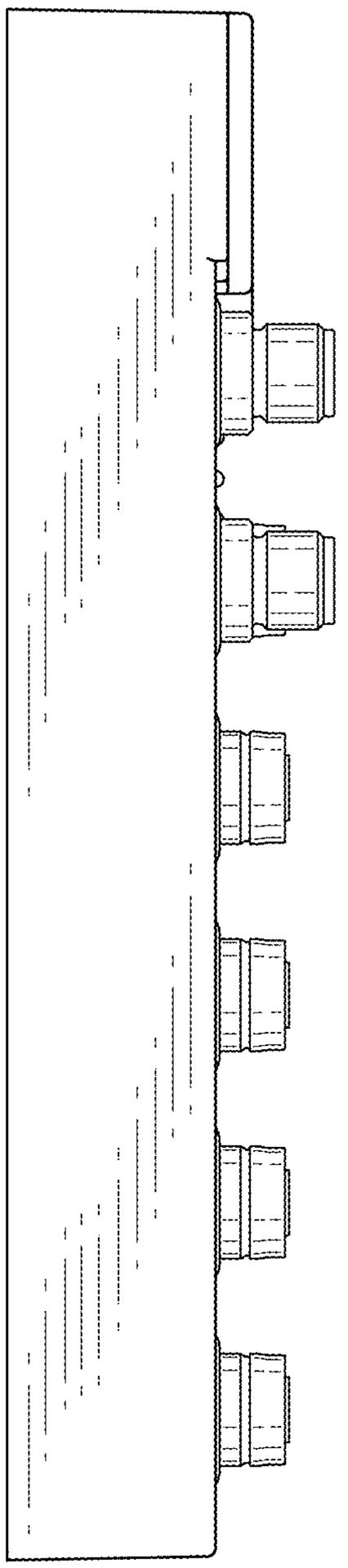


FIG. 4

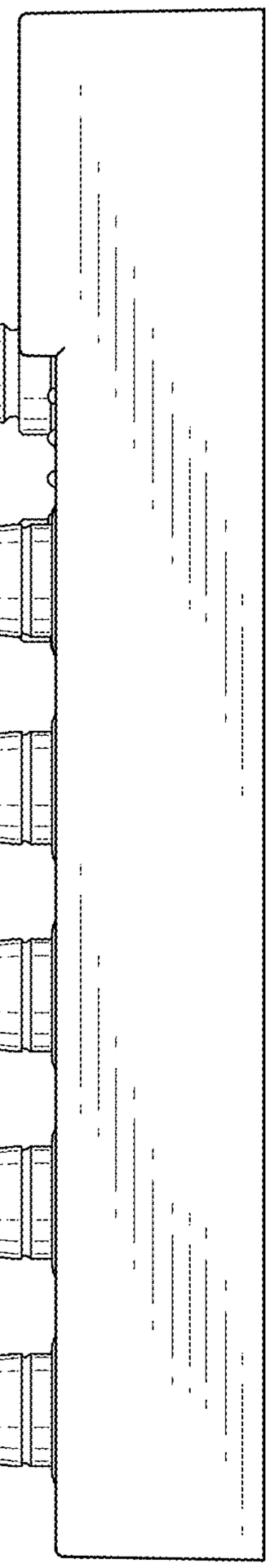


FIG. 5

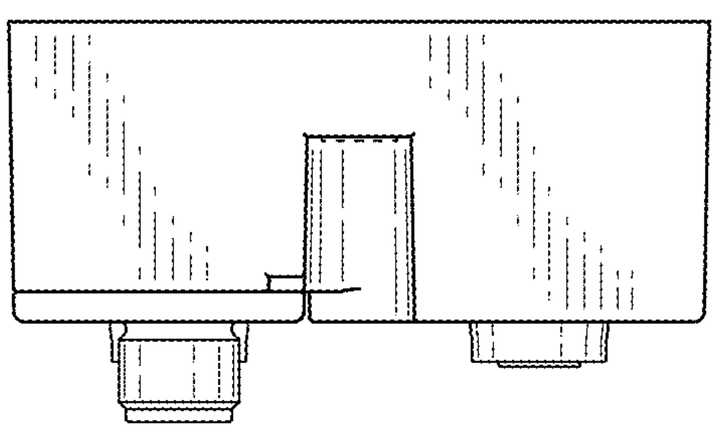


FIG. 6

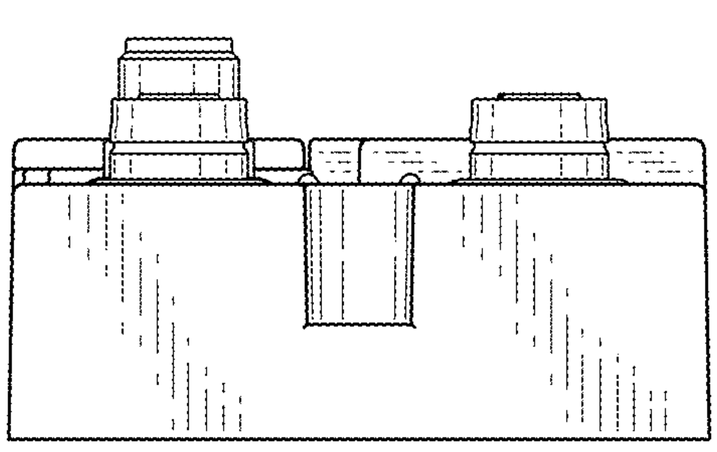
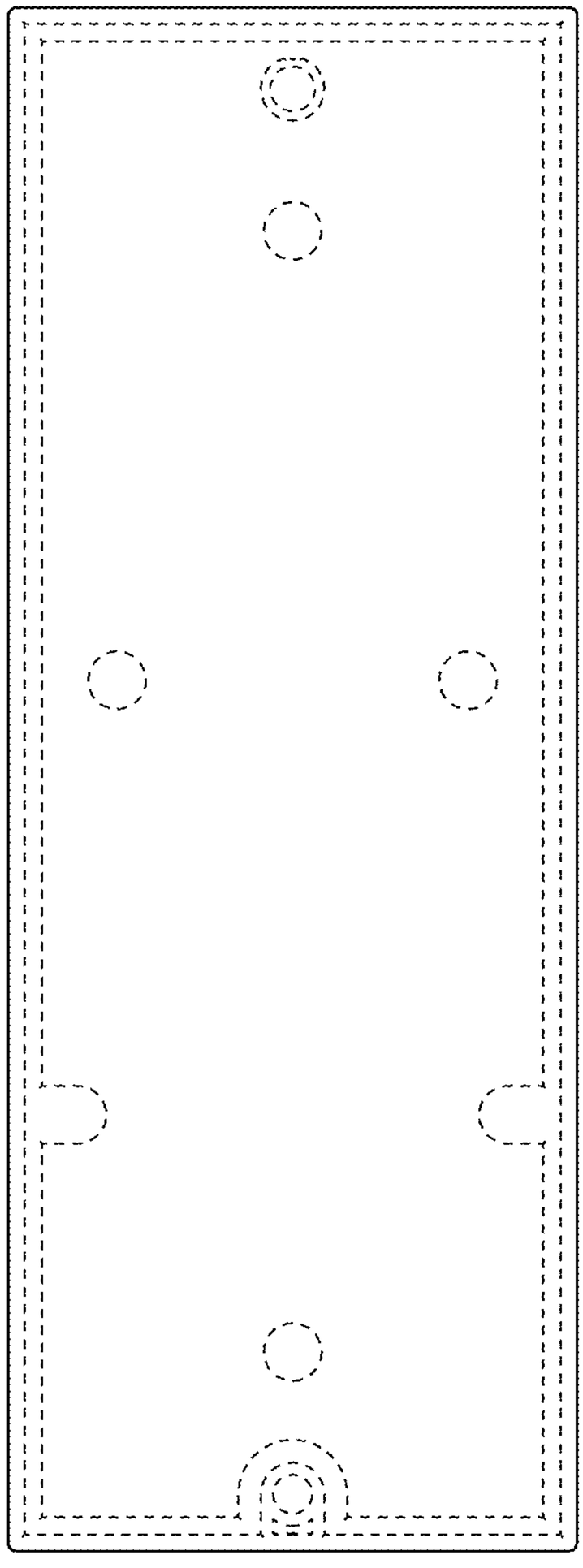


FIG. 7



UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : D825,472 S
APPLICATION NO. : 29/579272
DATED : August 14, 2018
INVENTOR(S) : Masashi Yamanaka et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title Page

Item (57), under DESCRIPTION should read as:
Fig. 1 is a front, right and top perspective view of an input/output device showing our new design;
Fig. 2 is a front view thereof;
Fig. 3 is a left side elevational view thereof;
Fig. 4 is a right side elevational view thereof;
Fig. 5 is a top plan view thereof;
Fig. 6 is a bottom plan view thereof; and
Fig. 7 is a rear view thereof.
The broken lines shown in FIGS. 1, 2, 5 and 7 represent unclaimed environment only and form no part of the claimed design.

Signed and Sealed this
Twelfth Day of March, 2019

Andrei Iancu
Director of the United States Patent and Trademark Office