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(12) **United States Design Patent** (10) **Patent No.: US D818,961 S**
Yamaguchi (45) **Date of Patent: ** May 29, 2018**

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(54) **INSULATION UNIT COVER OF SEMICONDUCTOR MANUFACTURING APPARATUS**

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(72) Inventor: **Takatomo Yamaguchi**, Toyama (JP)

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(**) Term: **15 Years**

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(30) **Foreign Application Priority Data**

Feb. 10, 2016 (JP) 002843/2016

(51) **LOC (11) Cl.** **13-03**
(52) **U.S. Cl.**
USPC **D13/129**
(58) **Field of Classification Search**
USPC D13/123–132, 182, 184, 199; D15/138, D15/140, 144.1
CPC F27B 17/0025; F27B 17/005; F27B 17/0058; F27B 2017/0091; G01R 1/40; G01R 1/42; G01R 1/44; H01L 21/31; H01L 21/3105; H01L 21/311; H01L 21/3115
See application file for complete search history.

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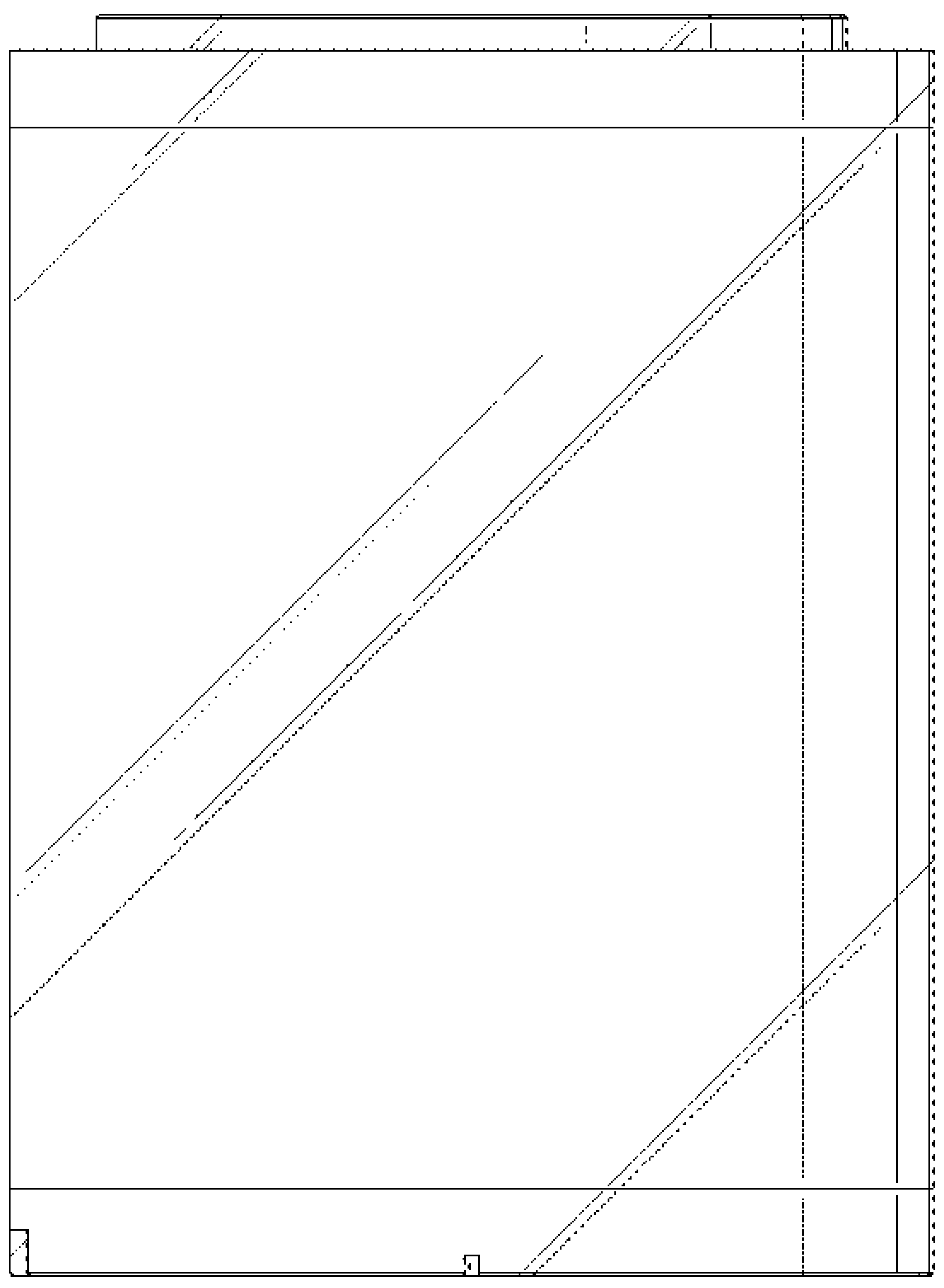
(57) **CLAIM**

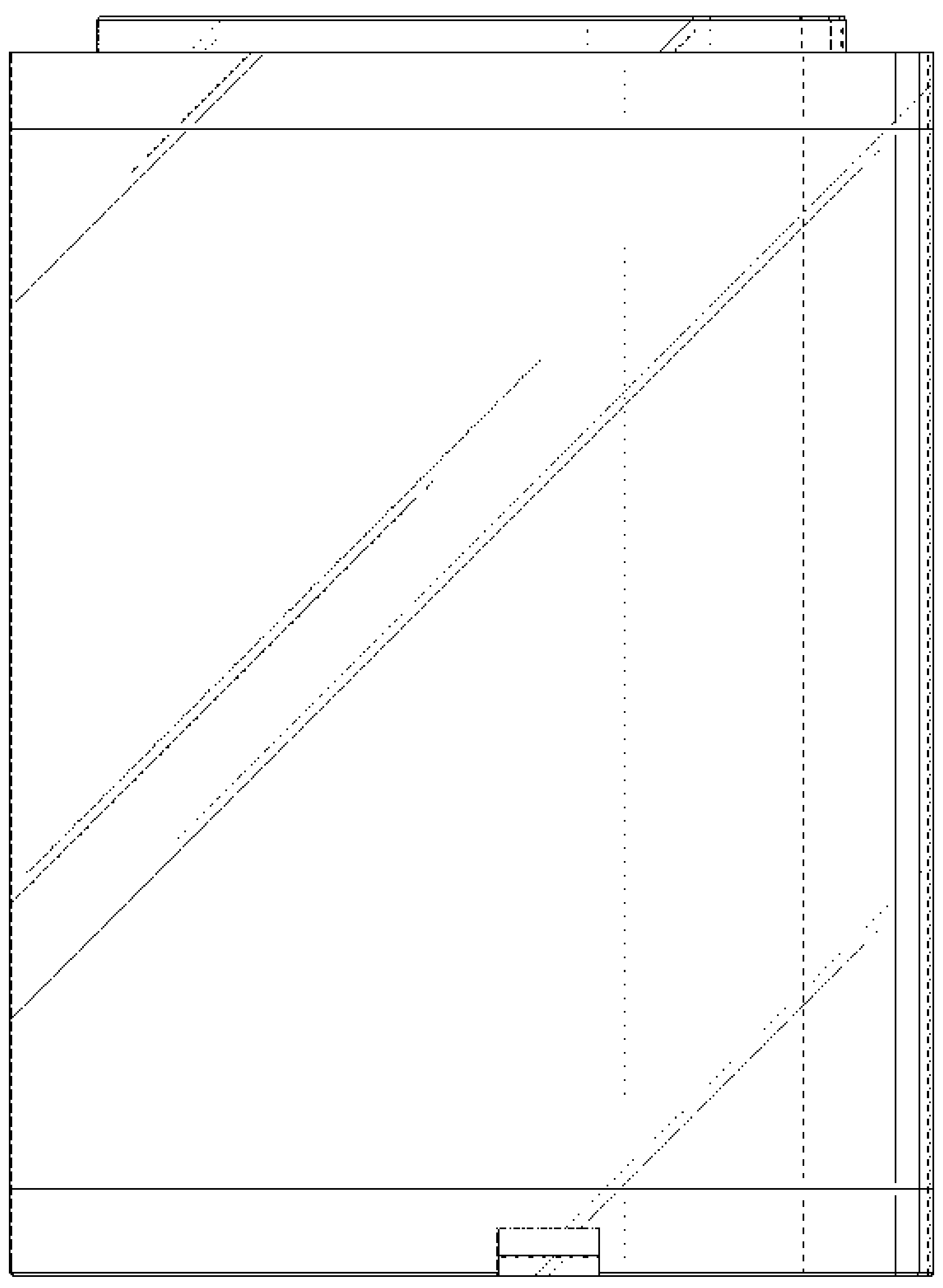
I claim the ornamental design for an insulation unit cover of semiconductor manufacturing apparatus, as shown and described.

DESCRIPTION

FIG. **1** is a perspective view of an insulation unit cover of semiconductor manufacturing apparatus showing my new design;
FIG. **2** is a front elevational view thereof;
FIG. **3** is a rear elevational view thereof;
FIG. **4** is a left side elevational view thereof;
FIG. **5** is a right side elevational view thereof;
FIG. **6** is a top plan view thereof;
FIG. **7** is a bottom plan view thereof; and,
FIG. **8** is a cross-sectional view thereof taken in the direction of line **8**-**8** in FIG. **6**.
The dot-dash broken lines FIG. **6** are for reference purposes only; the broken lines form no part of the claimed design.

1 Claim, 7 Drawing Sheets





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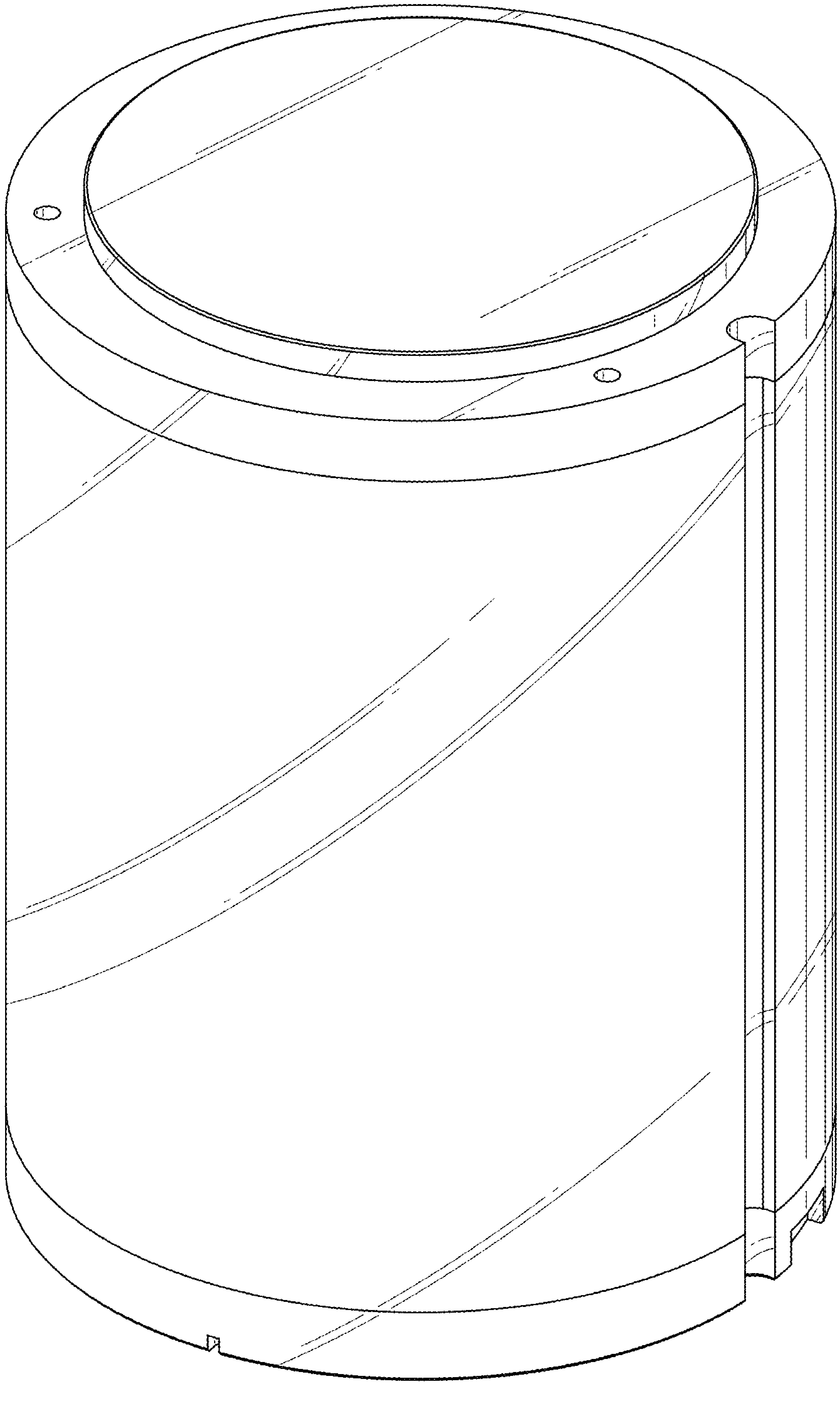

FIG. 1

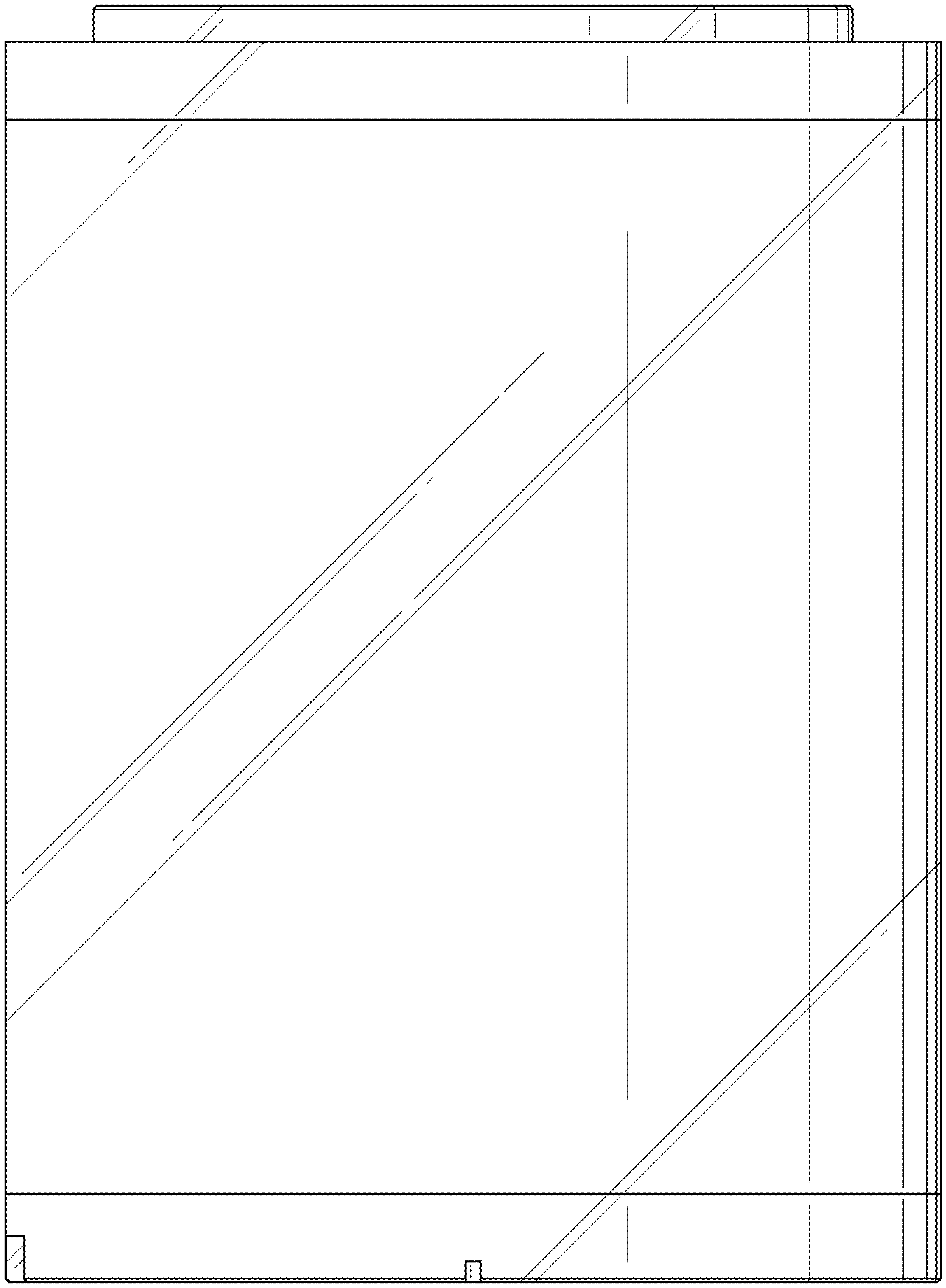

FIG. 2

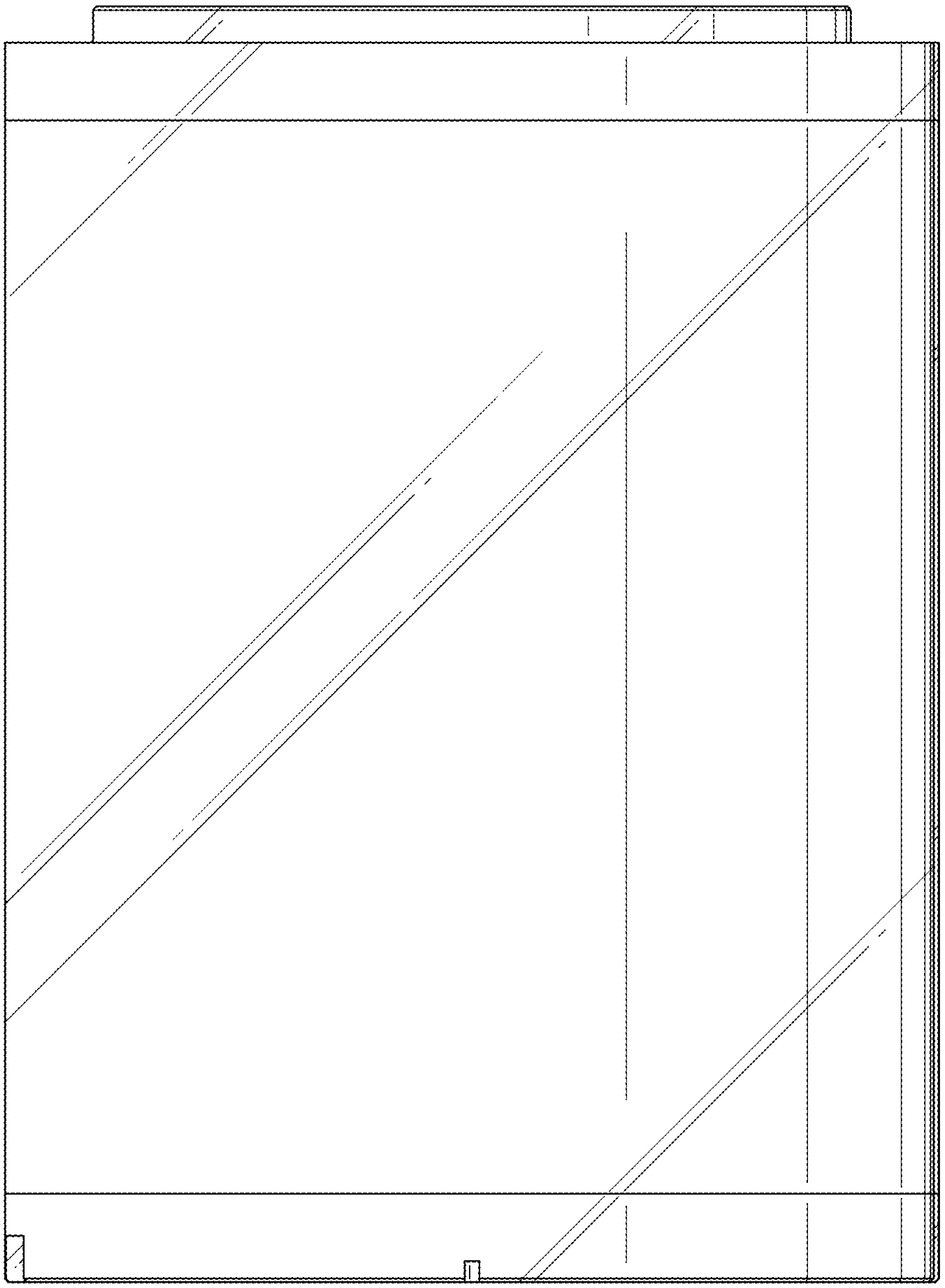

FIG. 3

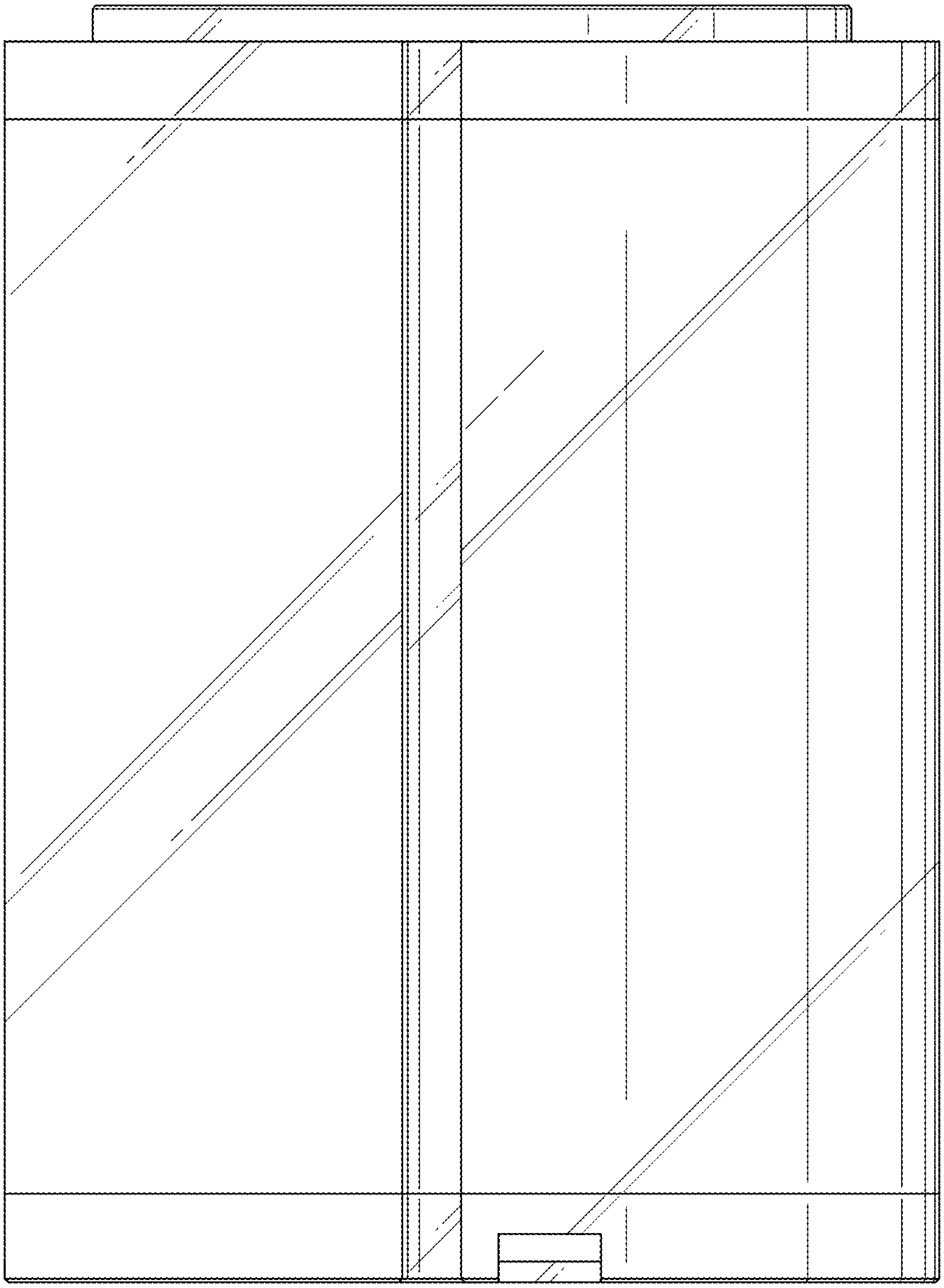

FIG. 4

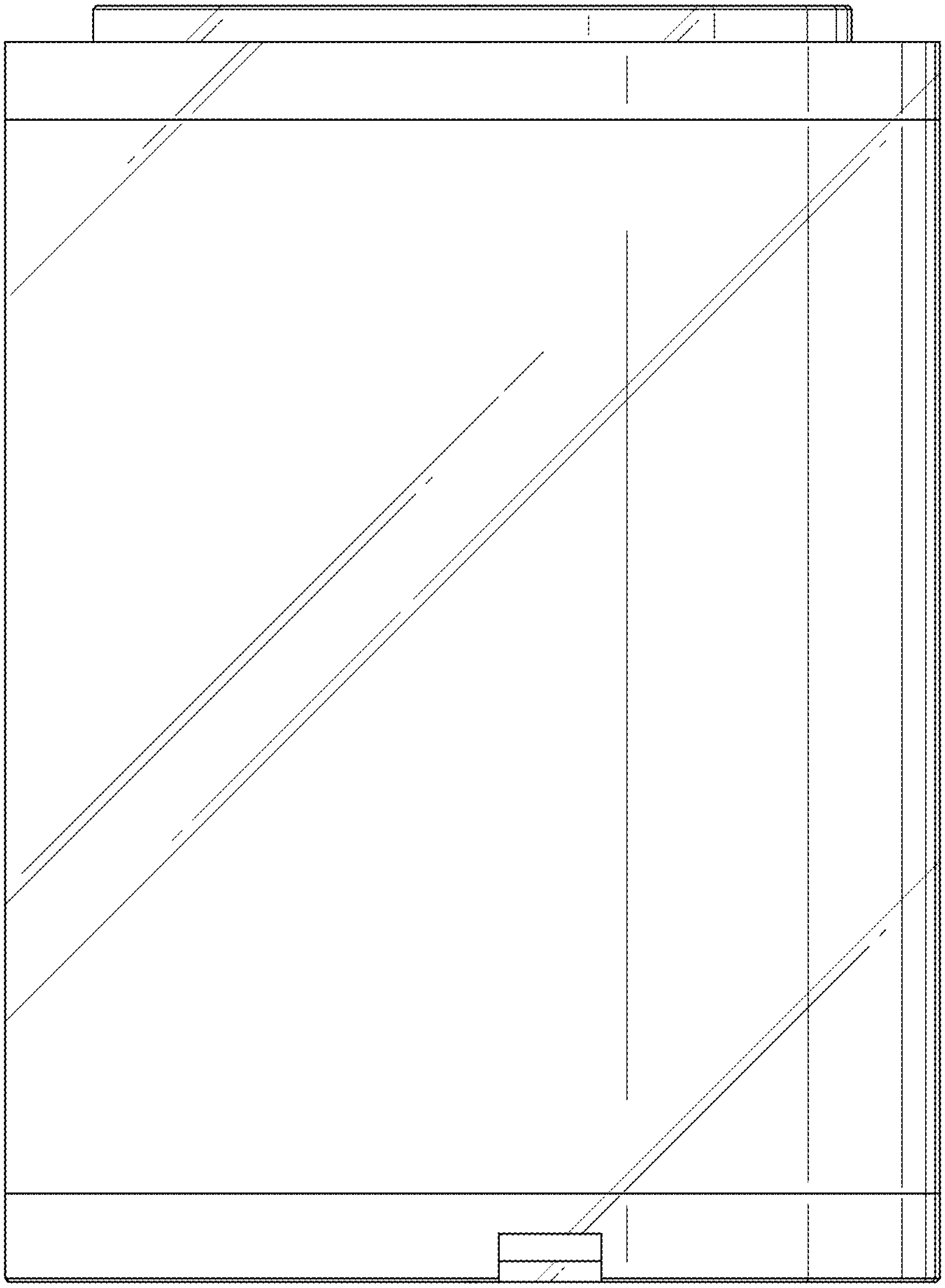

FIG. 5

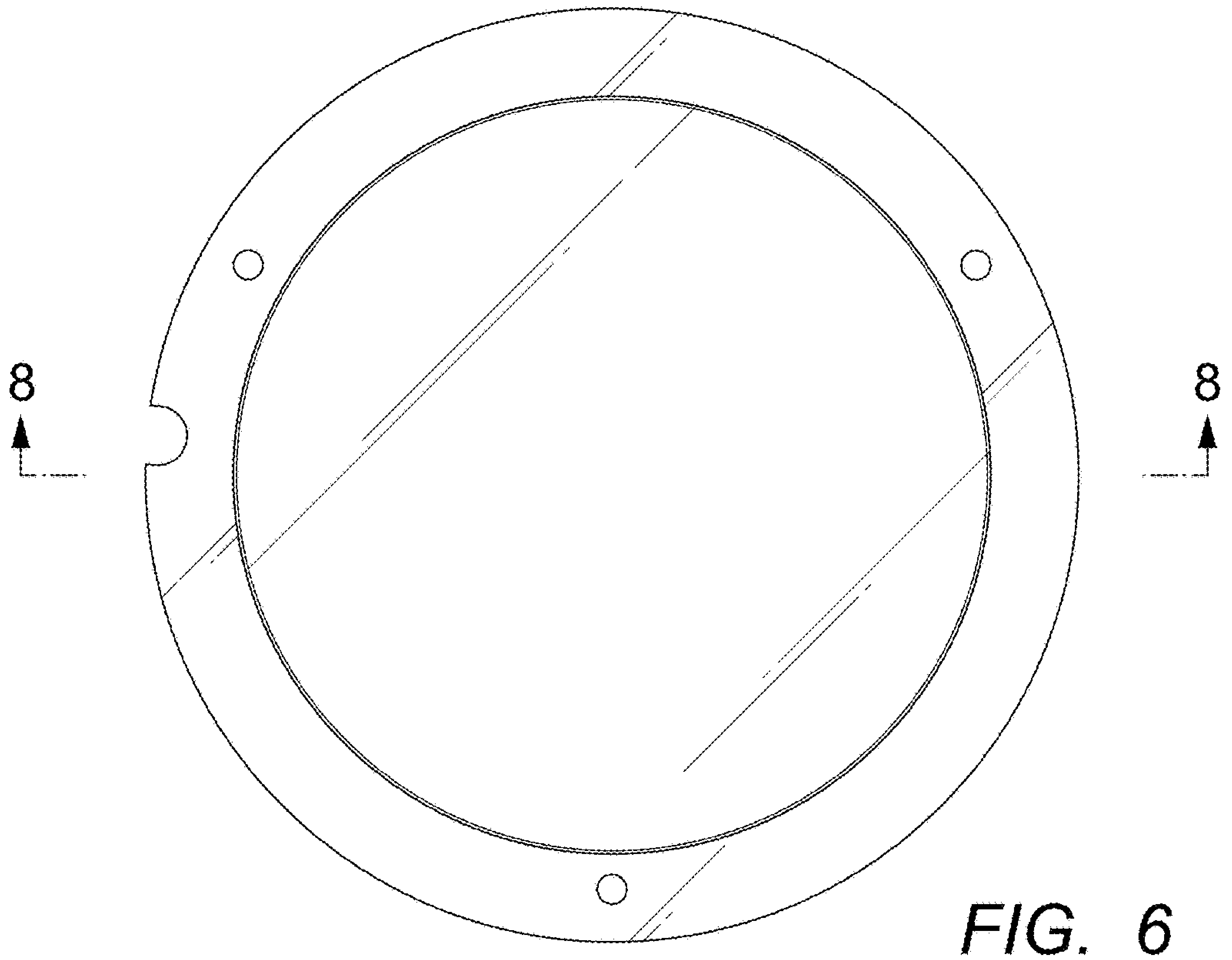

FIG. 6

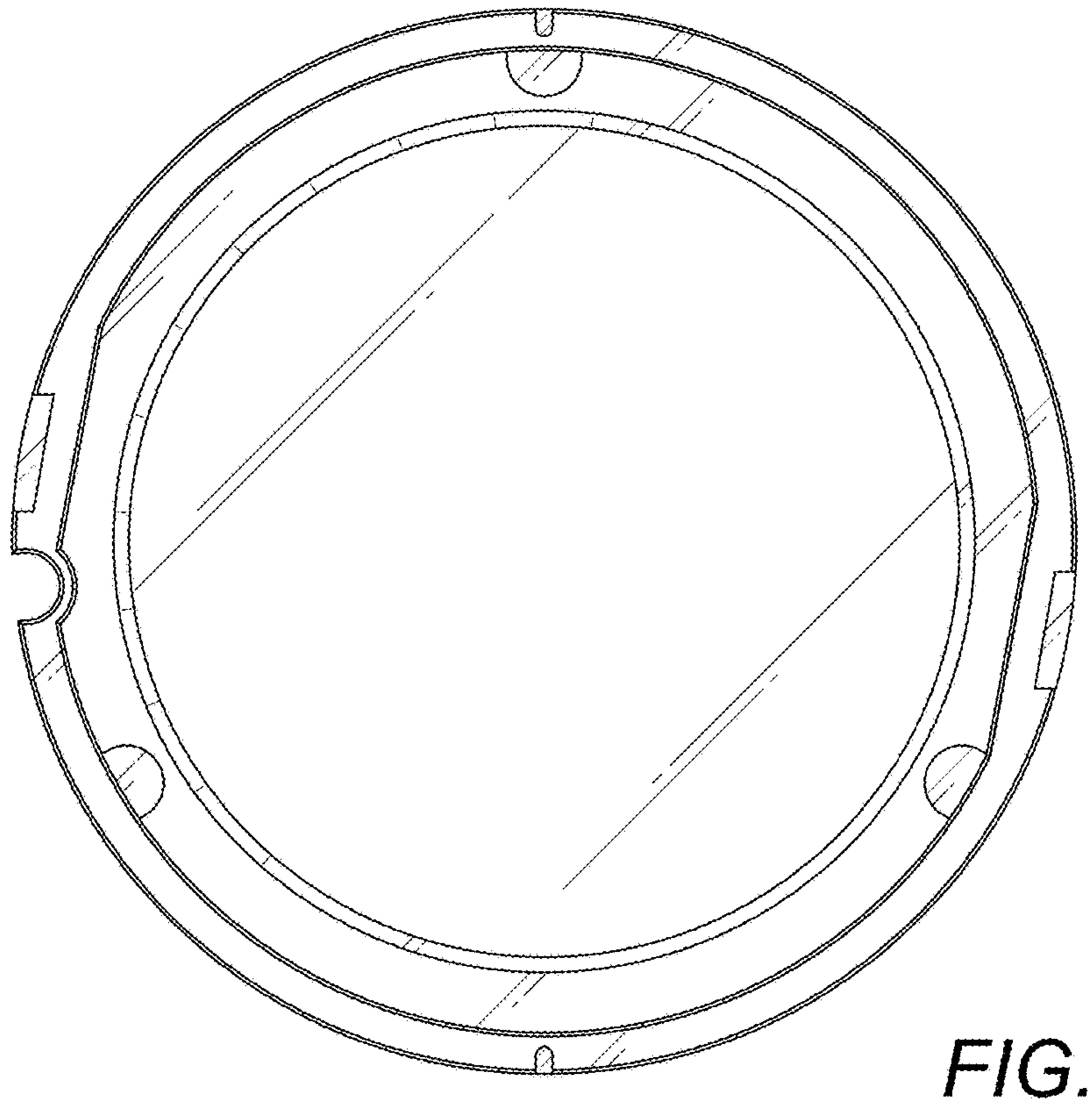

FIG. 7

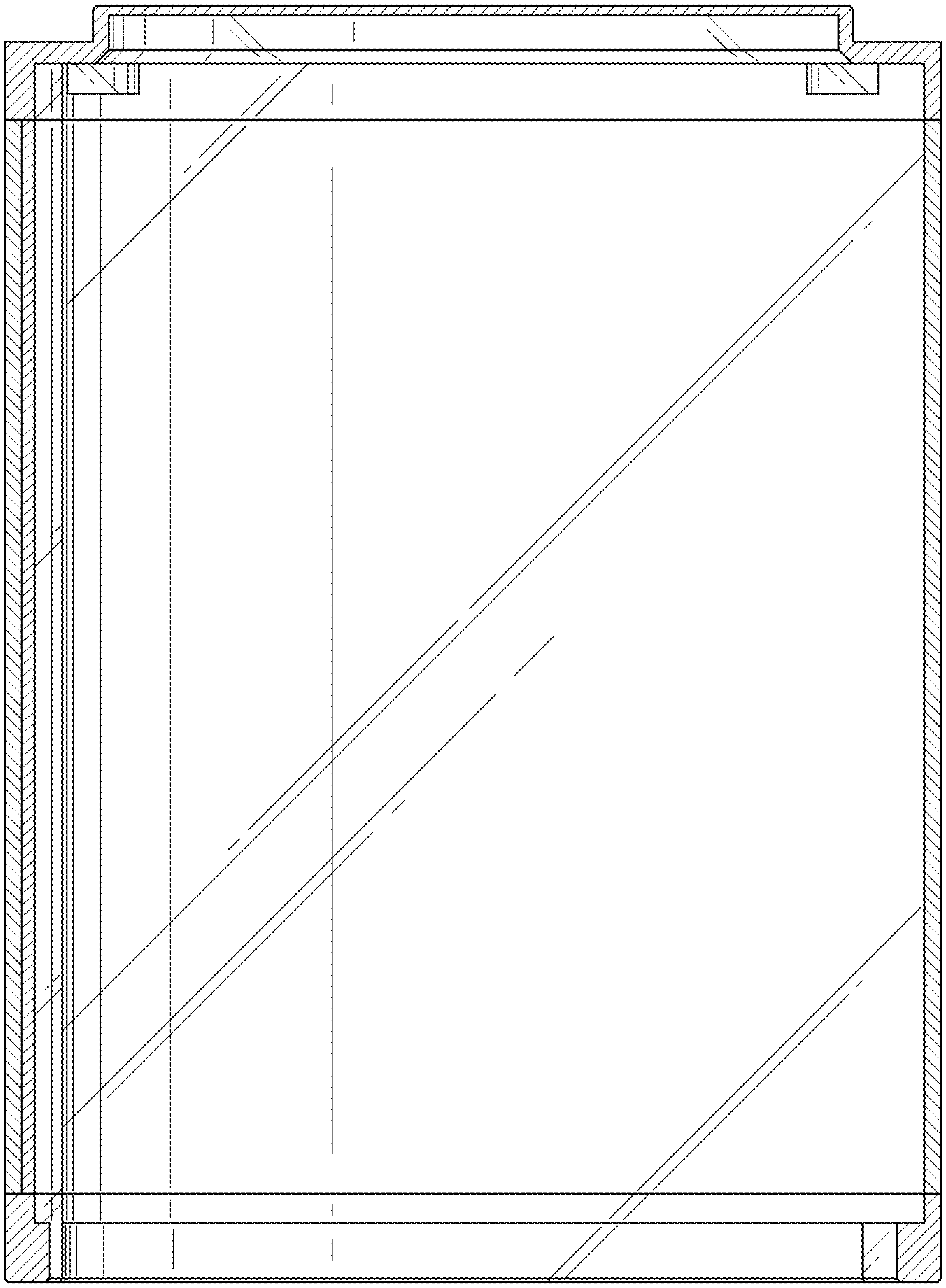

FIG. 8