



US00D818649S

(12) **United States Design Patent** (10) **Patent No.:** **US D818,649 S**
Ranade (45) **Date of Patent:** **** May 22, 2018**

(54) **VEST**
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(73) Assignee: **Intel Corporation**, Santa Clara, CA (US)
(**) Term: **15 Years**
(21) Appl. No.: **29/588,563**
(22) Filed: **Dec. 21, 2016**
(51) **LOC (11) Cl.** **29-02**
(52) **U.S. Cl.**
USPC **D29/101.4**
(58) **Field of Classification Search**
USPC D29/100, 101, 101.2, 101.3, 101.4, 122, D29/124; D2/626, 829, 830, 860; 362/108; D21/805; 441/88, 106, 108, 441/111, 117; 182/3; 2/48, 51, 92, 102, 2/103, 105, 913, 914, 915
CPC A41D 1/00; A45F 3/00
See application file for complete search history.

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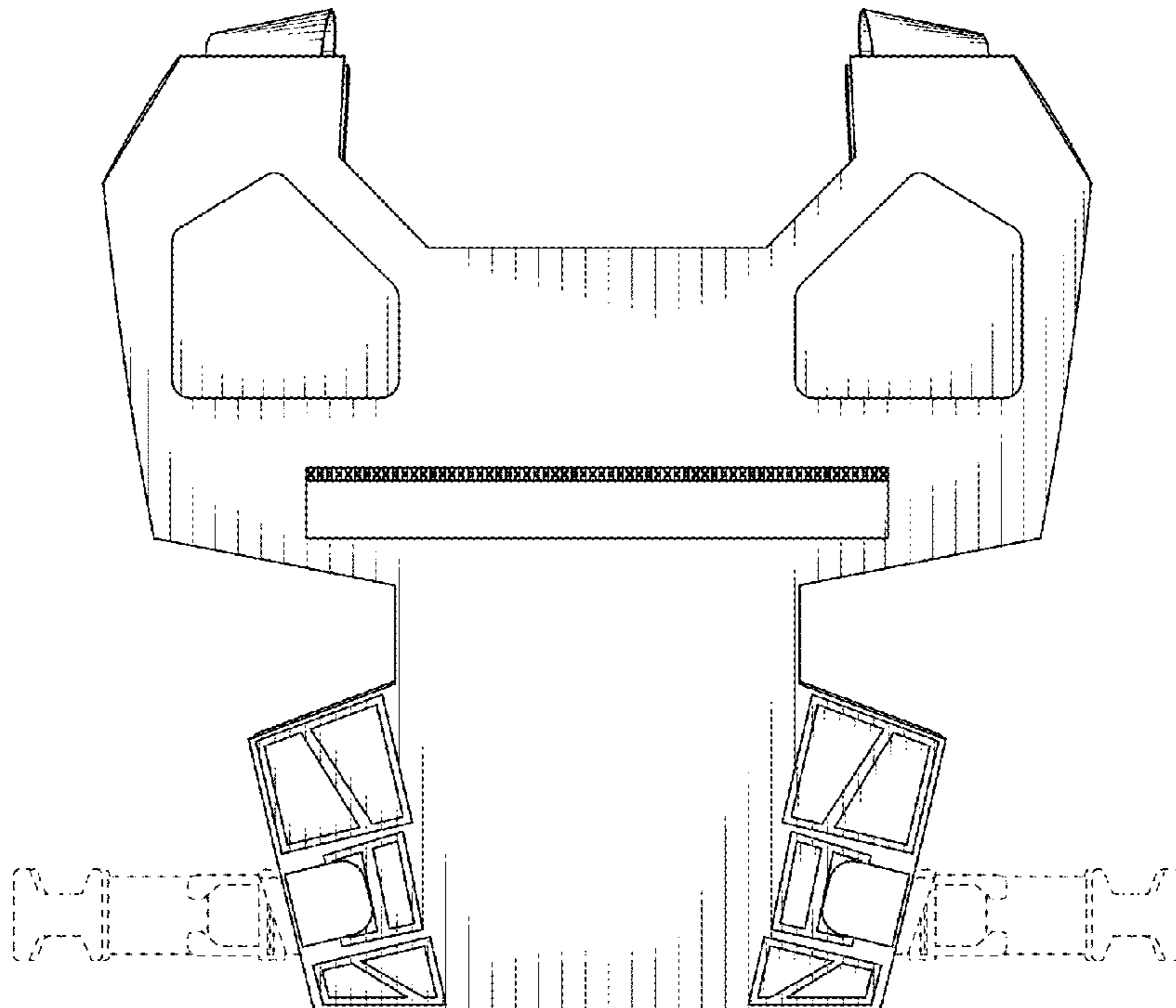
* cited by examiner

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(57) **CLAIM**
The ornamental design for a vest, as shown and described.

DESCRIPTION
FIG. 1 is a front view of a vest (e.g., an electronics module carrier vest), showing my new design.
FIG. 2 is a rear view of the vest.
FIG. 3 is a right side view of the vest.
FIG. 4 is a left side view of the vest.
FIG. 5 is a top view of the vest.
FIG. 6 is a bottom view of the vest.
FIG. 7 is a bottom-rear-right perspective view of the vest.
FIG. 8 is a top-rear-right perspective view of the vest.
FIG. 9 is a top-front-right perspective view of the vest; and, FIG. 10 is a bottom-front-left perspective view of the vest.
The shade lines show surface contour and not surface ornamentation.
The broken line showing of fasteners (e.g., straps and buckles) of the vest illustrates environmental structure, and the broken lines form no part of the claimed design.

1 Claim, 8 Drawing Sheets



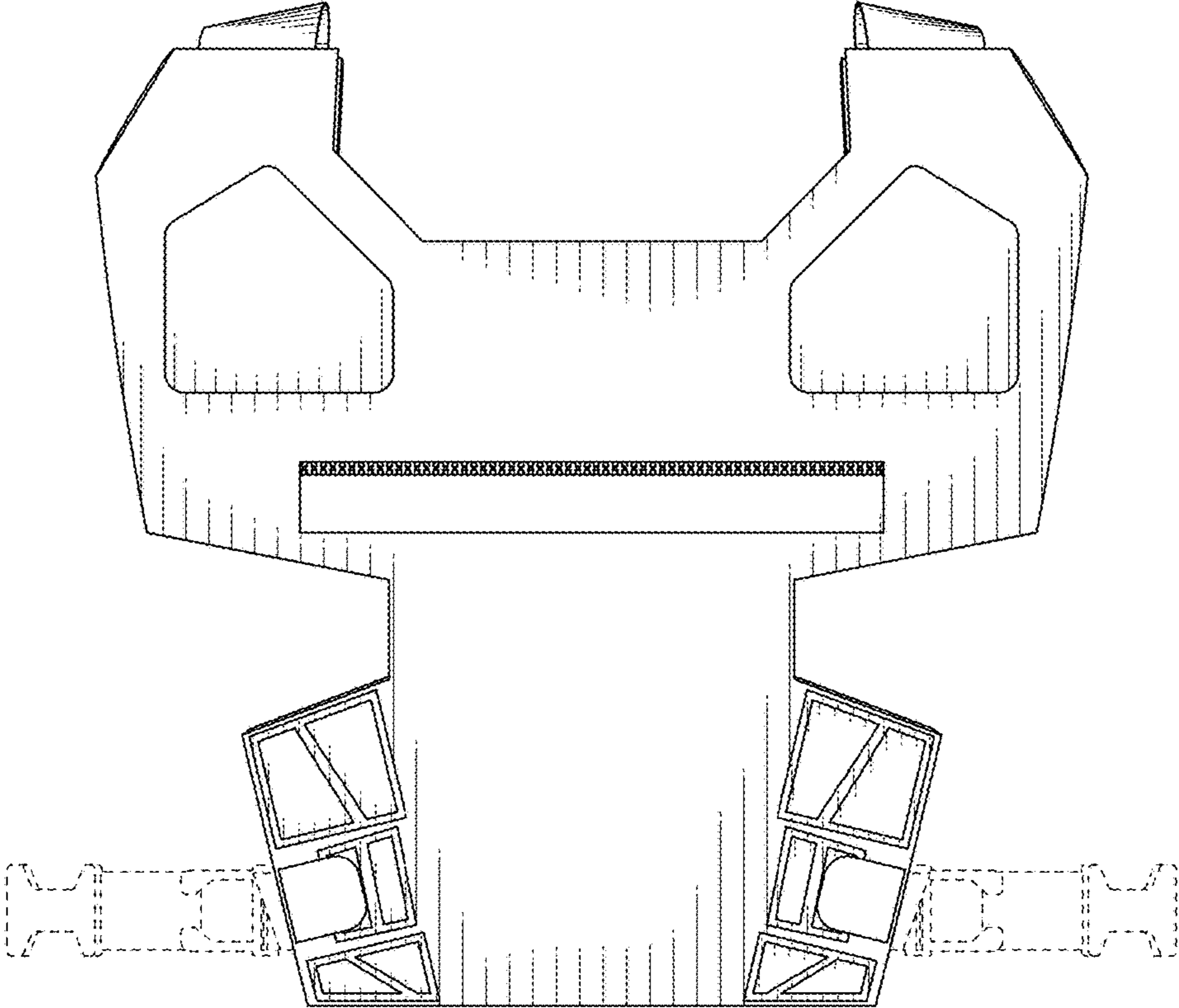


FIG. 1

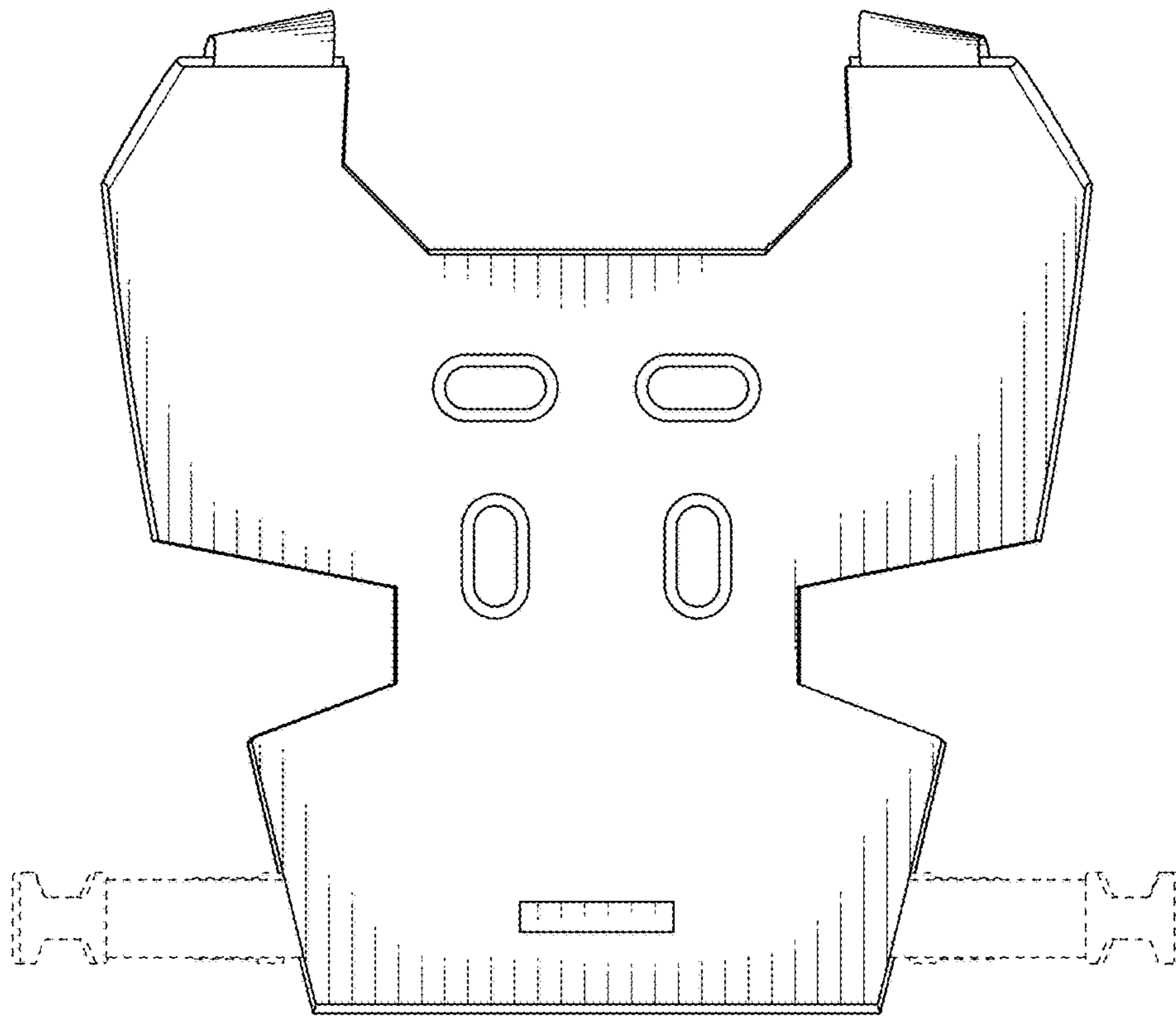


FIG. 2

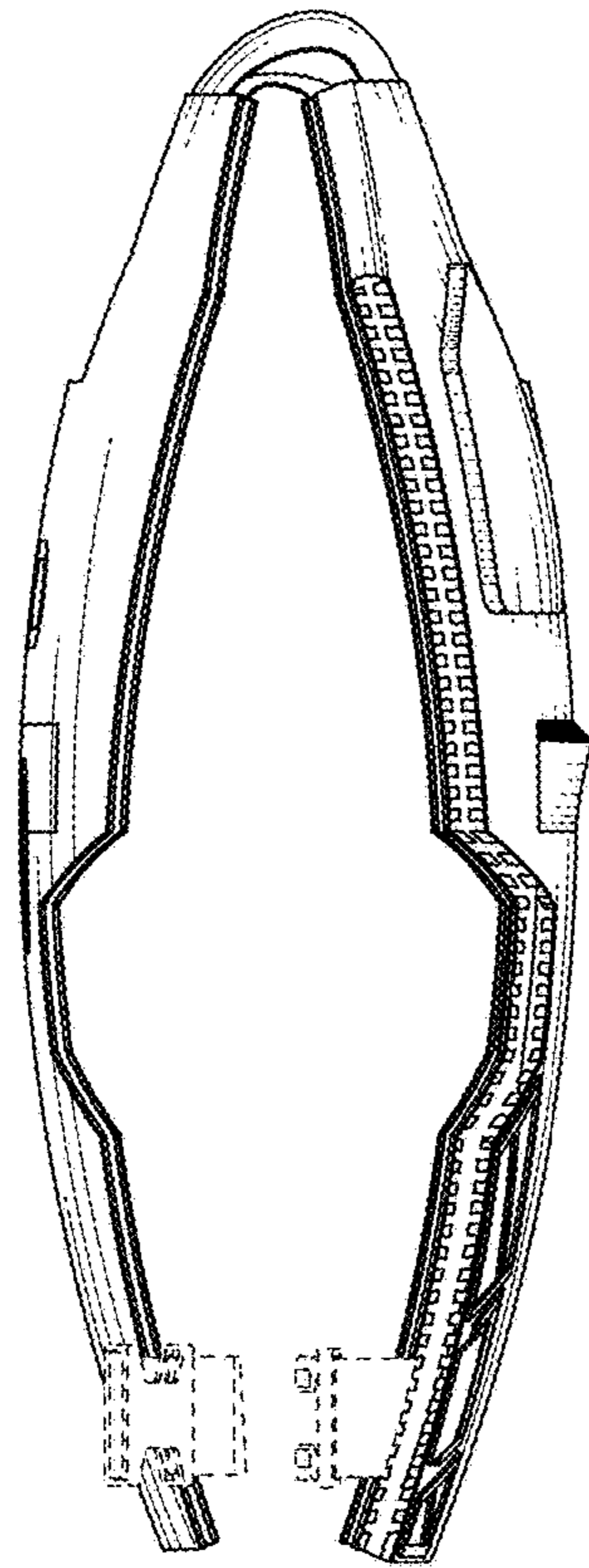


FIG. 3

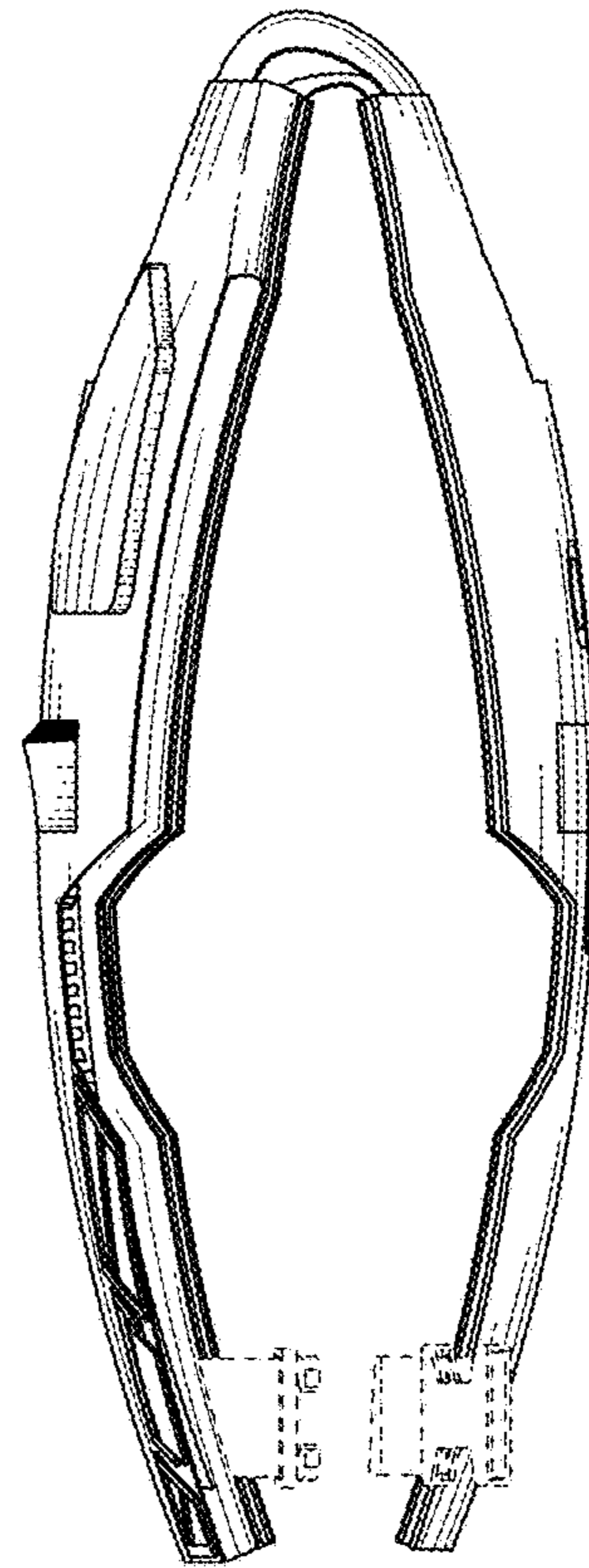


FIG. 4

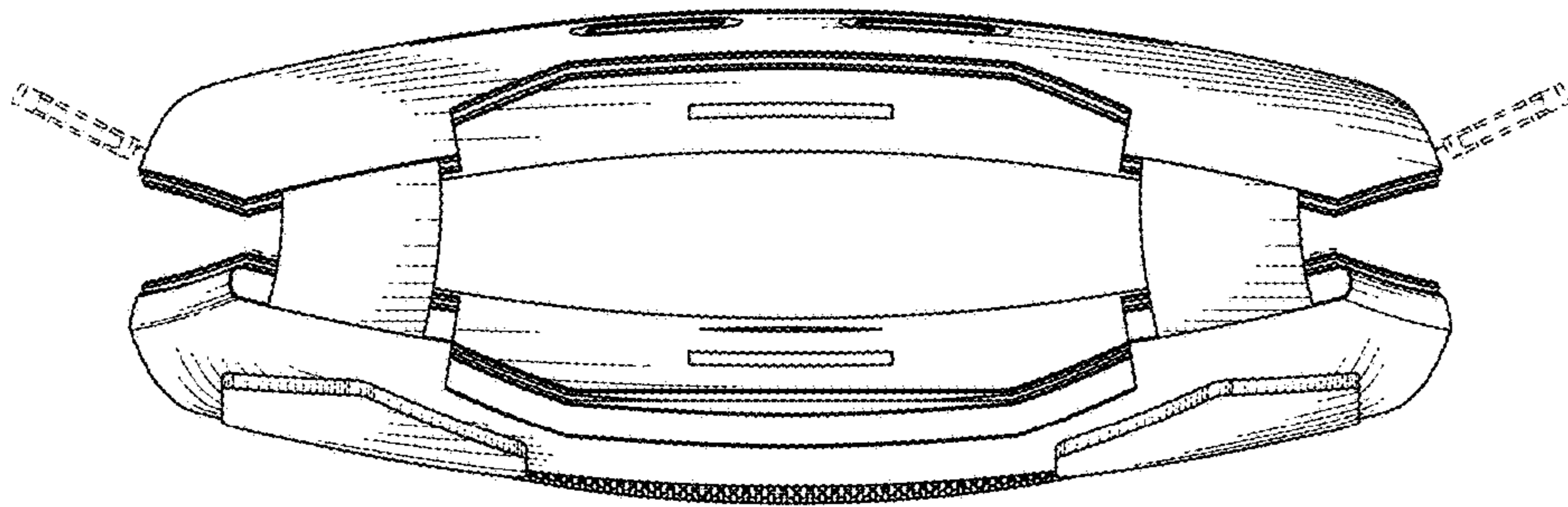


FIG. 5

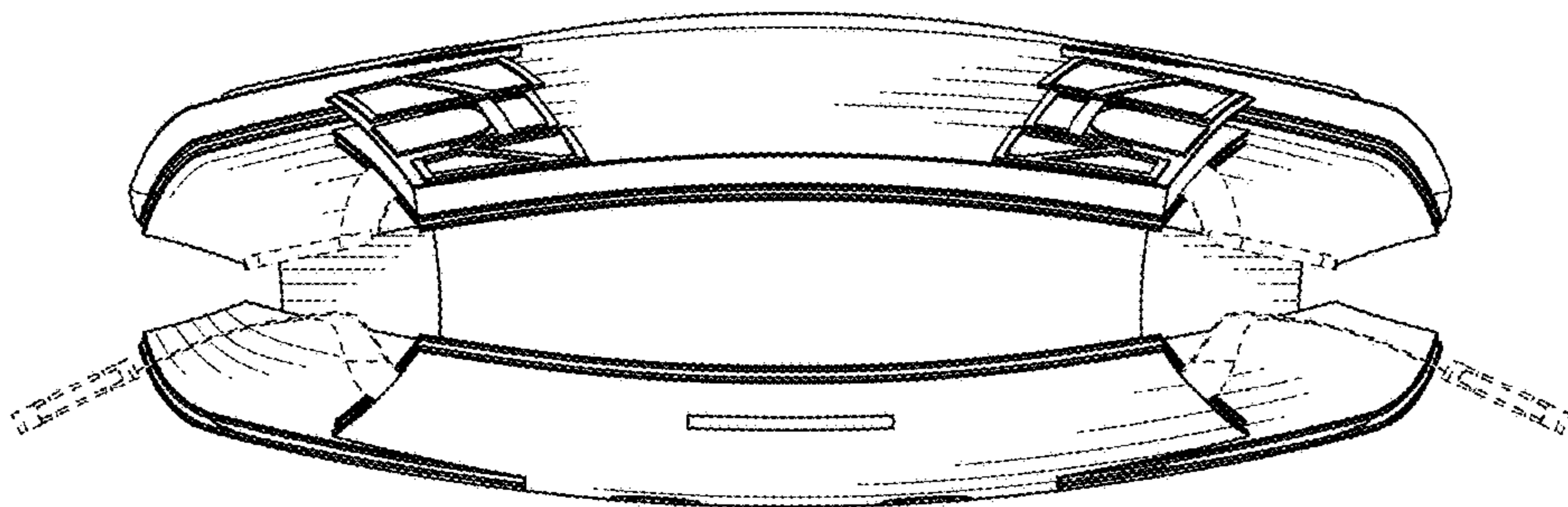


FIG. 6

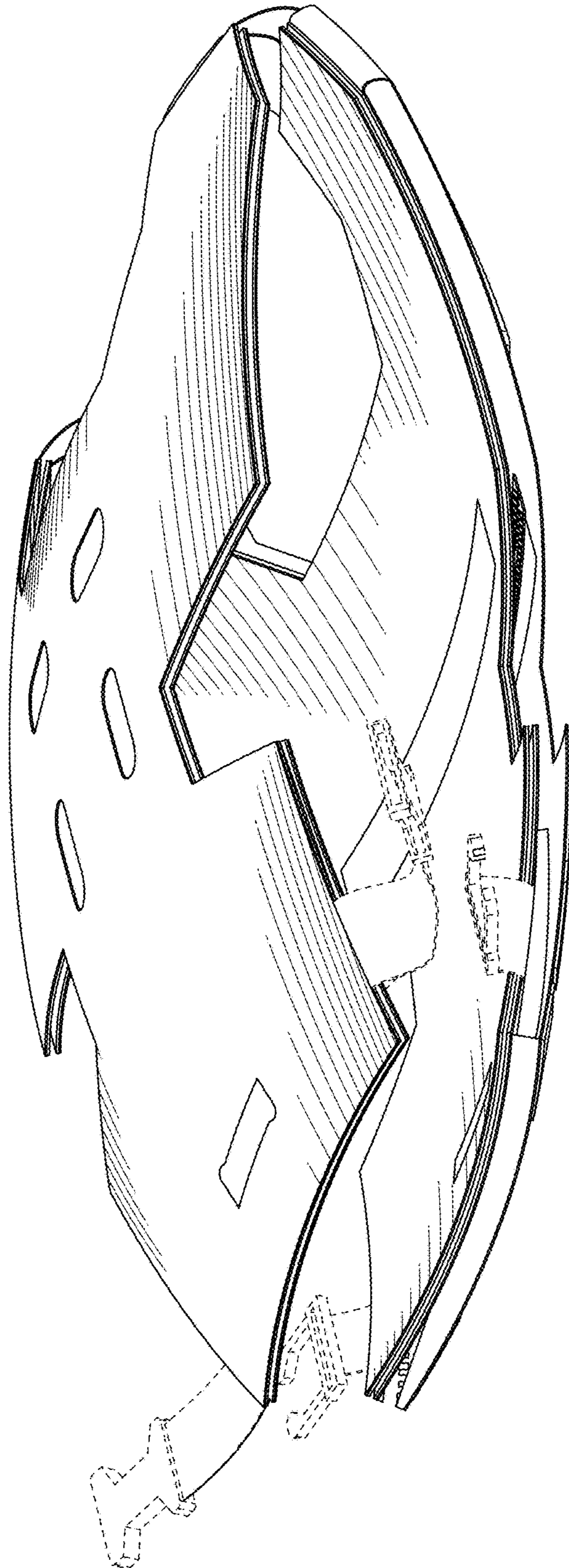


FIG. 7

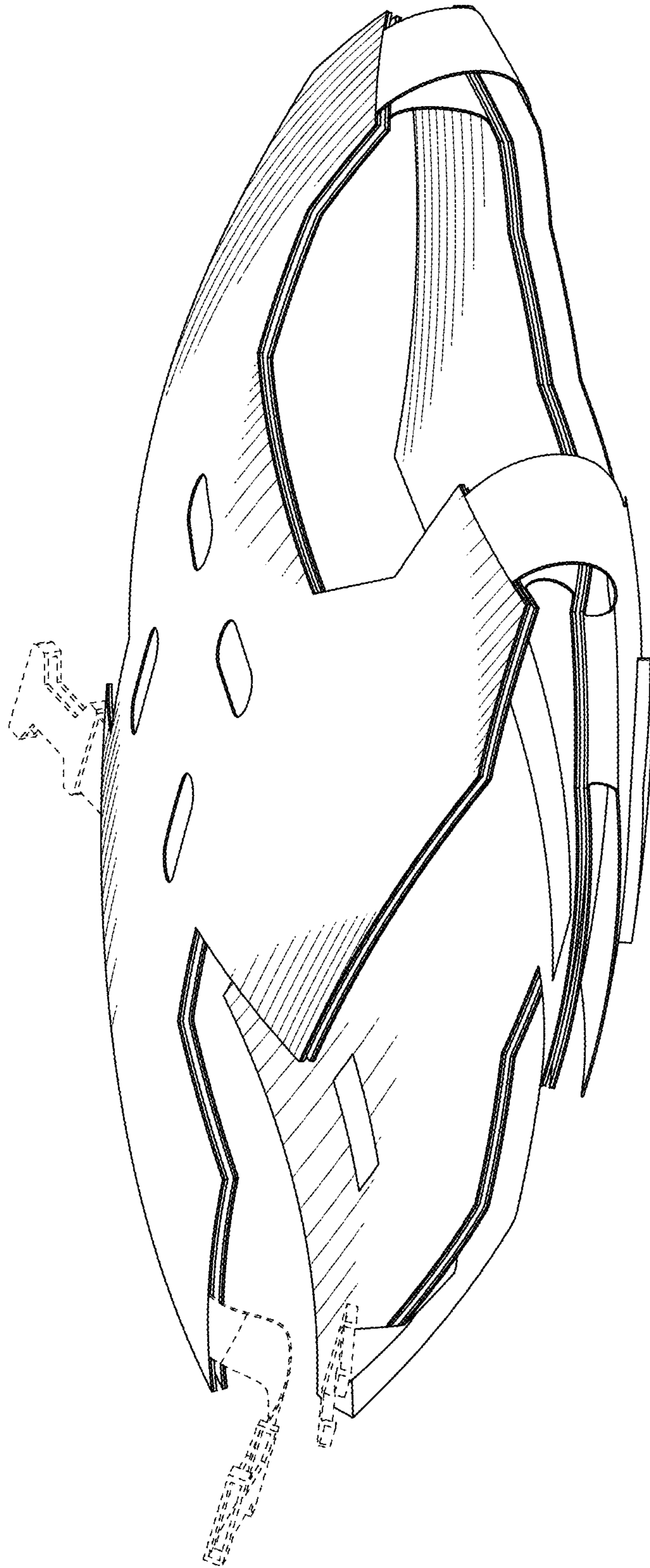


FIG. 8

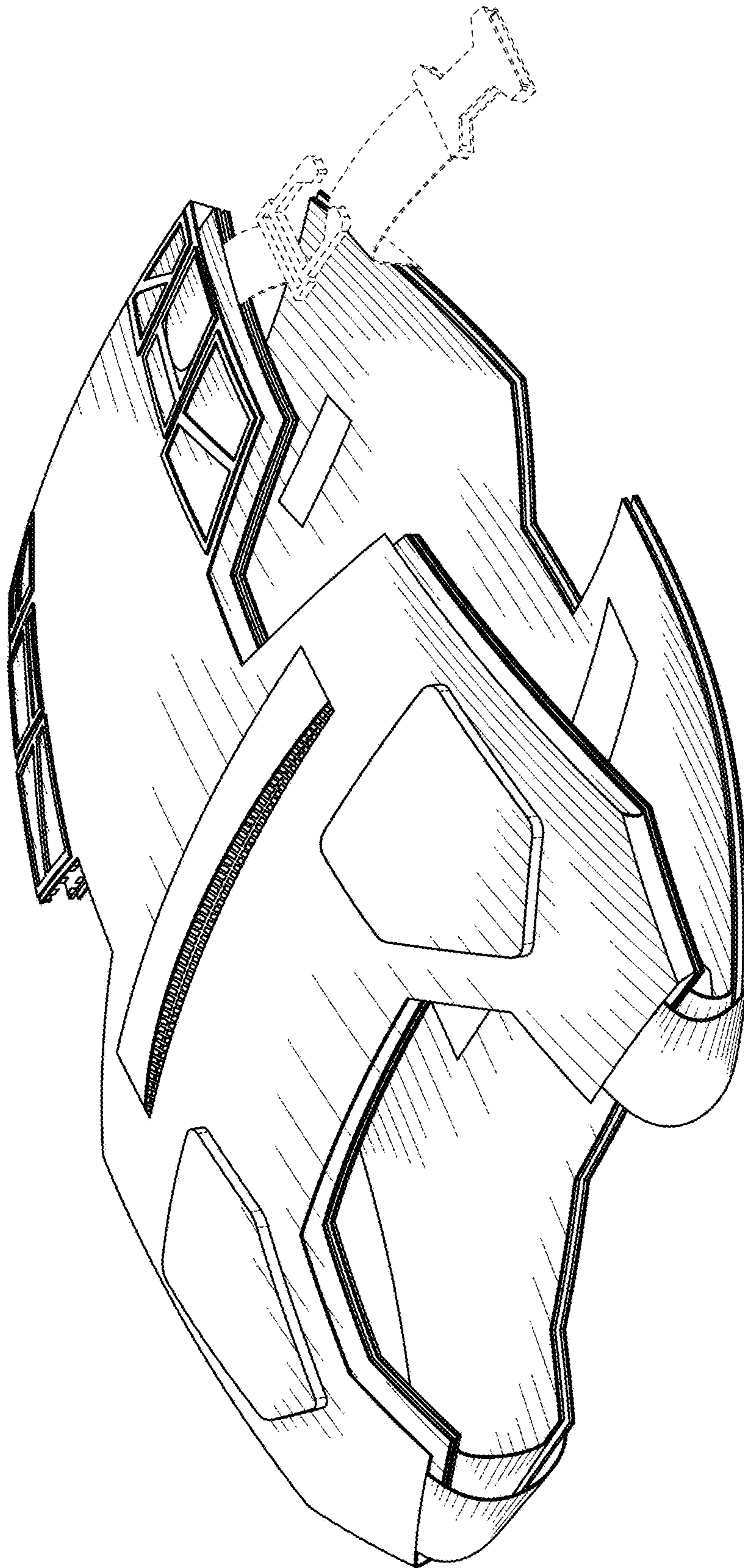


FIG. 9

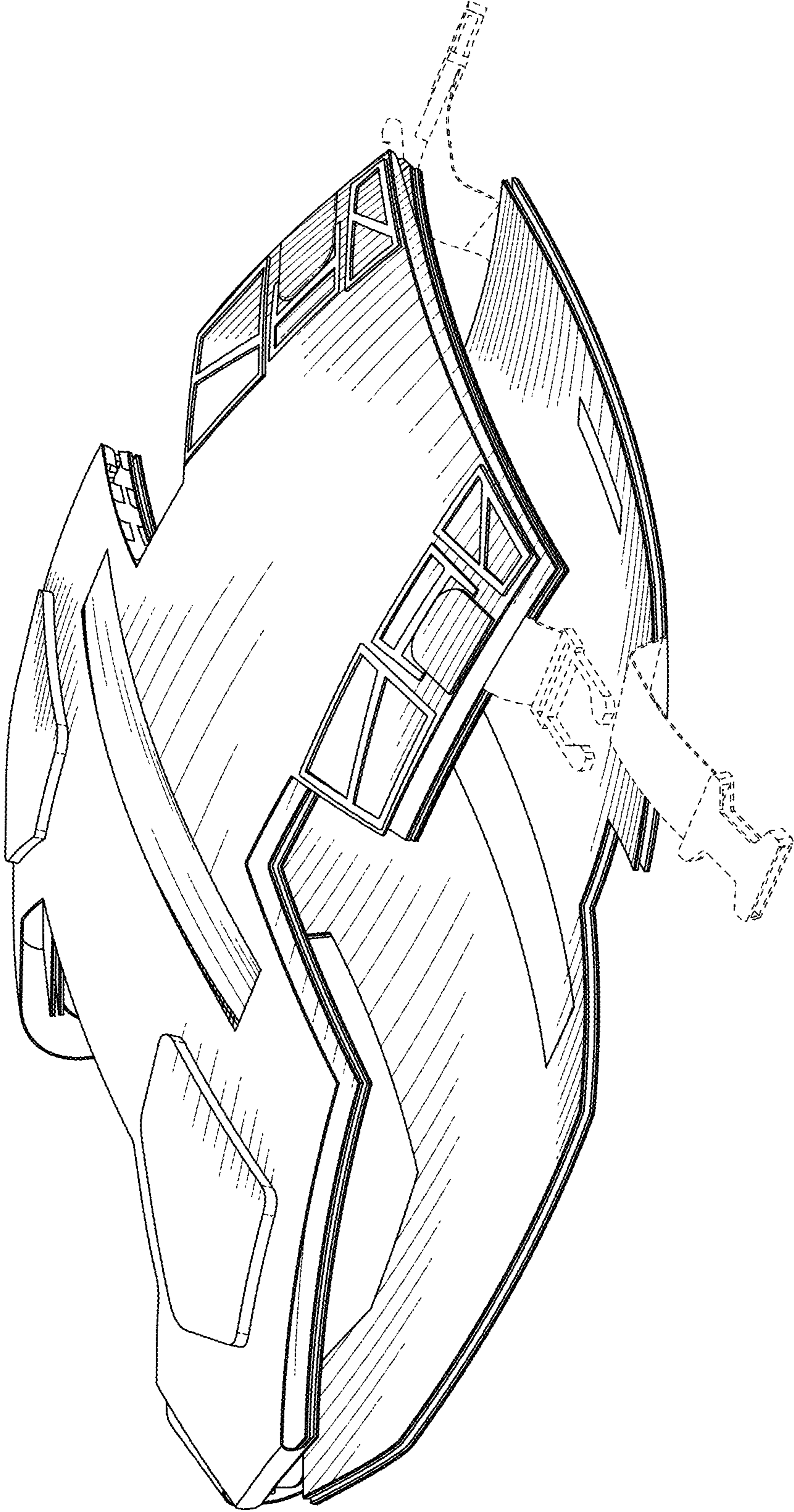


FIG. 10