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(12) **United States Design Patent**
Fukushima et al.

(10) **Patent No.:** **US D813,180 S**
(45) **Date of Patent:** **** Mar. 20, 2018**

(54) **ELASTIC MEMBRANE FOR SEMICONDUCTOR WAFER POLISHING APPARATUS**

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(73) Assignee: **EBARA CORPORATION**, Tokyo (JP)

(**) Term: **15 Years**

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Related U.S. Application Data

(62) Division of application No. 29/472,346, filed on Nov. 12, 2013, now Pat. No. Des. 769,200.

(30) **Foreign Application Priority Data**

May 15, 2013 (JP) 2013-10672
May 15, 2013 (JP) 2013-10673

(Continued)

(51) **LOC (11) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182; 451/66, 288, 289

(Continued)

(56) **References Cited**

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Primary Examiner — Elizabeth J Oswecki

(74) *Attorney, Agent, or Firm* — Pearne & Gordon LLP

(57) **CLAIM**

The ornamental design for an elastic membrane for semiconductor wafer polishing apparatus, as shown and described.

DESCRIPTION

FIG. 1 is a top plan view of a first embodiment of an elastic membrane for semiconductor wafer polishing apparatus showing our new design;

FIG. 2 is a bottom plan view thereof;

FIG. 3 is a front side view thereof;

FIG. 4 is a right side view thereof;

FIG. 5 is a left side view thereof;

FIG. 6 is a cross sectional view taken along section line 6-6 in FIG. 1;

FIG. 7 is an enlarged perspective view of a portion labeled FIG. 7 in FIG. 1;

FIG. 8 is an opposite side view of FIG. 7;

FIG. 9 is a top plan view of a second embodiment of an elastic membrane for semiconductor wafer polishing apparatus showing our new design;

FIG. 10 is a bottom plan view thereof;

FIG. 11 is a front side view thereof;

FIG. 12 is a right side view thereof;

FIG. 13 is a left side view thereof;

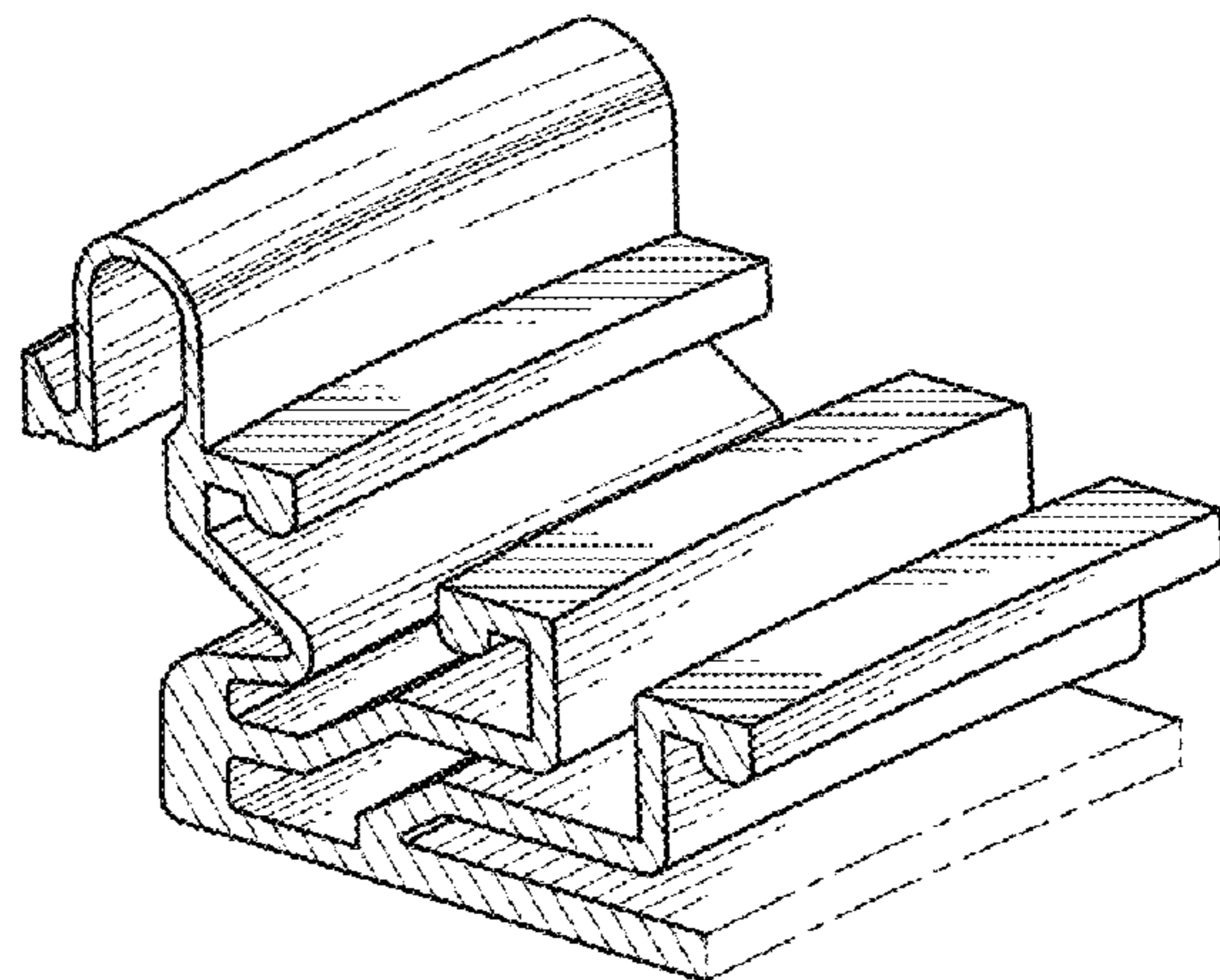
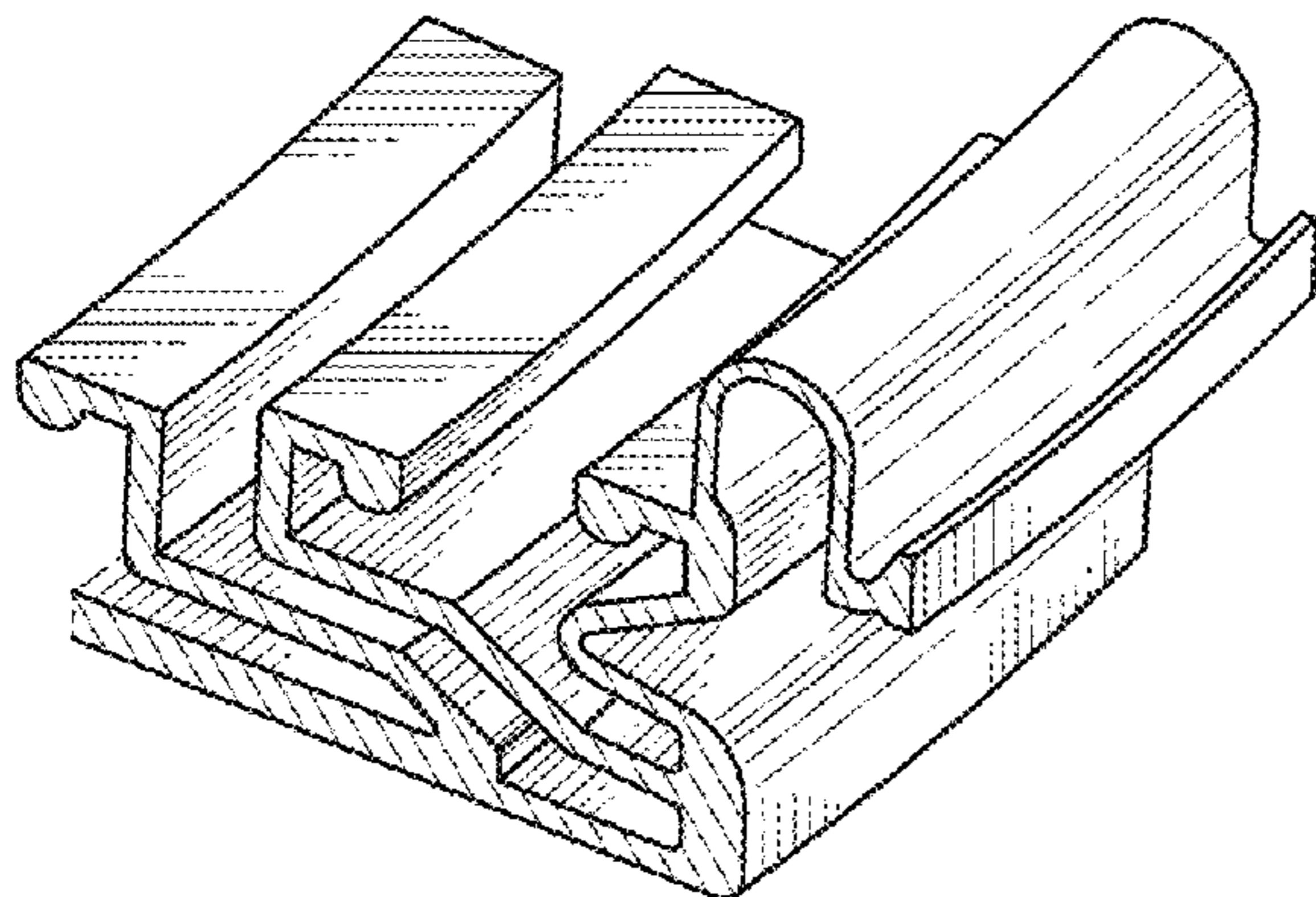
FIG. 14 is a cross sectional view taken along section line 14-14 in FIG. 9;

FIG. 15 is an enlarged perspective view of a portion labeled FIG. 15 in FIG. 9; and,

FIG. 16 is an opposite side view of FIG. 15.

The broken lines shown in the drawings represent portions of the elastic membrane for semiconductor wafer polishing apparatus that form no part of the claimed design. The

(Continued)



dashed-dot-dashed lines represent the boundary lines of the claimed design.

All surfaces not shown form no part of the claimed design.

1 Claim, 6 Drawing Sheets

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 May 15, 2013 (JP) 2013-10676
 May 15, 2013 (JP) 2013-10677
 May 15, 2013 (JP) 2013-10678

(58) Field of Classification Search

CPC B24B 37/30; B24B 41/061; B24B 49/16
 See application file for complete search history.

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FIG. 1

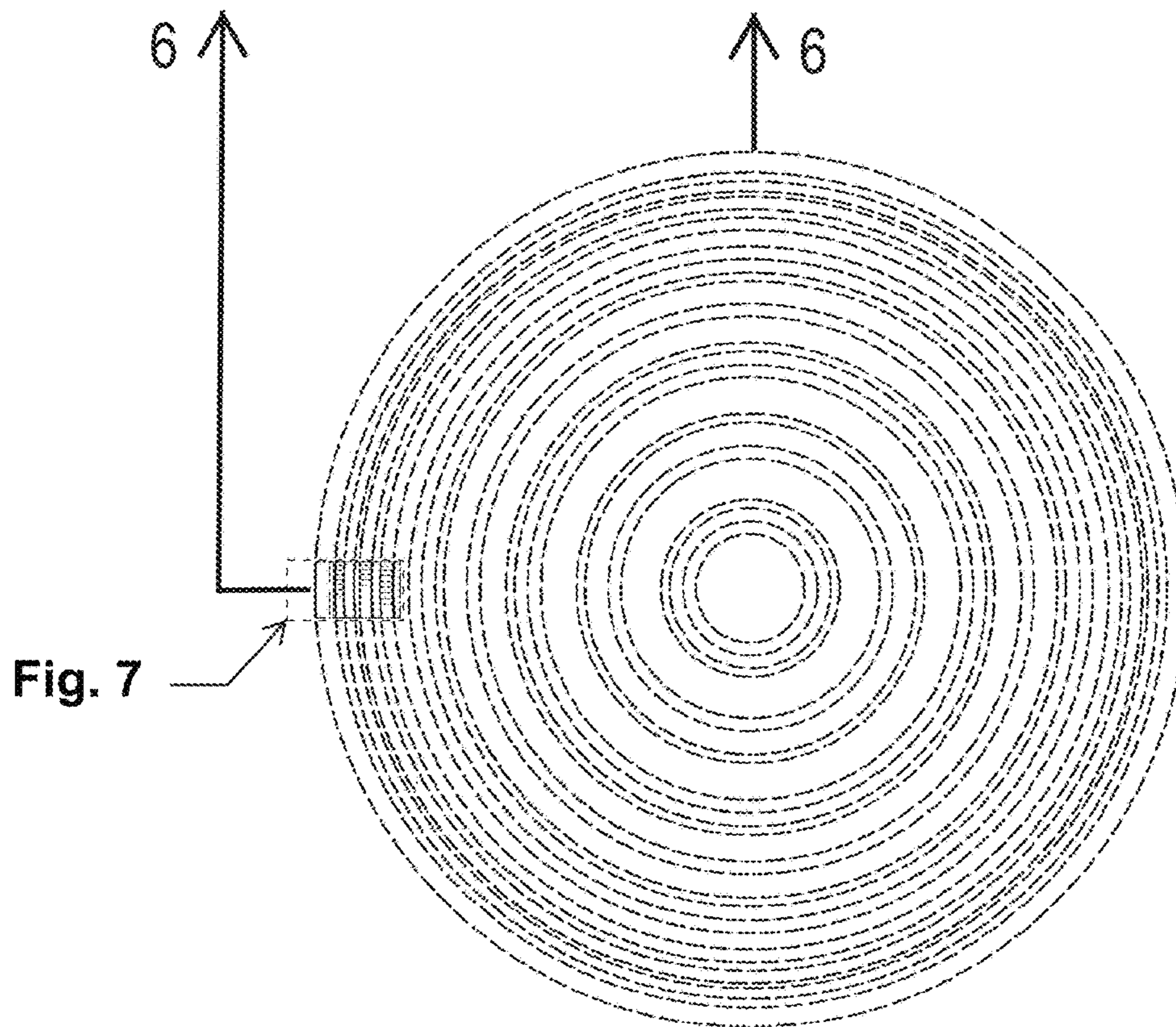


FIG. 2

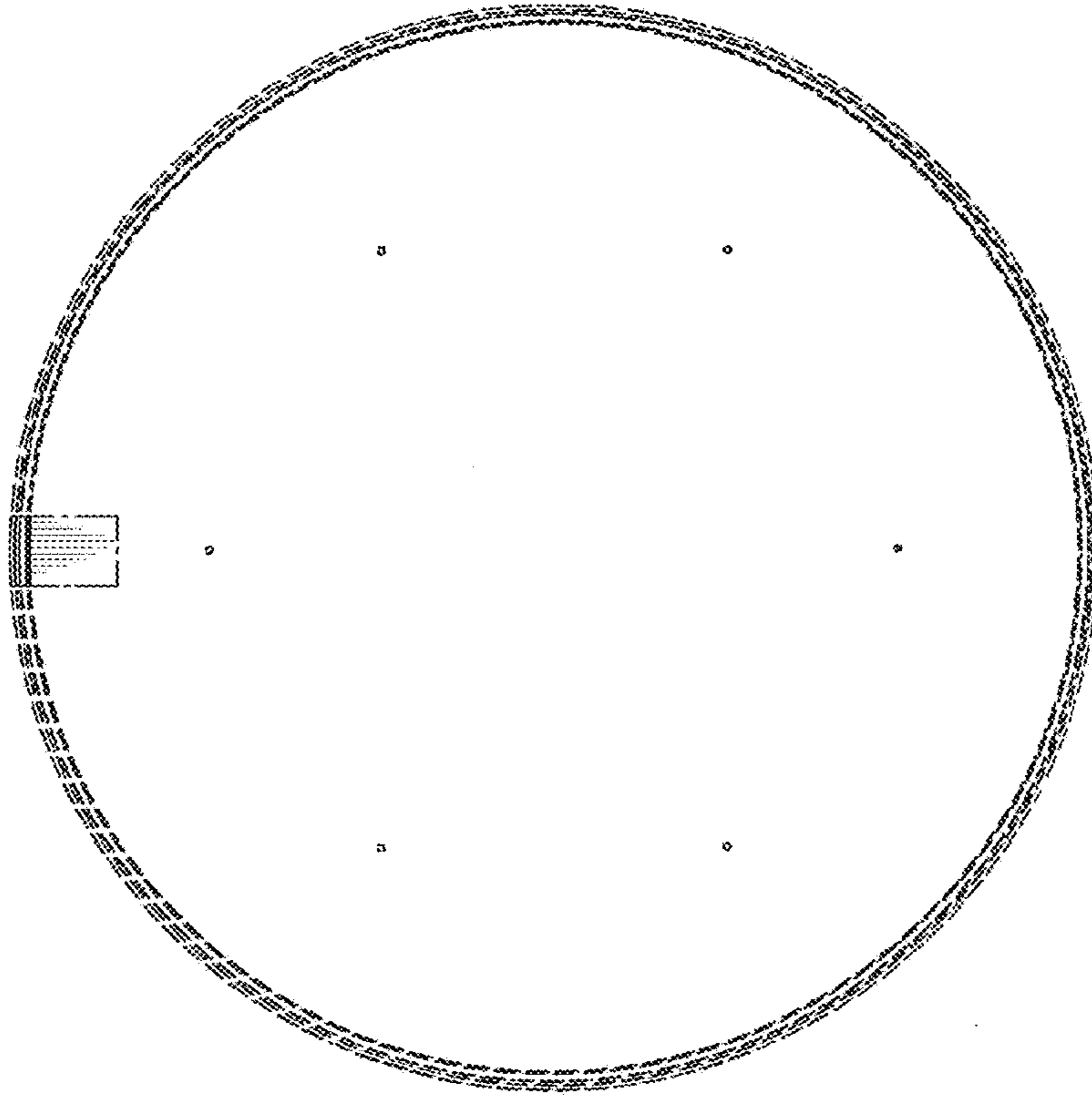


FIG. 3

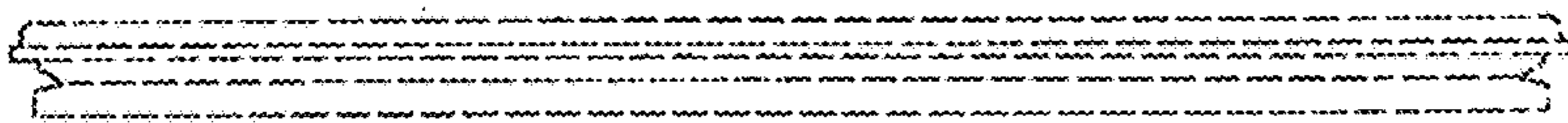


FIG. 4

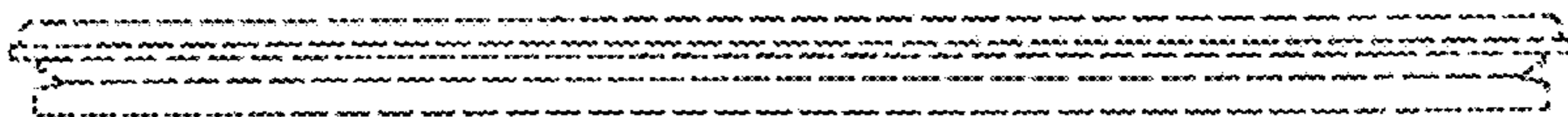


FIG. 5

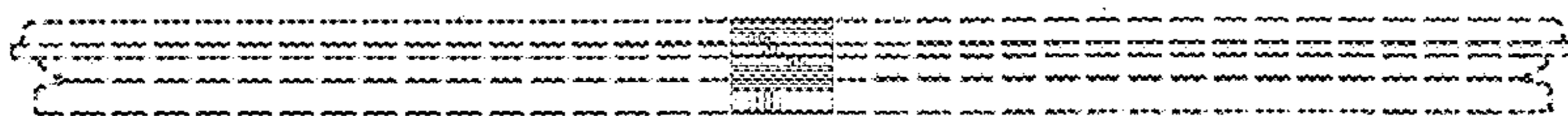


FIG.6

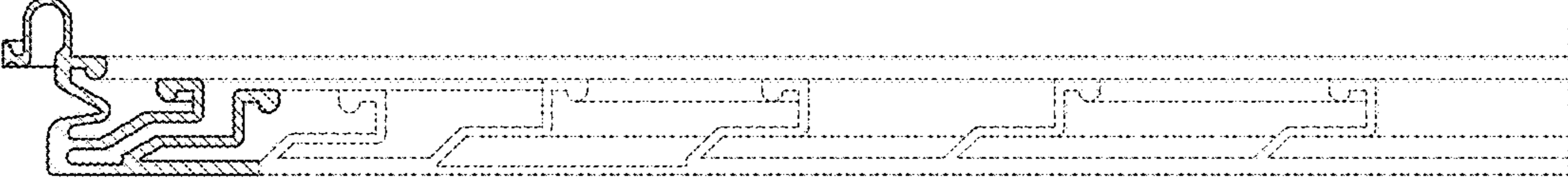


FIG.7

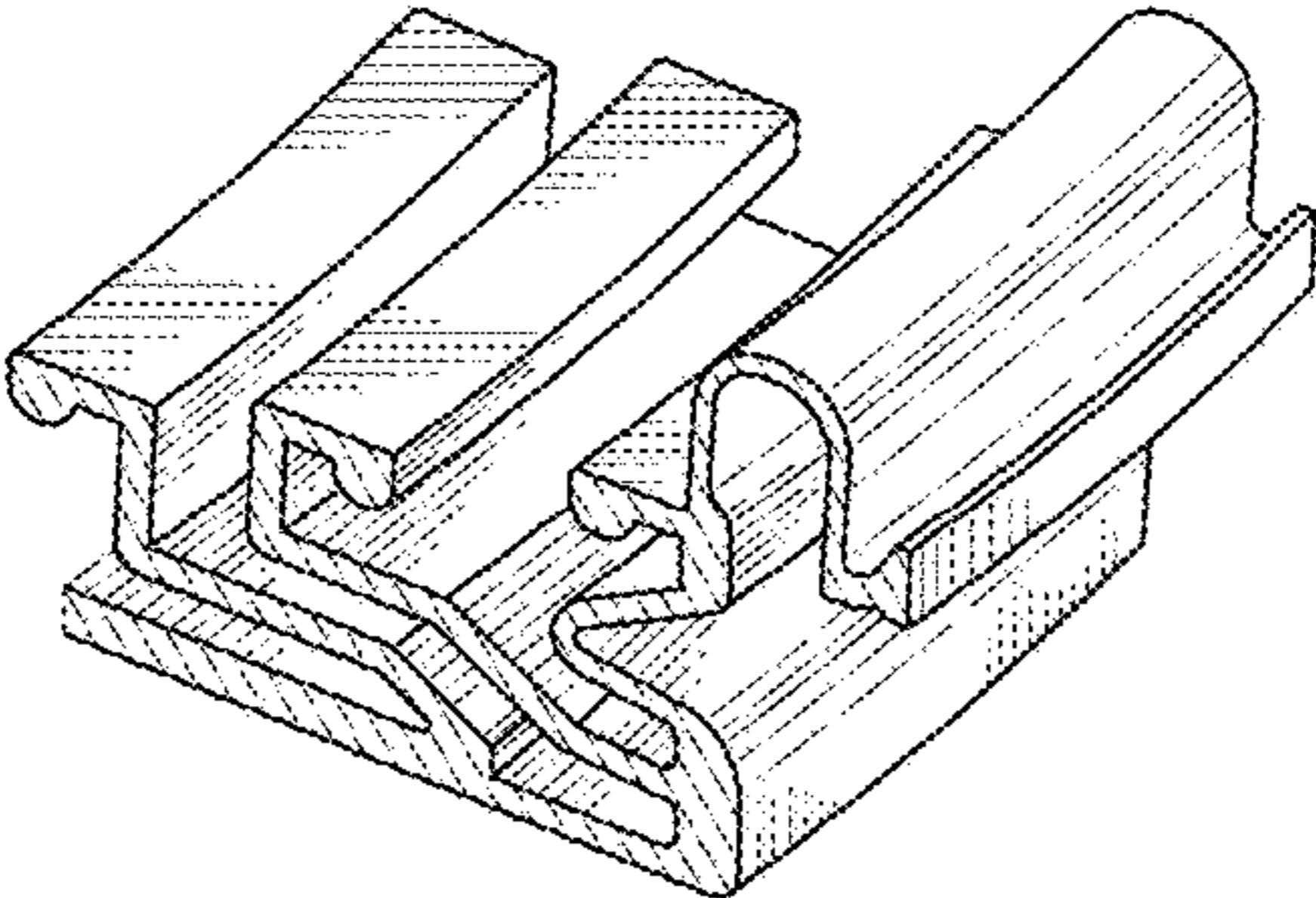


FIG.8

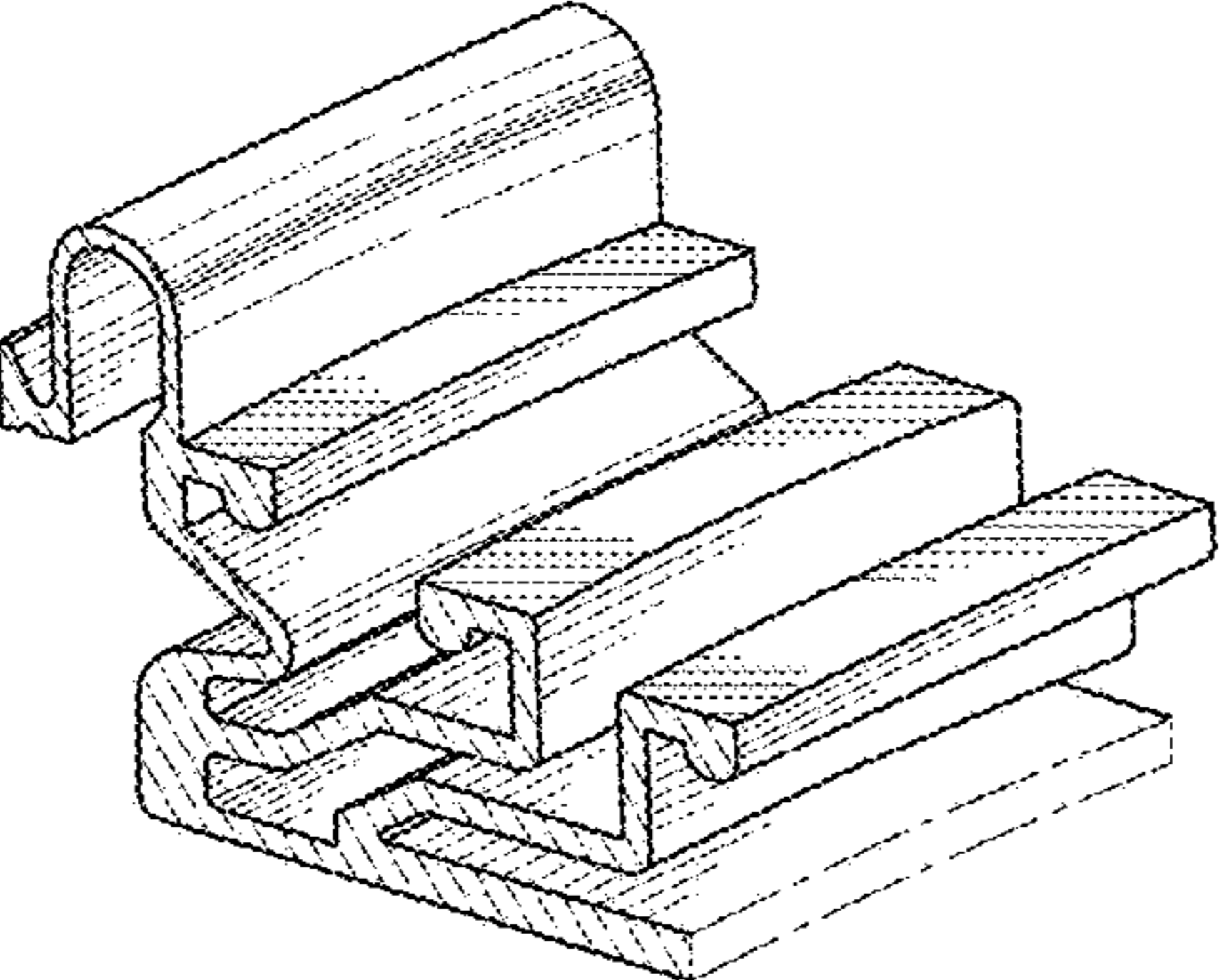


FIG. 9

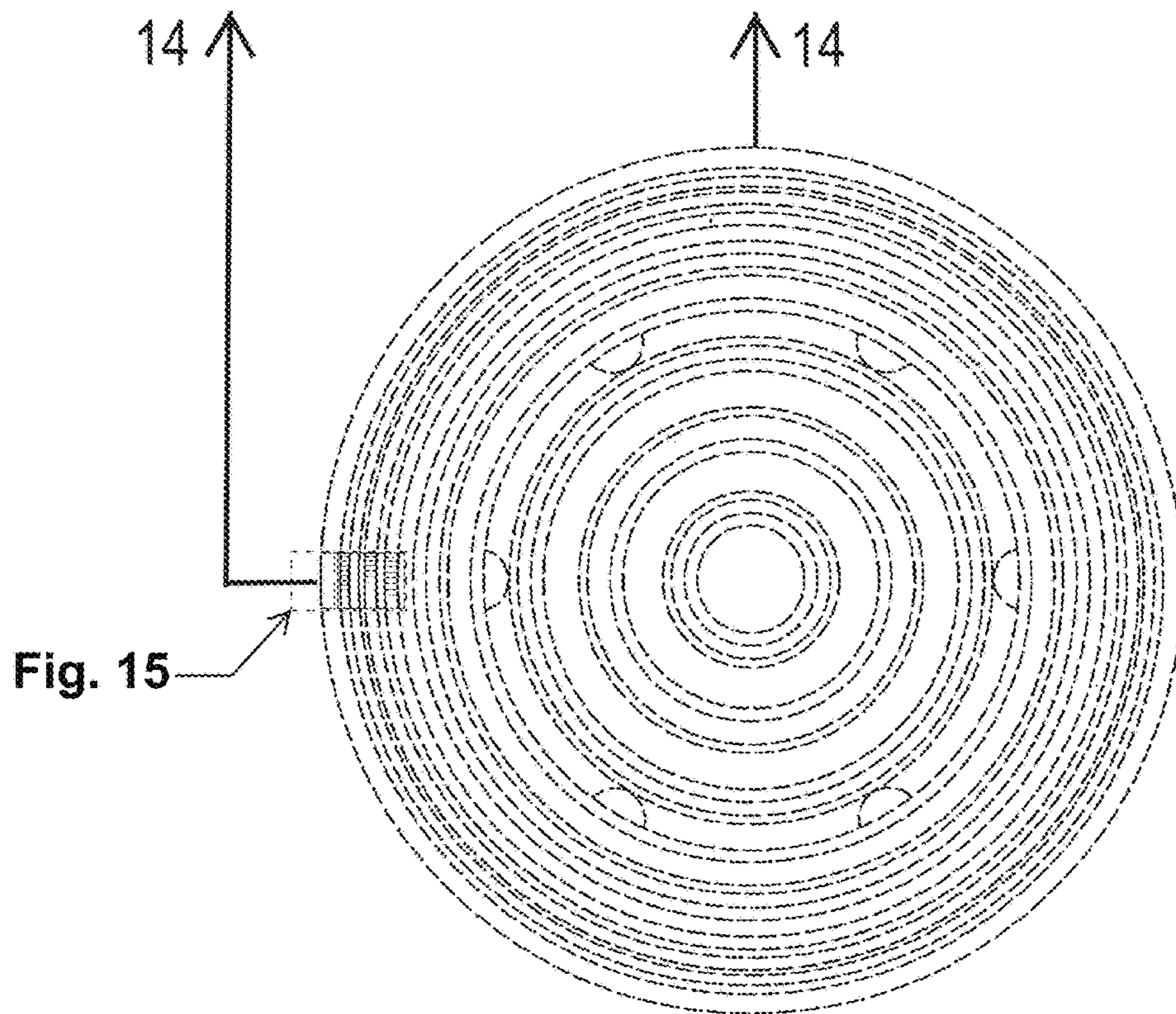


FIG. 10

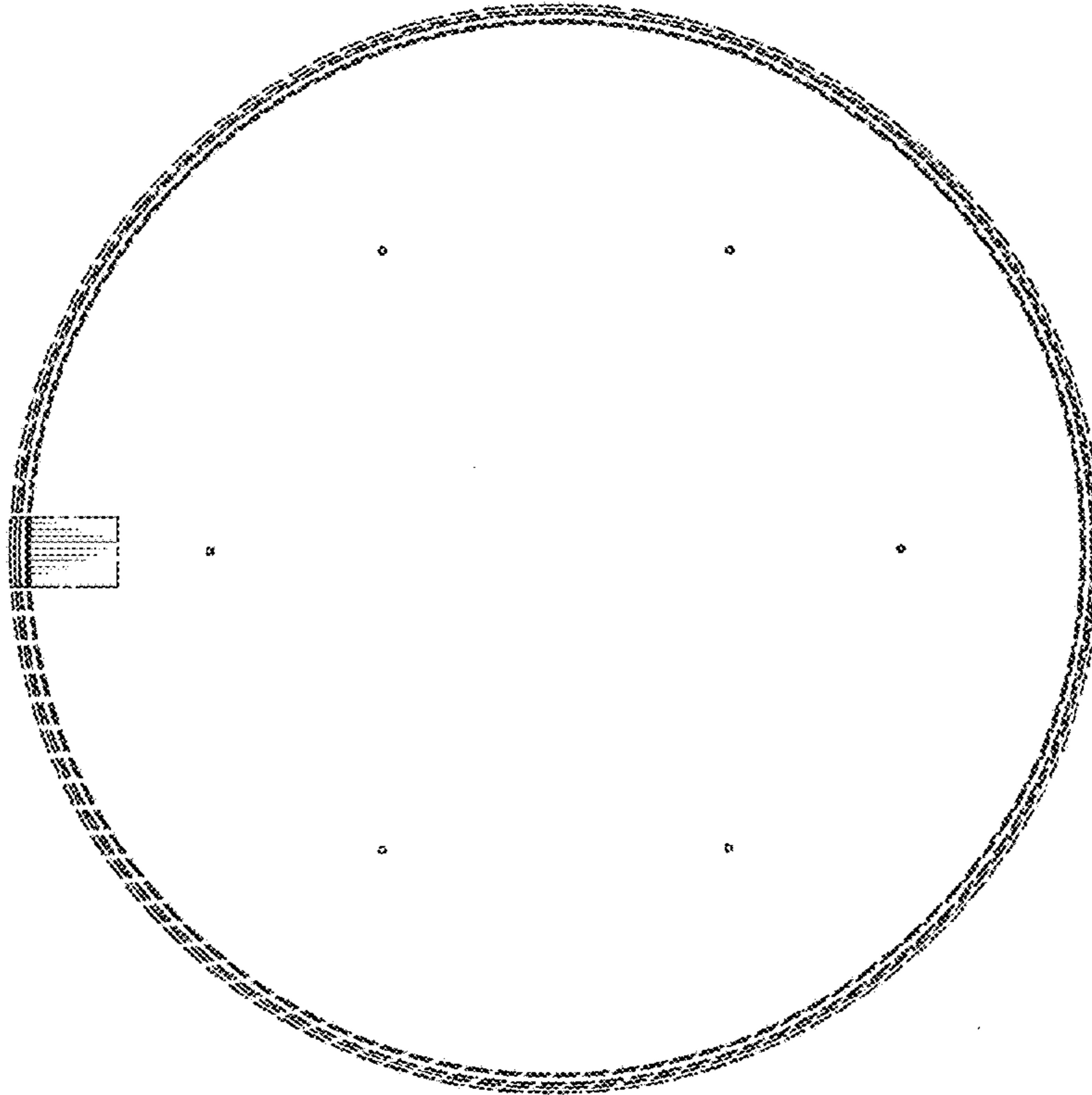


FIG. 11

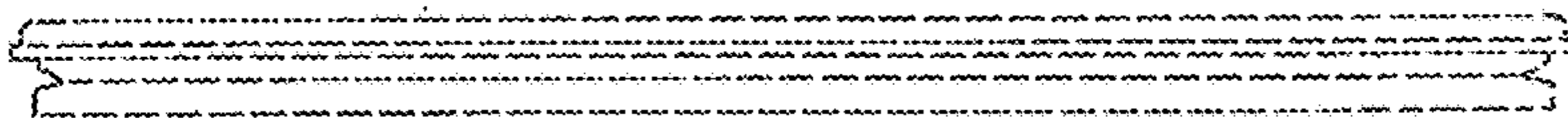


FIG. 12

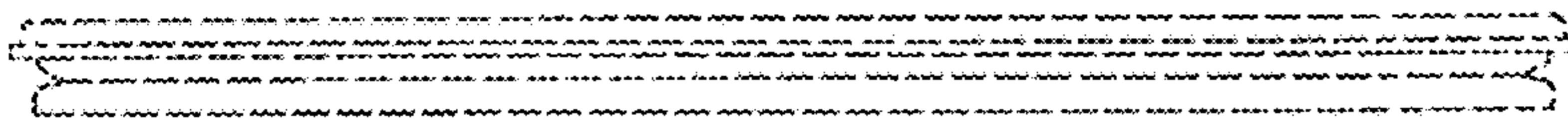


FIG. 13

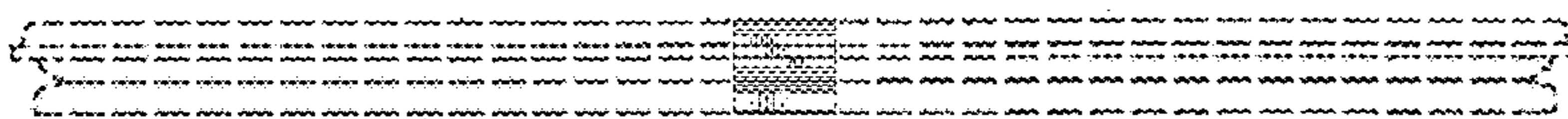


FIG. 14

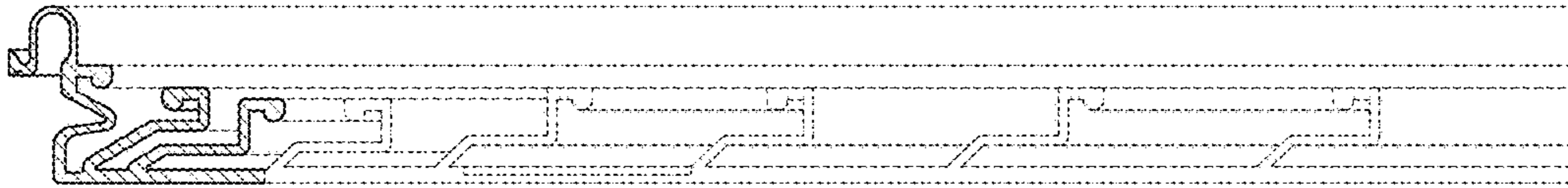


FIG. 15

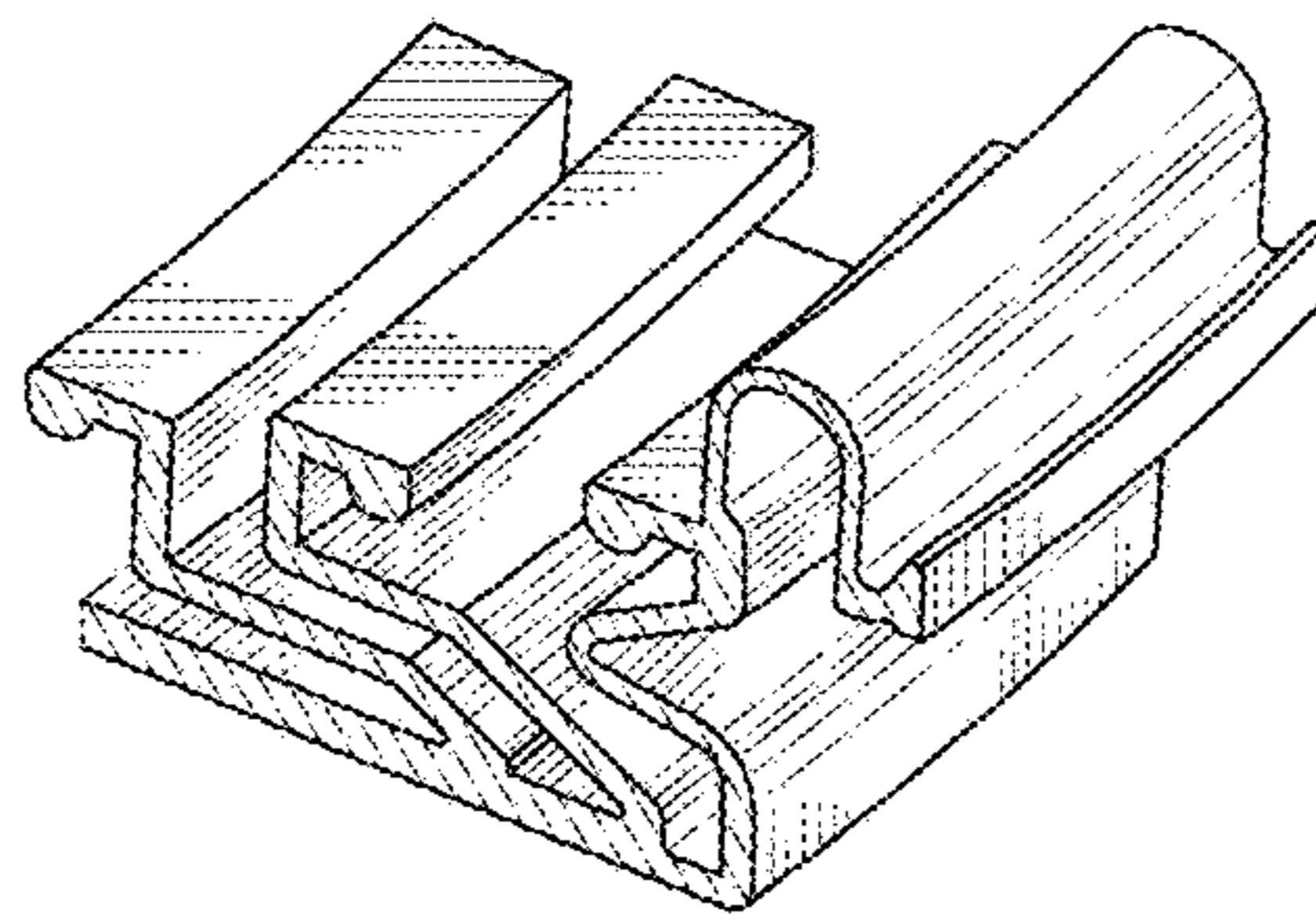


FIG. 16

