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(12) **United States Design Patent**  
**Hochman et al.**

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(54) **ELECTRONICS ENCLOSURE**

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(\*\*) Term: **15 Years**

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(51) **LOC (10) Cl.** ..... **13-99**

(52) **U.S. Cl.**  
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(58) **Field of Classification Search**  
USPC ..... D14/356-358, 361, 362, 365, 367, 370,  
D14/388, 432, 496, 125, 140, 142, 155,  
D14/168, 240, 243, 299, 188, 300, 301;  
D13/103, 107, 108, 123, 152, 158, 159,  
D13/162.1, 182, 199, 110, 151, 162, 184,  
D13/179, 180  
CPC ..... H05B 37/00; H05B 41/00; H05B 39/00;  
H05B 39/02; H05B 39/04; H05B 39/041;  
H05B 39/045; H05B 39/08; G06F 1/00;  
G06F 1/02; G06F 1/1635; G06F 1/18;  
G06F 1/181; G06F 1/189; G06F 1/206;  
G06F 21/00; H05K 5/00

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

D267,949 S \* 2/1983 Hisatsune ..... D14/188  
D281,315 S \* 11/1985 Kjeld ..... D13/179  
D335,670 S \* 5/1993 Kerr ..... D13/184  
D368,261 S \* 3/1996 Shushurin ..... D13/110  
D377,335 S \* 1/1997 Katooka ..... D13/110

D386,148 S \* 11/1997 Katooka ..... D13/110  
D400,167 S \* 10/1998 Klaus ..... D13/110  
D402,627 S \* 12/1998 Klaus ..... D13/110  
D421,598 S 3/2000 Berusha et al.  
D429,225 S \* 8/2000 Halliday ..... D13/184  
D431,816 S \* 10/2000 Beaumont ..... D14/188

(Continued)

FOREIGN PATENT DOCUMENTS

CA 81279 7/1997

OTHER PUBLICATIONS

Aitech, Embedded Computing Without Compromise, Dual VME Slot Enclosure (Jun. 29, 2017).

(Continued)

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(57) **CLAIM**

The ornamental design for an electronics enclosure, as shown and described.

**DESCRIPTION**

FIG. 1 is a perspective view of an electronics enclosure showing our new design;

FIG. 2 is an end view thereof;

FIG. 3 is a second end view thereof;

FIG. 4 is a side view thereof;

FIG. 5 is a second side view thereof;

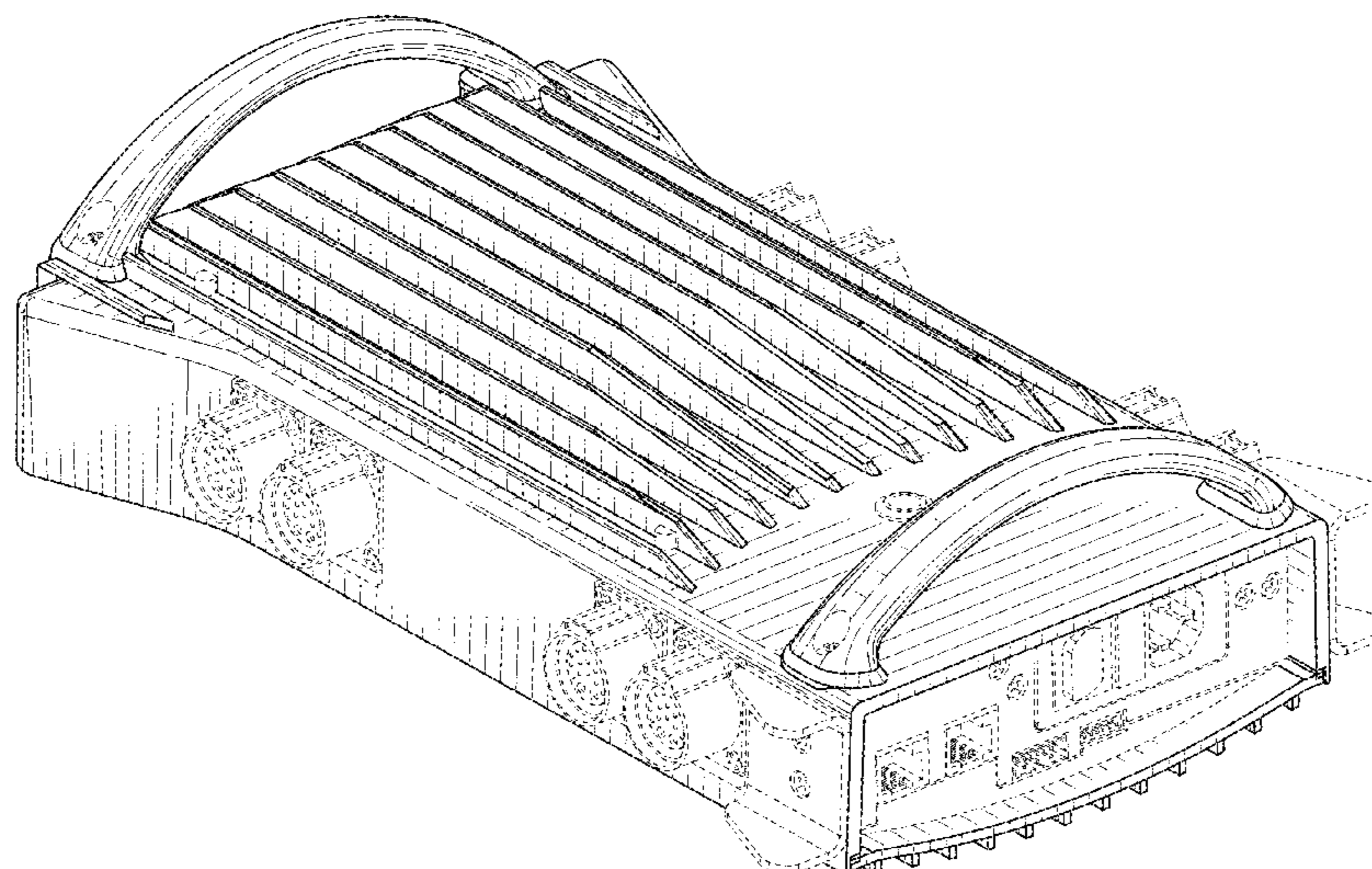
FIG. 6 is a top view thereof; and,

FIG. 7 is a bottom view thereof.

The broken lines in the Figures are for the purpose of illustrating unclaimed portions of the electronics enclosure and form no part of the claimed design.

The shade lines in the Figures show contour and not surface ornamentation.

**1 Claim, 5 Drawing Sheets**



(56)

References Cited

U.S. PATENT DOCUMENTS

D436,918 S \* 1/2001 Matsuda ..... D13/110  
 D437,288 S \* 2/2001 Light ..... D13/110  
 D464,327 S \* 10/2002 Frank, Jr. .... D13/162  
 D469,401 S \* 1/2003 Griffey ..... D13/110  
 D474,738 S \* 5/2003 Ishii ..... D13/110  
 D479,195 S \* 9/2003 Krieger ..... D13/110  
 D486,446 S \* 2/2004 Hriscu ..... D13/110  
 D489,682 S \* 5/2004 Guillarme ..... D13/110  
 D499,074 S 11/2004 Cook et al.  
 D503,676 S \* 4/2005 Krieger ..... D13/110  
 D505,915 S \* 6/2005 Hussaini ..... D13/110  
 D507,528 S \* 7/2005 Feldman ..... D13/102  
 D510,736 S \* 10/2005 Chen ..... D14/300  
 D513,247 S \* 12/2005 Matsuoka ..... D14/188  
 D516,554 S 3/2006 Richardson et al.  
 D520,985 S \* 5/2006 Ishinabe ..... D14/188  
 D538,260 S \* 3/2007 Wada ..... D14/188  
 D538,742 S \* 3/2007 Pickvet ..... D13/110  
 D540,253 S \* 4/2007 Tsai ..... D13/110  
 D546,282 S \* 7/2007 Wardenburg ..... D13/110  
 D548,695 S \* 8/2007 Krieger ..... D13/110  
 D549,214 S \* 8/2007 Uehara ..... D14/188  
 D551,621 S \* 9/2007 Iacovelli ..... D13/110  
 D561,688 S \* 2/2008 Hussaini ..... D13/110  
 D565,030 S \* 3/2008 Amit ..... D14/188  
 D577,668 S \* 9/2008 Buck ..... D13/110  
 D585,439 S \* 1/2009 Ching ..... D14/300  
 D586,814 S \* 2/2009 Kramer ..... D14/432  
 D595,647 S \* 7/2009 Shum ..... D13/110  
 D600,698 S \* 9/2009 Kramer ..... D14/432  
 D610,539 S \* 2/2010 Dahan ..... D13/110

D616,376 S \* 5/2010 Lannoch ..... D13/162  
 D617,788 S \* 6/2010 Crisp ..... D14/301  
 D619,104 S \* 7/2010 Boyland ..... D13/162  
 D620,432 S \* 7/2010 Chen ..... D13/101  
 D621,350 S \* 8/2010 Huang ..... D13/110  
 D621,351 S \* 8/2010 Huang ..... D13/110  
 D649,141 S 11/2011 Thomas et al.  
 D655,280 S 3/2012 MacManus et al.  
 D684,130 S \* 6/2013 Vincent ..... D13/184  
 D690,738 S \* 10/2013 York ..... D14/188  
 D697,901 S 1/2014 Gae et al.  
 D709,449 S \* 7/2014 Oba ..... D13/110  
 D713,336 S \* 9/2014 Penn ..... D13/110  
 D716,730 S \* 11/2014 Liu ..... D13/110  
 D721,738 S \* 1/2015 Hochman ..... D14/496  
 D730,333 S 5/2015 Matsumoto  
 D737,817 S \* 9/2015 Starck ..... D14/365  
 D739,347 S \* 9/2015 Huang ..... D13/110  
 D751,998 S \* 3/2016 Hochman ..... D13/180  
 D780,692 S \* 3/2017 Hopponen ..... D13/110  
 D786,204 S \* 5/2017 Hochman ..... D13/184  
 D786,475 S \* 5/2017 Hargreaves ..... D26/76  
 D789,931 S \* 6/2017 Drew ..... D14/357  
 2006/0214592 A1 \* 9/2006 Hopkins ..... H05B 41/00  
 315/56  
 2011/0111636 A1 \* 5/2011 Zheng ..... H01R 31/06  
 439/650

OTHER PUBLICATIONS

Aitech, Embedded Computing Without Compromise, Full ATR Short VME Enclosure (Jun. 29, 2017).

\* cited by examiner

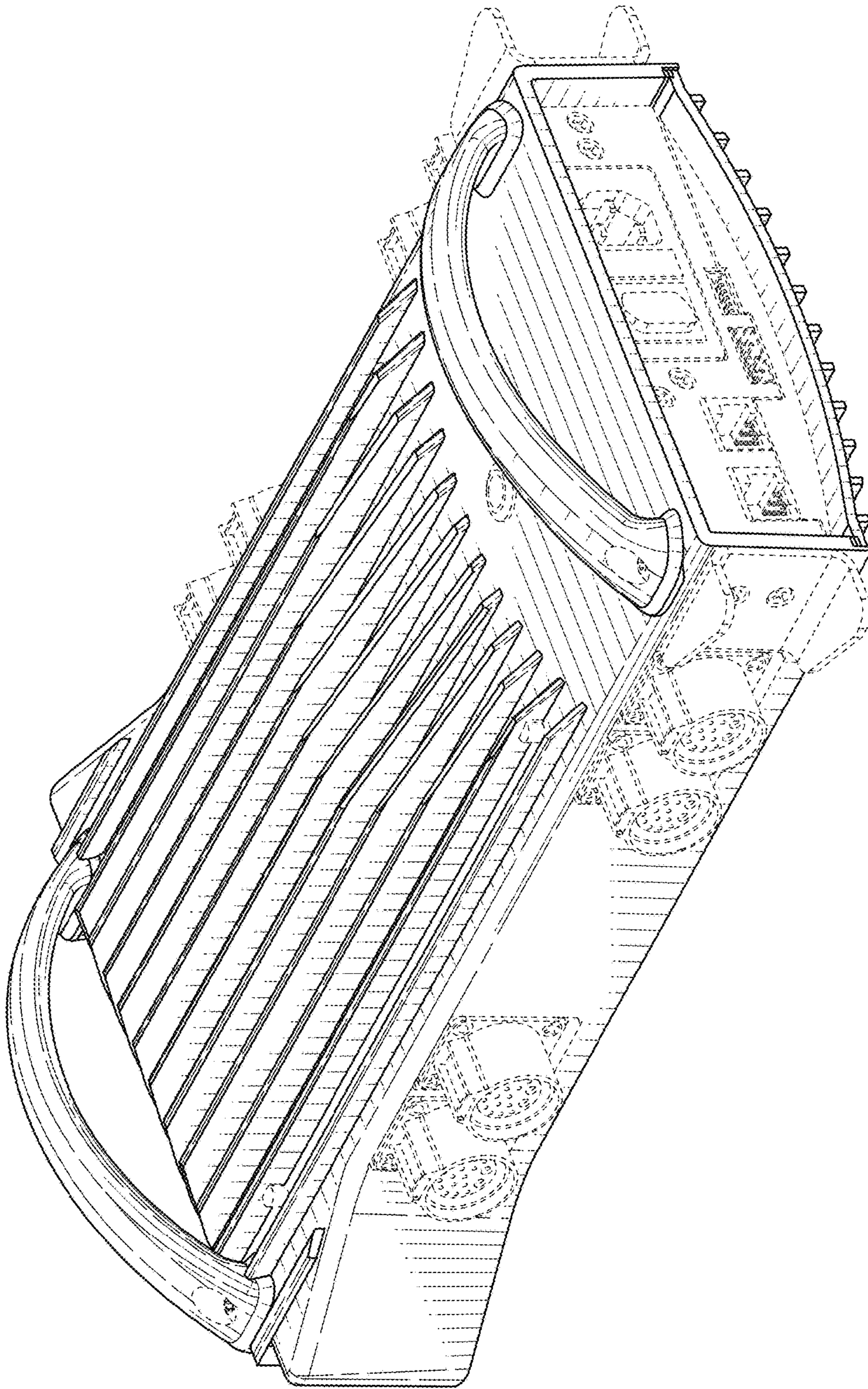


FIG. 1

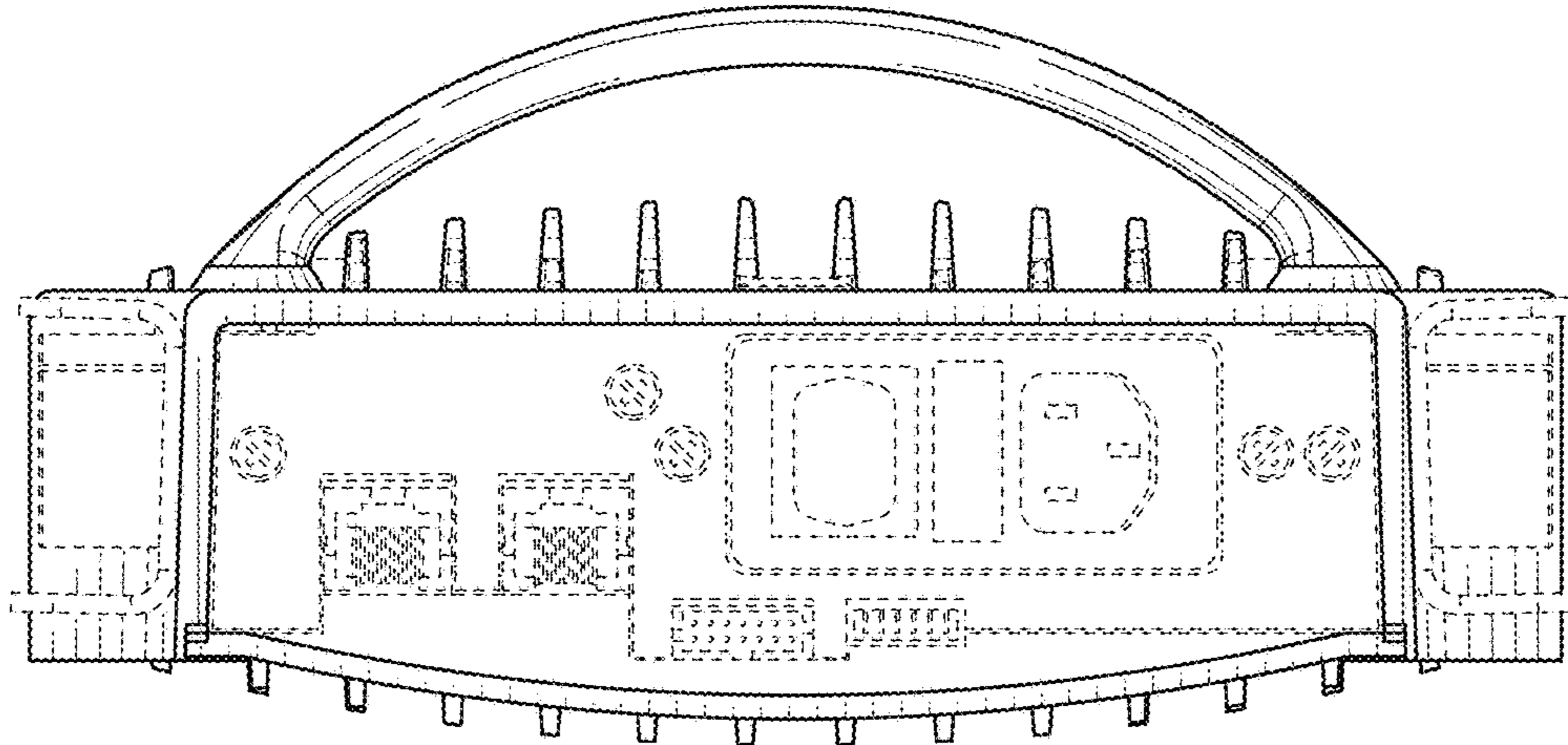


FIG. 2

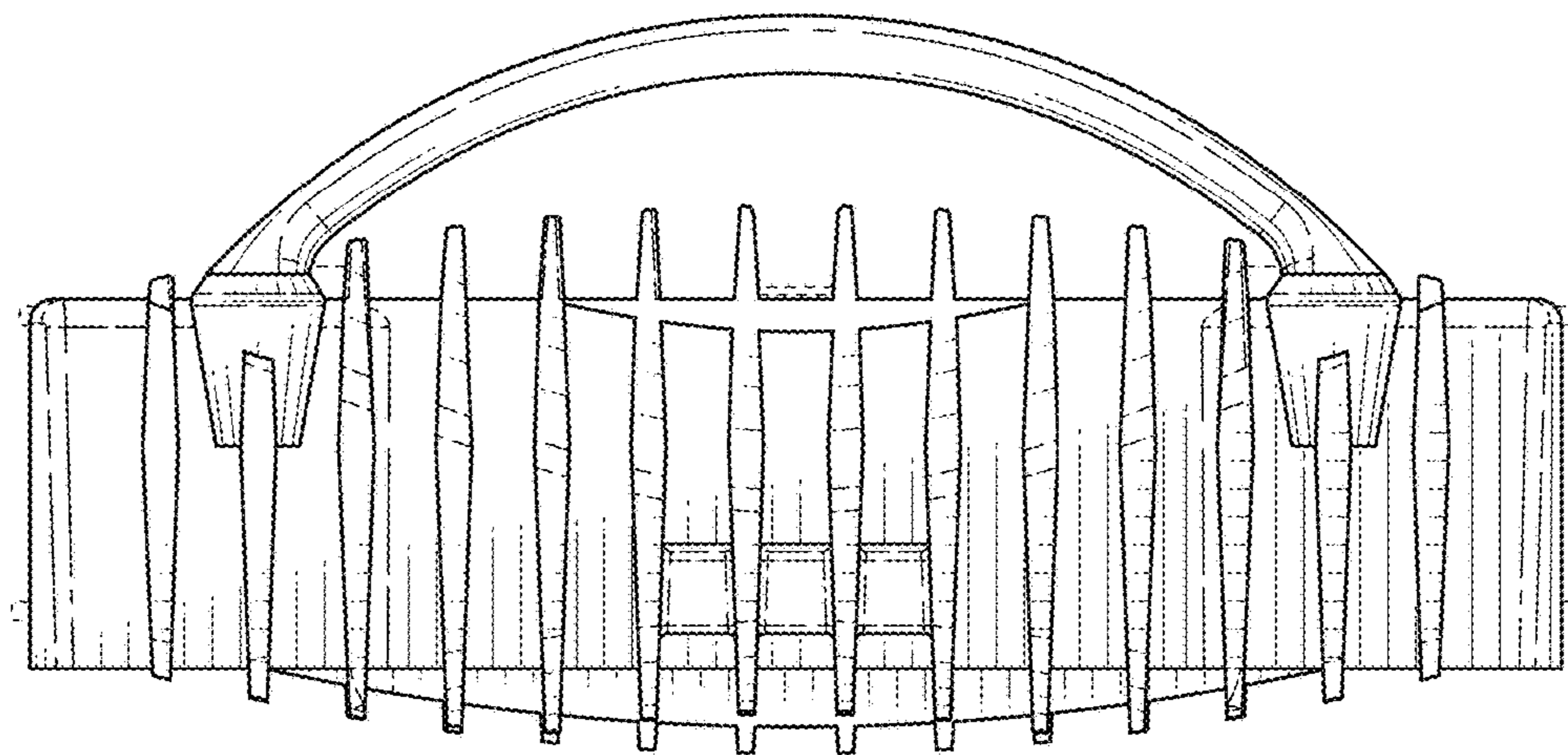


FIG. 3

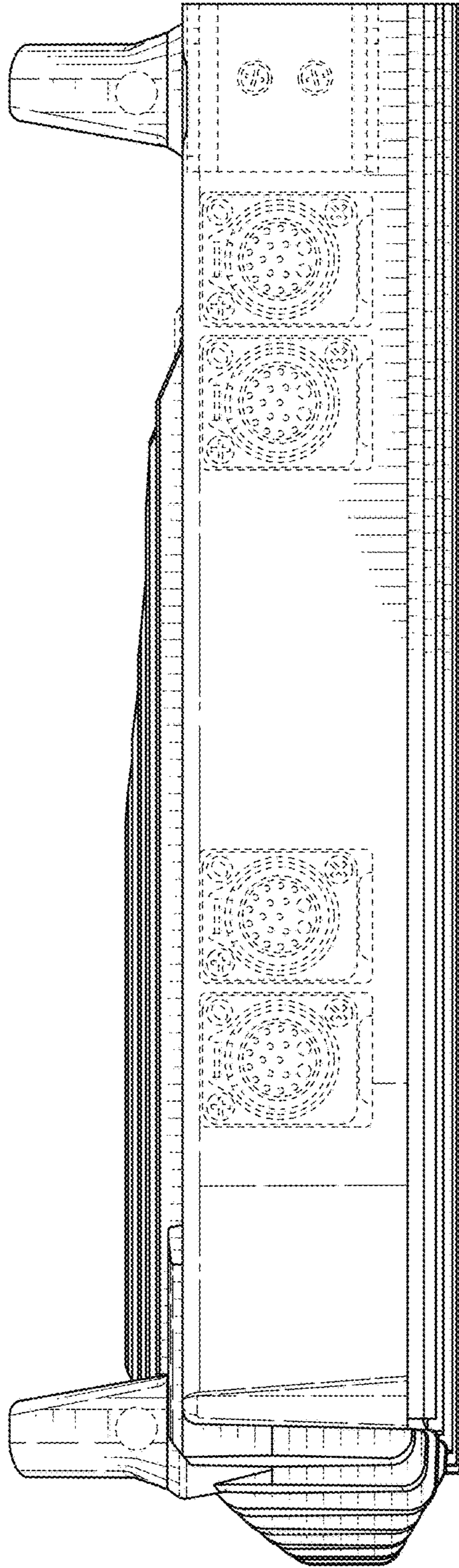


FIG. 4

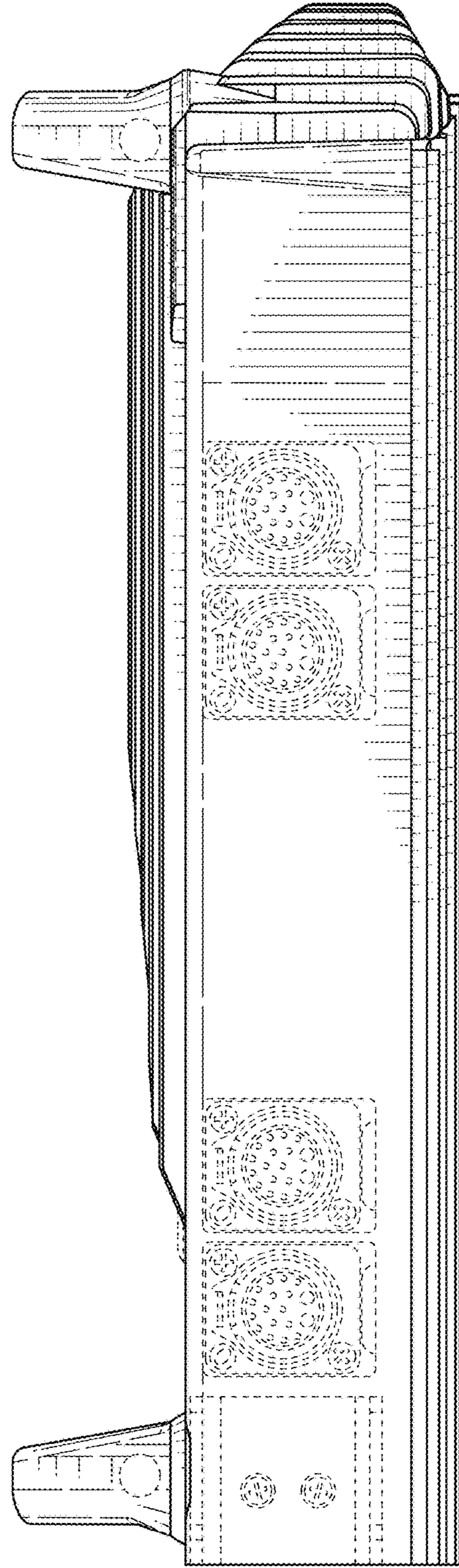


FIG. 5

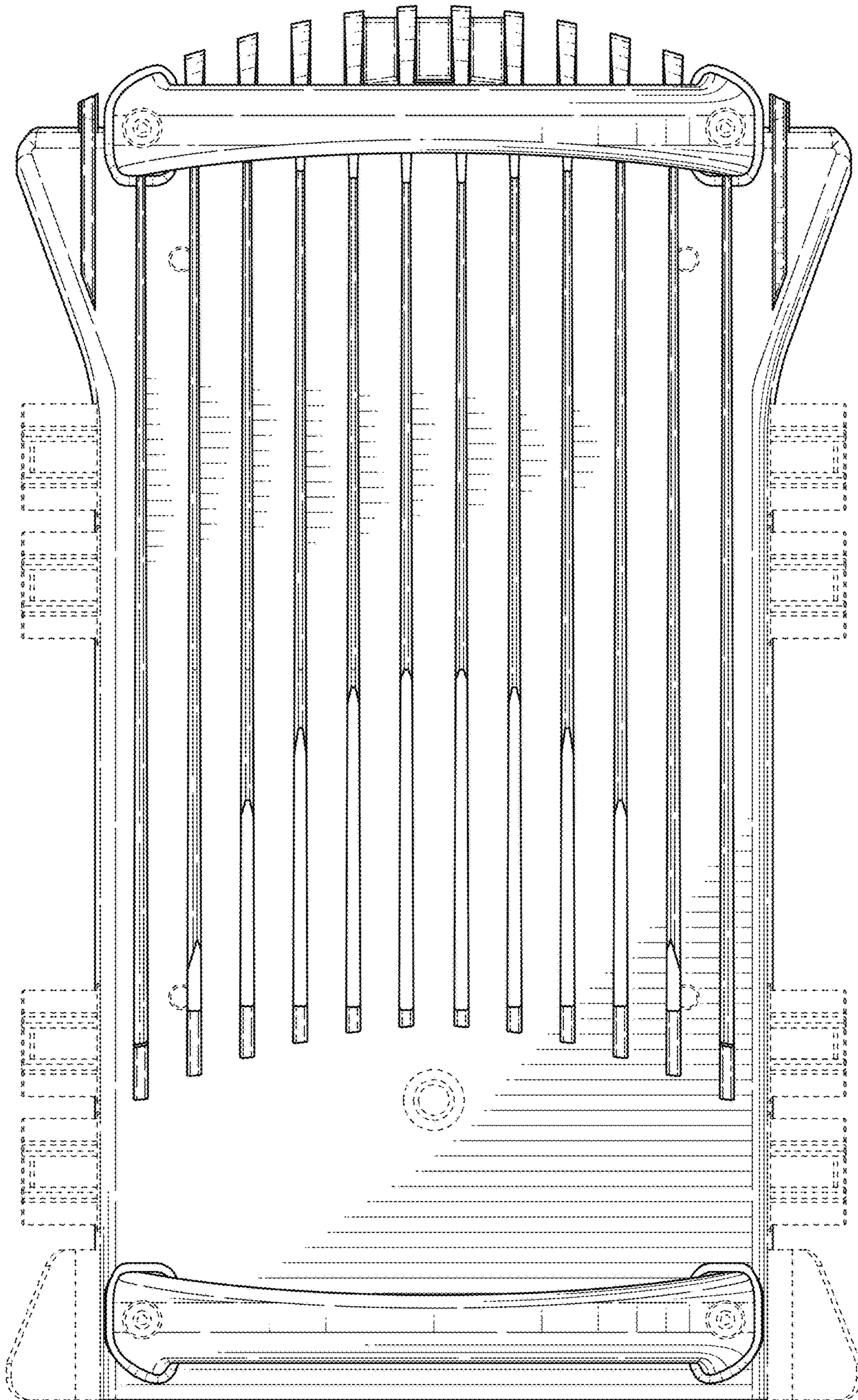


FIG. 6

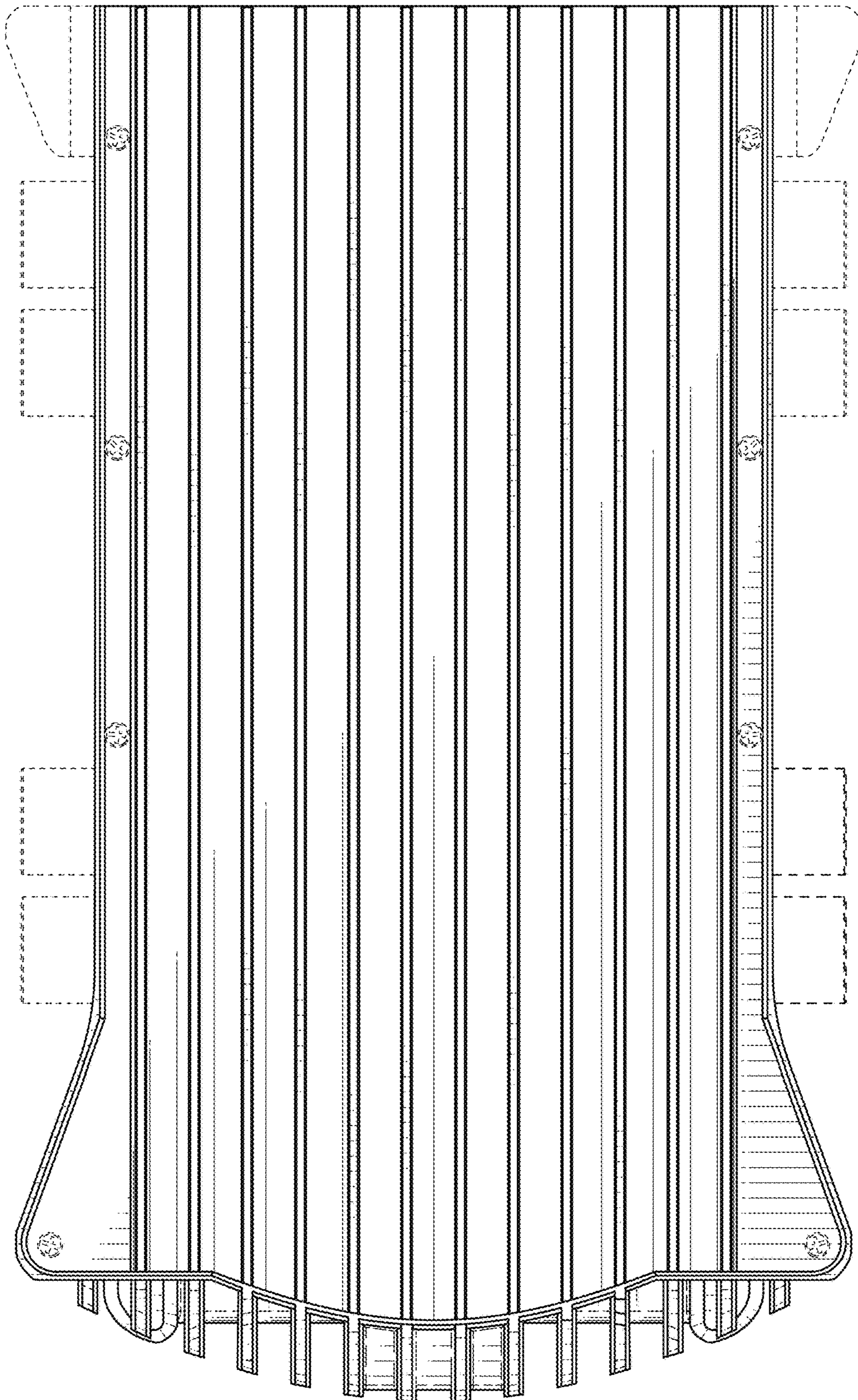


FIG. 7