



US00D805486S

(12) **United States Design Patent** (10) **Patent No.:** **US D805,486 S**
Hochman et al. (45) **Date of Patent:** **** Dec. 19, 2017**

(54) **ELECTRONICS ENCLOSURE**
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(**) Term: **15 Years**

Aitech, Embedded Computing Without Compromise, Dual VME Slot Enclosure (Jun. 29, 2017).

(Continued)

(21) Appl. No.: **29/610,180**

(22) Filed: **Jul. 10, 2017**

(51) **LOC (10) Cl.** **13-99**

Primary Examiner — Susan Bennett Hattan

(52) **U.S. Cl.**

Assistant Examiner — Marie D. Fast Horse

USPC **D13/184**; D13/110; D14/356; D14/300

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(58) **Field of Classification Search**

USPC D14/356–358, 361, 362, 365, 367, 370, D14/388, 432, 496, 125, 140, 142, 155, D14/168, 240, 243, 299, 188, 300, 301; D13/103, 107, 108, 123, 152, 158, 159, D13/162.1, 182, 199, 110, 151, 162, 184, D13/179, 180

(57) **CLAIM**

The ornamental design for an electronics enclosure, as shown and described.

CPC H05B 37/00; H05B 41/00; H05B 39/00; H05B 39/02; H05B 39/04; H05B 39/041; H05B 39/045; H05B 39/08; G06F 1/00; G06F 1/02; G06F 1/1635; G06F 1/18; G06F 1/181; G06F 1/189; G06F 1/206; G06F 21/00; H05K 5/00

DESCRIPTION

See application file for complete search history.

FIG. 1 is a perspective view of an electronics enclosure showing our new design;
FIG. 2 is an end view thereof;
FIG. 3 is a second end view thereof;
FIG. 4 is a side view thereof;
FIG. 5 is a second side view thereof;
FIG. 6 is a top view thereof; and,
FIG. 7 is a bottom view thereof.

The broken lines in the Figures are for the purpose of illustrating unclaimed portions of the electronics enclosure and form no part of the claimed design.

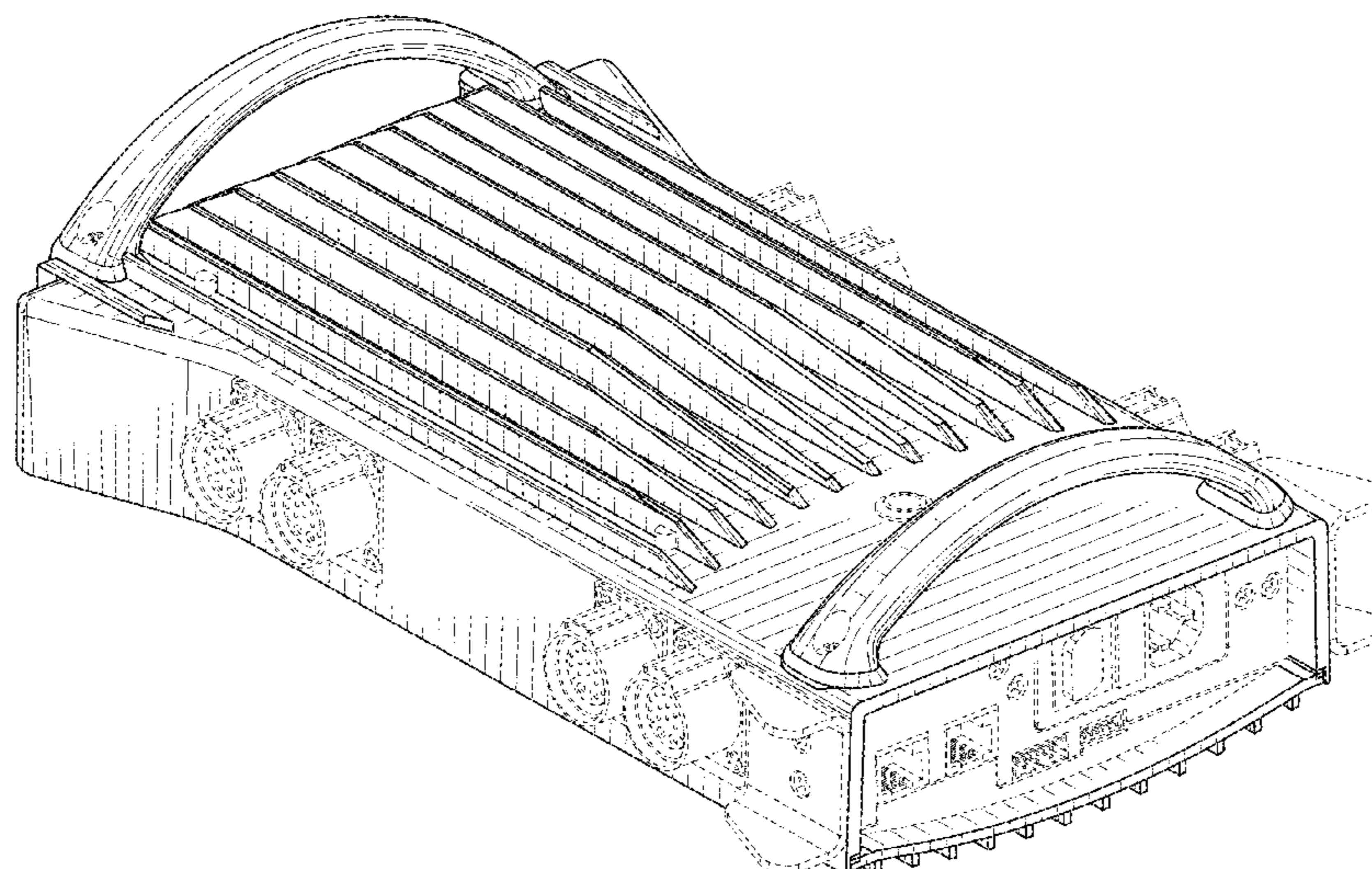
The shade lines in the Figures show contour and not surface ornamentation.

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1 Claim, 5 Drawing Sheets



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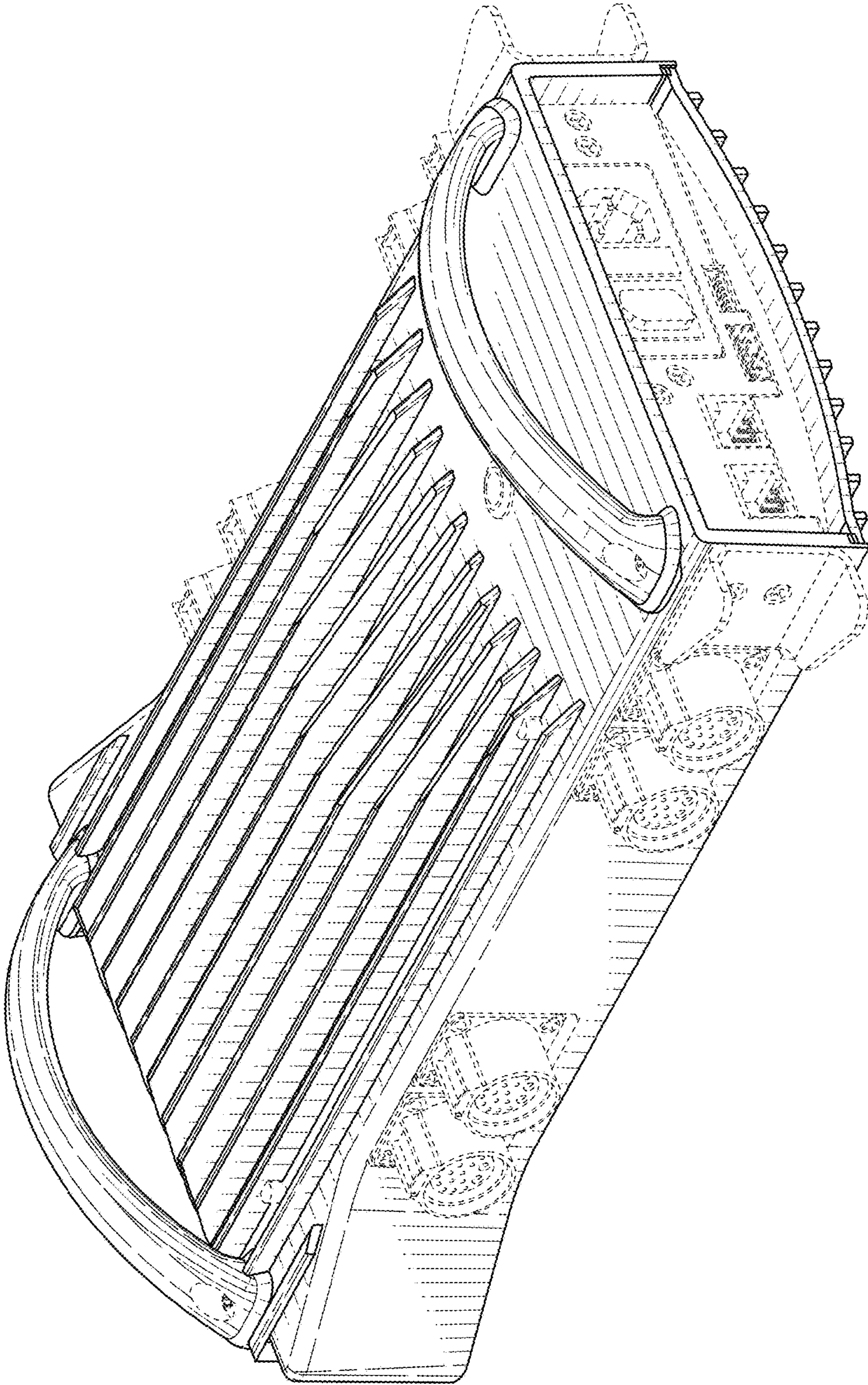


FIG. 1

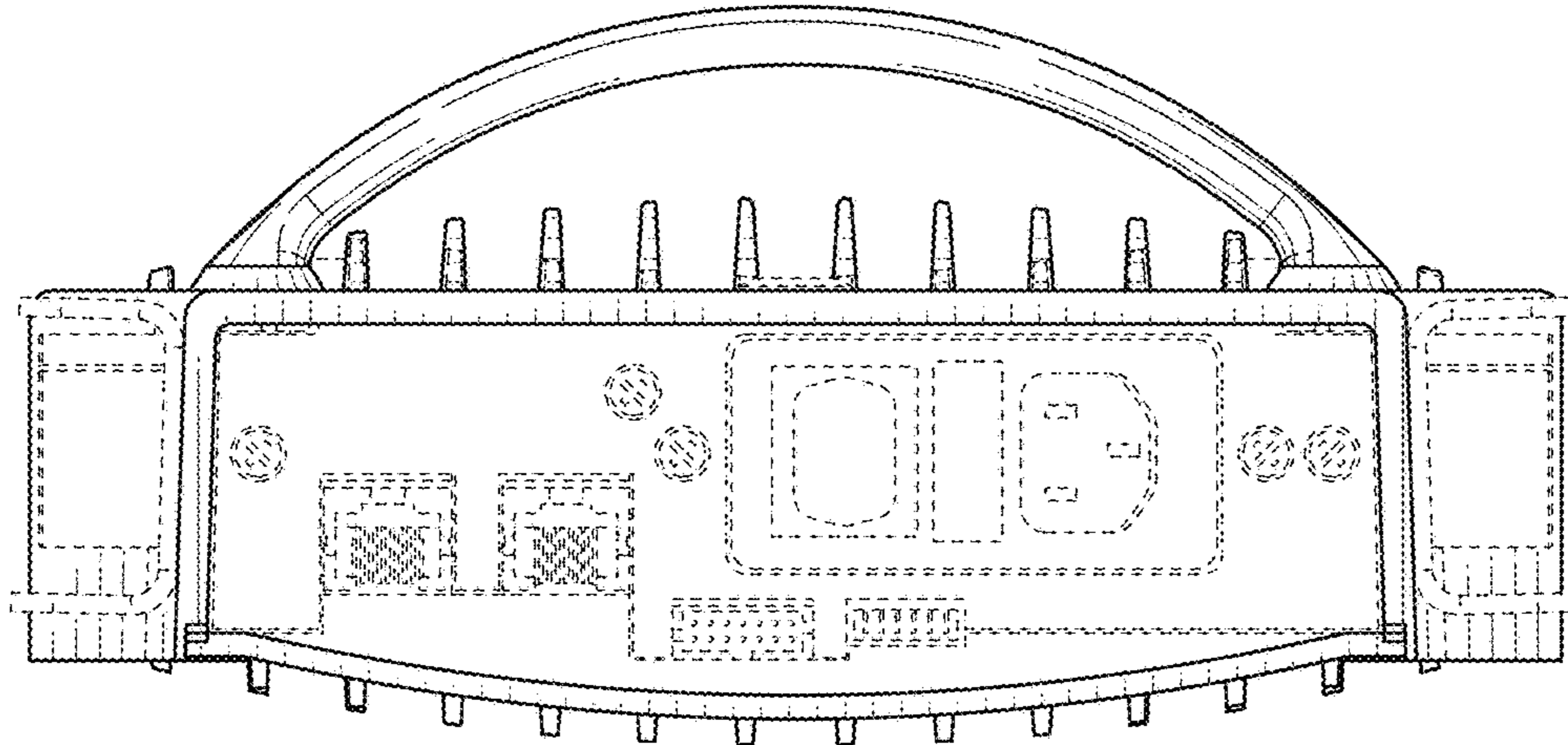


FIG. 2

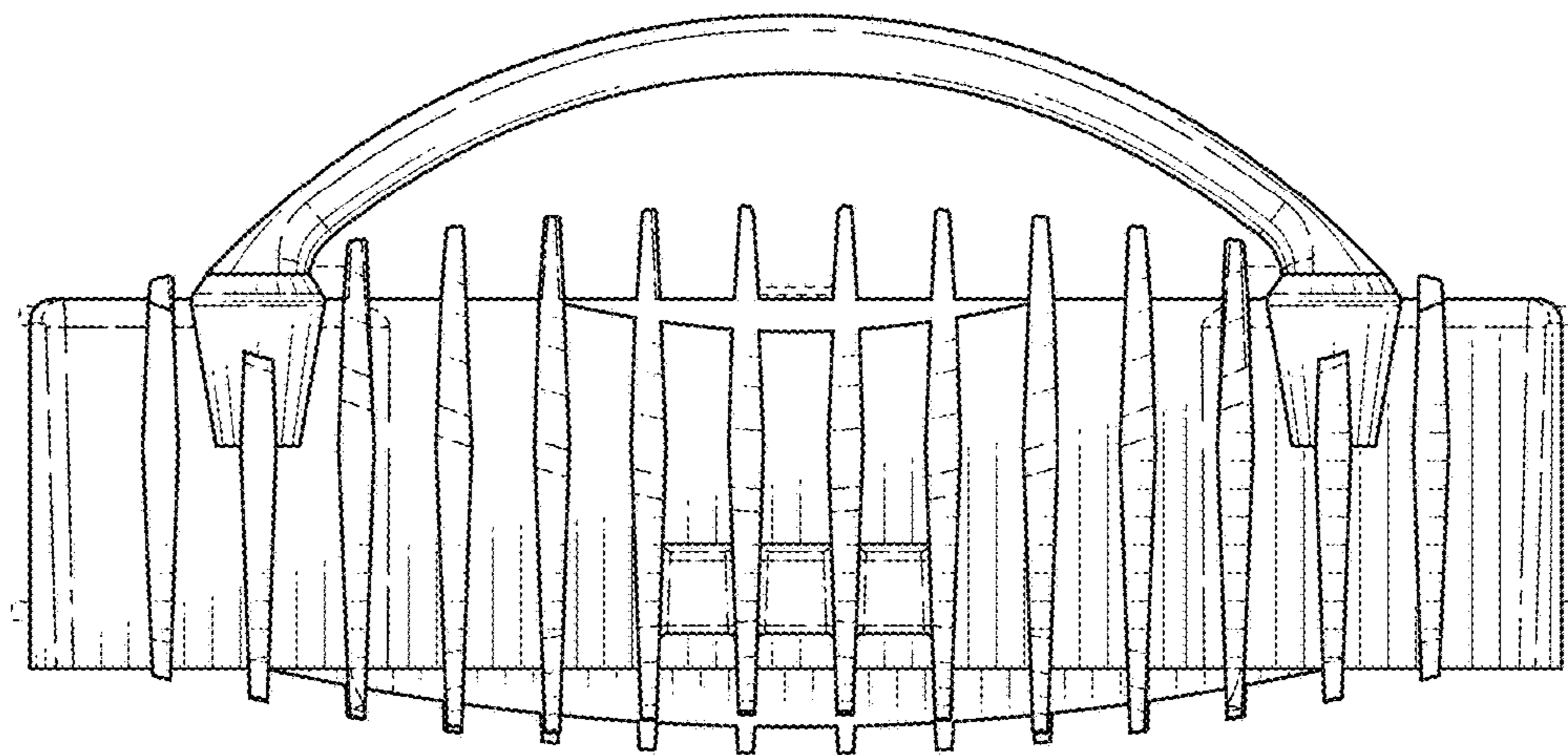


FIG. 3

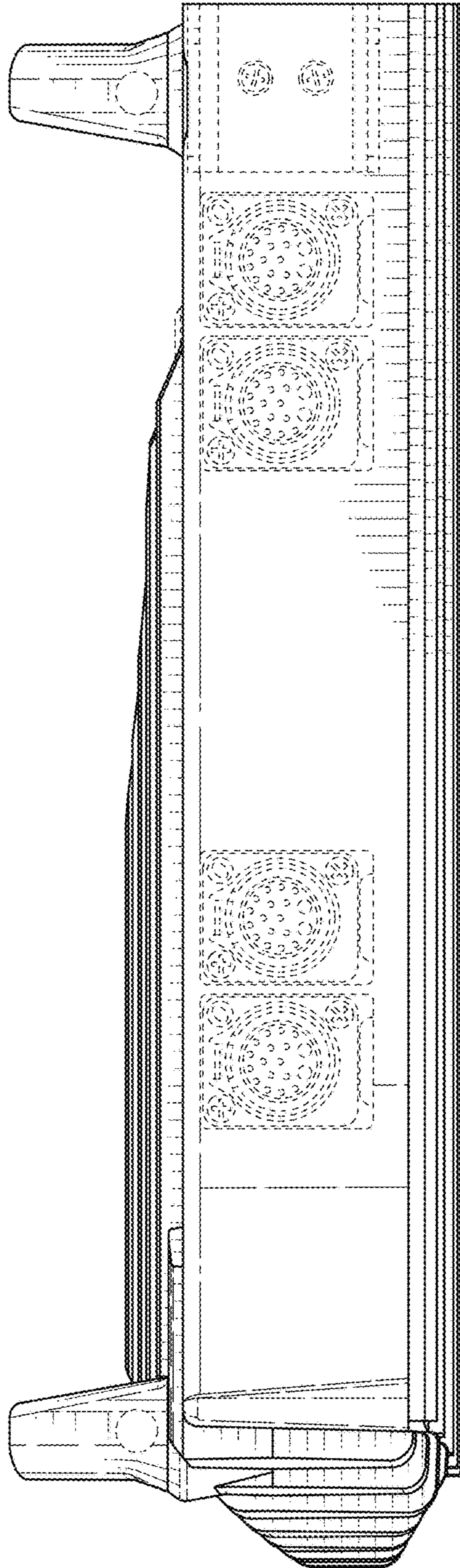


FIG. 4

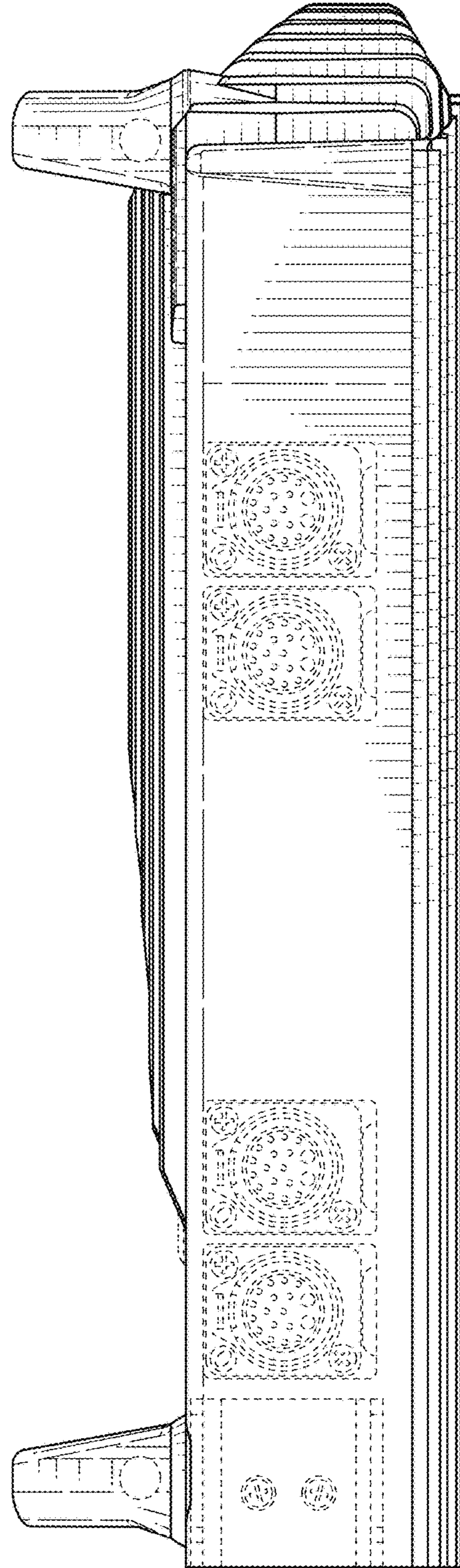


FIG. 5

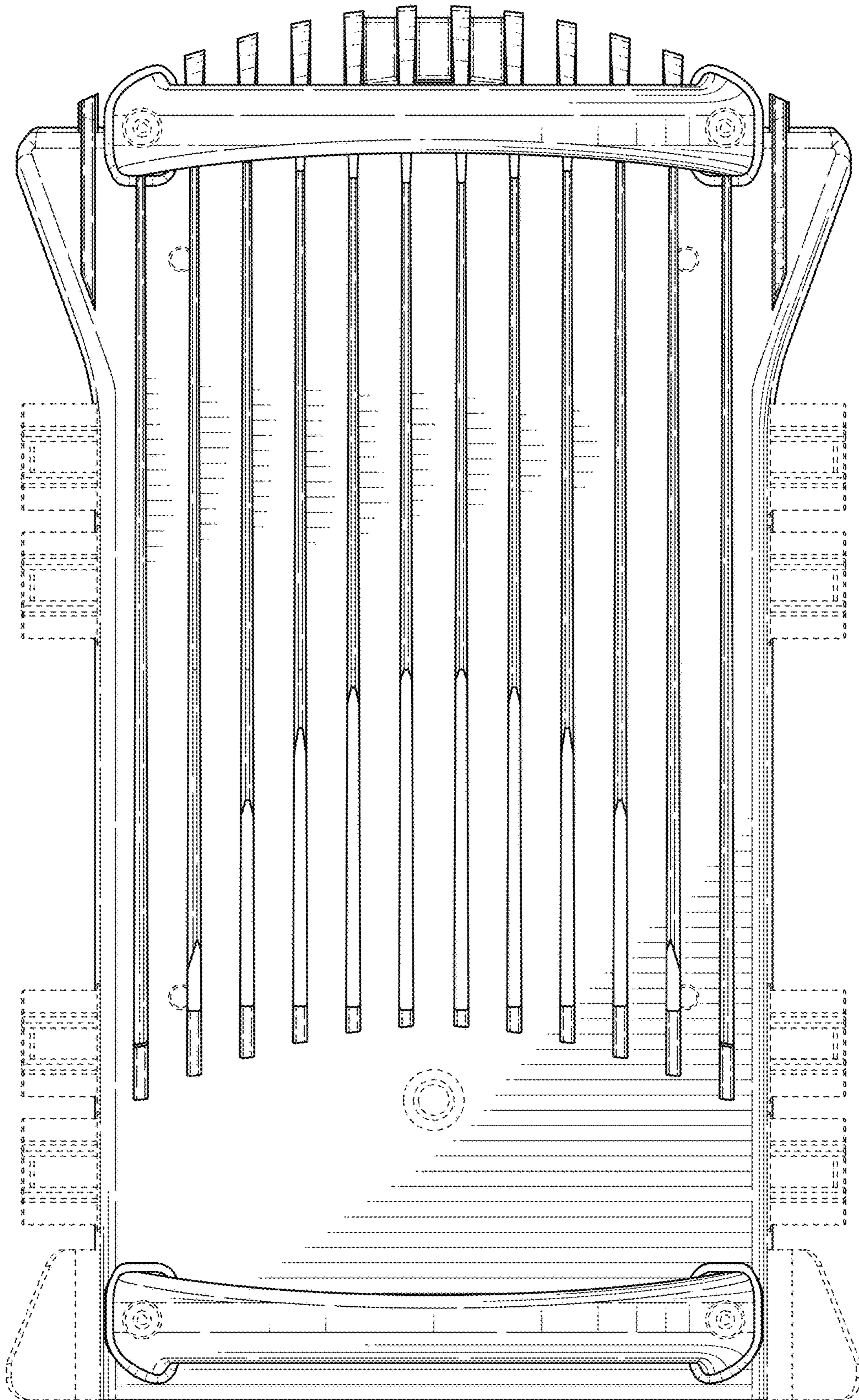


FIG. 6

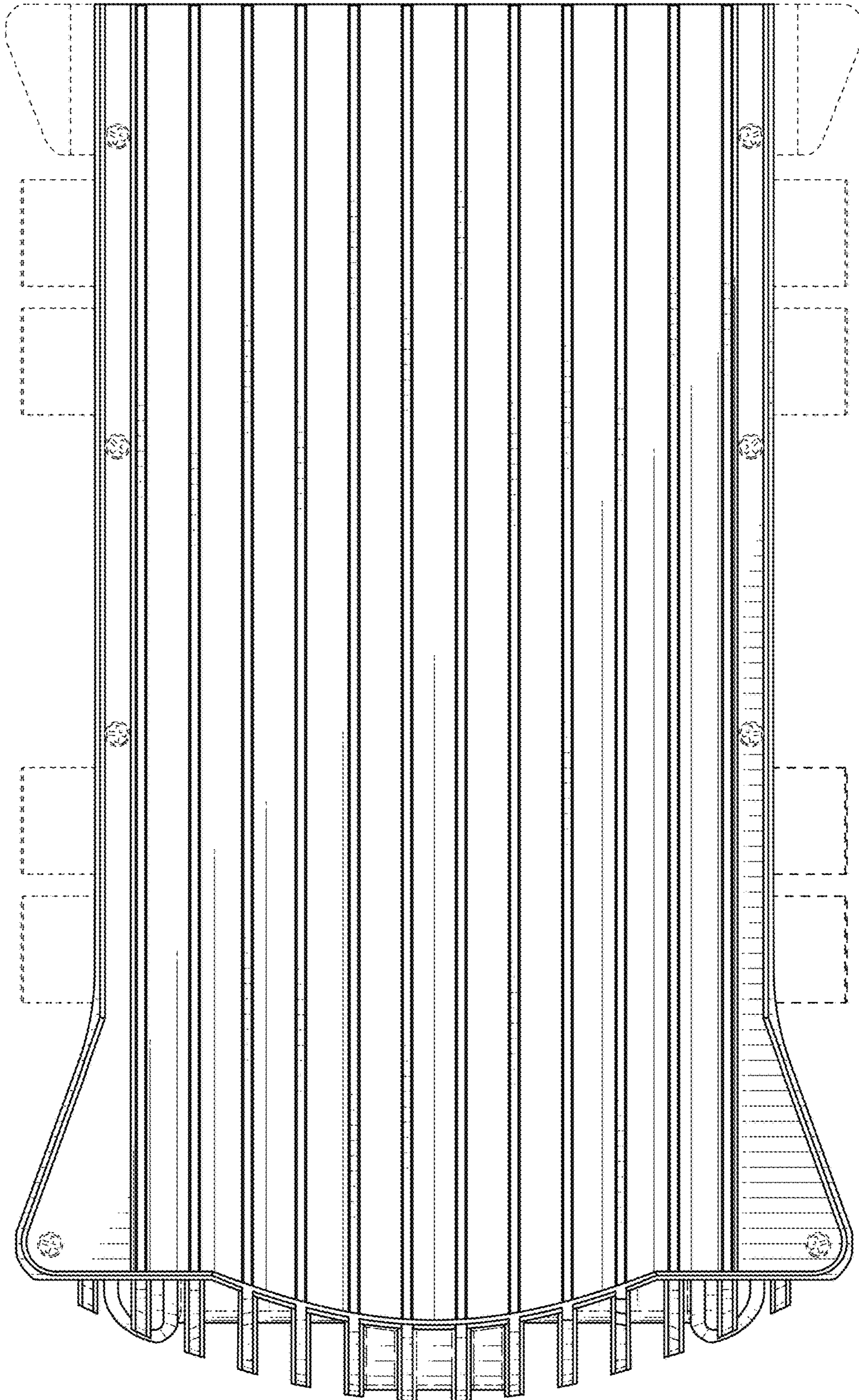


FIG. 7