



US00D804438S

(12) **United States Design Patent** (10) **Patent No.:** **US D804,438 S**
Makis et al. (45) **Date of Patent:** **** Dec. 5, 2017**

(54) **ELECTRONICS ENCLOSURE**
(71) Applicant: **EATON CORPORATION**, Cleveland, OH (US)
(72) Inventors: **David Loren Makis**, Shakopee, MN (US); **Rajkiran Bhagwat Rokade**, Pune (IN)

(73) Assignee: **EATON CORPORATION**, Cleveland, OH (US)

(**) Term: **15 Years**

(21) Appl. No.: **29/541,741**

(22) Filed: **Oct. 7, 2015**

(30) **Foreign Application Priority Data**

Apr. 10, 2015 (IN) 271302

(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/184**

(58) **Field of Classification Search**
USPC D13/110, 118, 123, 133, 146, 147, 149, D13/152, 153, 158-161, 173, 184, 199
CPC H02B 1/063; H02B 1/066
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

D618,619 S * 6/2010 Walter D13/147
D625,270 S * 10/2010 Schafmeister D13/147
D631,015 S * 1/2011 Iijima D13/147

D673,117 S * 12/2012 Gassauer D13/133
D737,765 S * 9/2015 Sekine D13/110
D739,822 S * 9/2015 Severing D13/146
D750,023 S * 2/2016 Sasano D13/146
D756,304 S * 5/2016 Wu D13/146
D758,317 S * 6/2016 Plassiard D13/154
2009/0269985 A1 * 10/2009 Stadler H01R 9/2458
439/629

* cited by examiner

Primary Examiner — Lakiya Rogers
Assistant Examiner — Harold E Blackwell, II
(74) *Attorney, Agent, or Firm* — Jarett D. Millar

(57) **CLAIM**

The ornamental design for an electronics enclosure, as shown and described.

DESCRIPTION

FIG. 1 is a perspective view of an electronics enclosure showing my new design.

FIG. 2 is a front elevation view of the electronics enclosure of FIG. 1.

FIG. 3 is a back elevation view of the electronics enclosure of FIG. 1.

FIG. 4 is a top plan view of the electronics enclosure of FIG. 1.

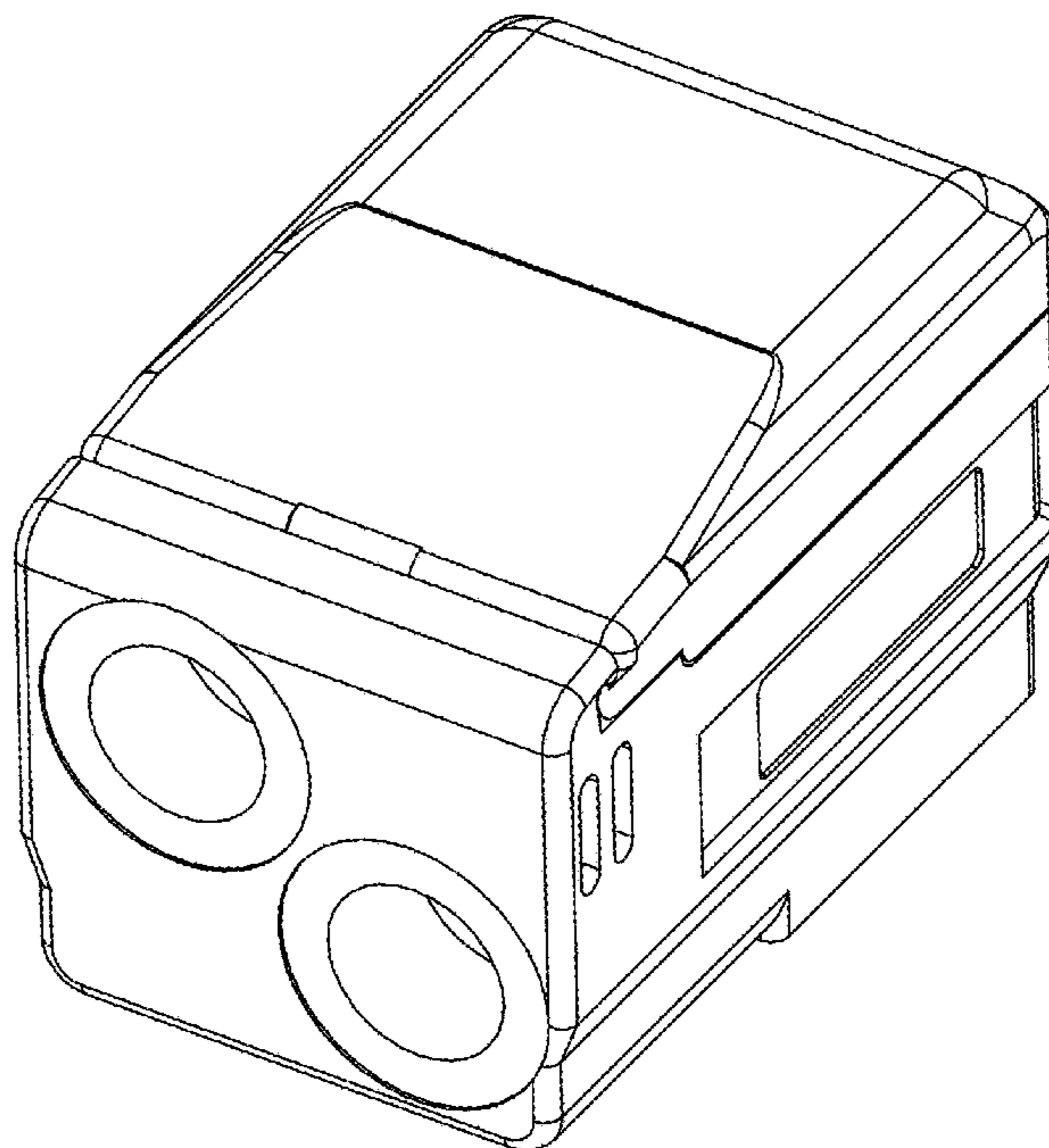
FIG. 5 is a bottom plan view of the electronics enclosure of FIG. 1.

FIG. 6 is a left elevation view of the electronics enclosure of FIG. 1; and,

FIG. 7 is a right elevation view of the electronics enclosure of FIG. 1.

The broken lines illustrate portions of the electronics enclosure which form no part of the claimed design.

1 Claim, 7 Drawing Sheets



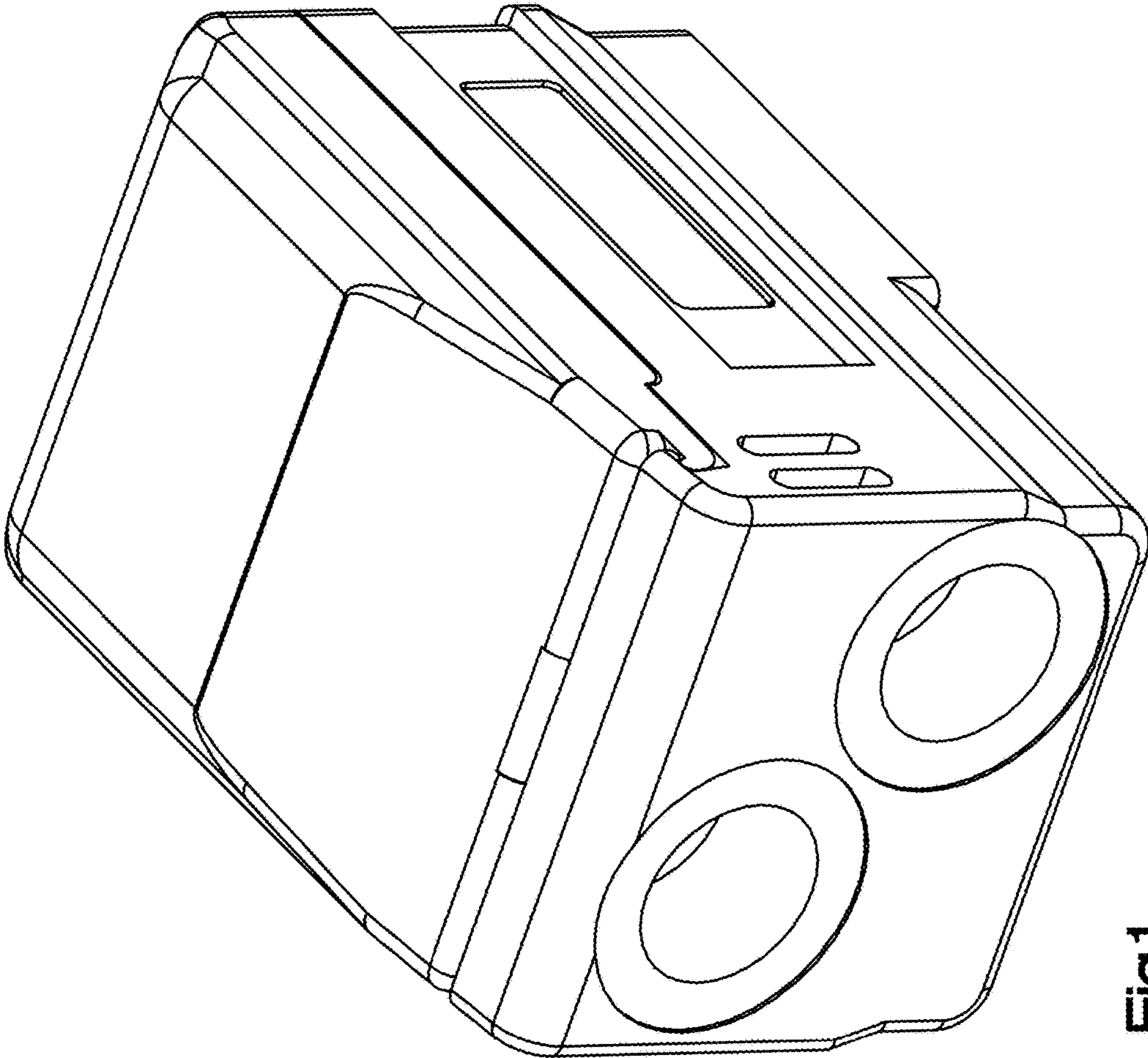


Fig.1

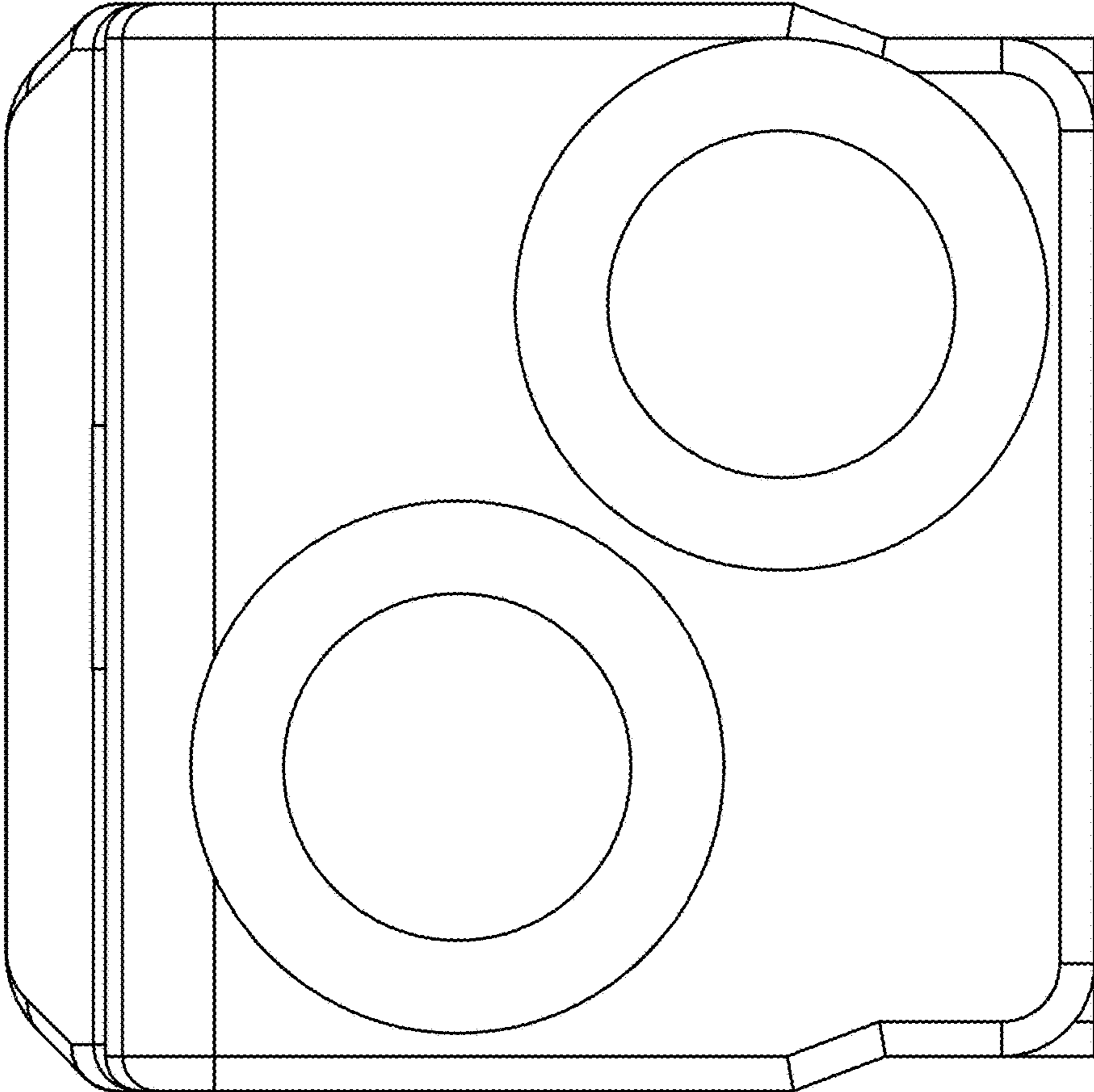


Fig.2

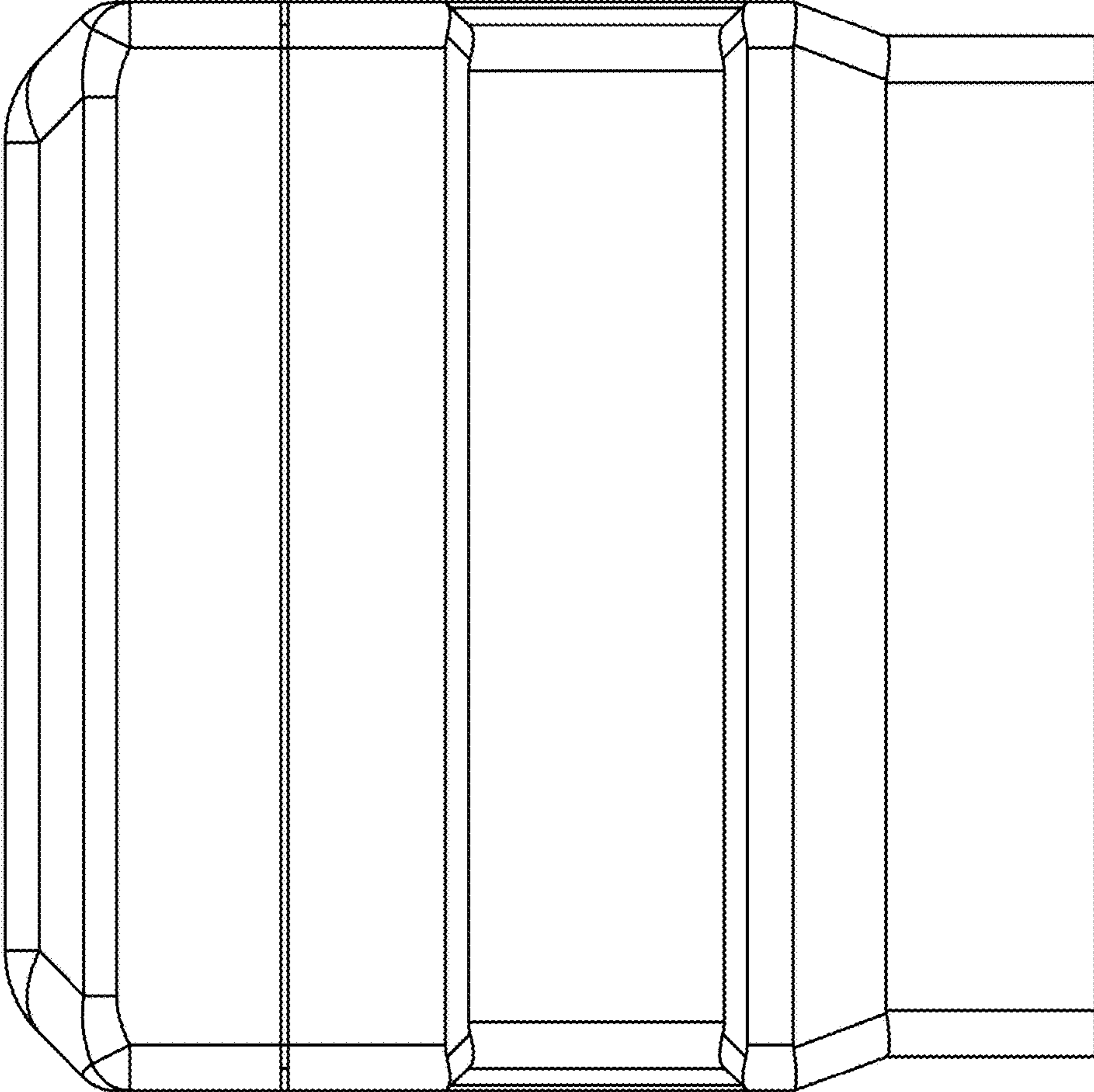


Fig.3

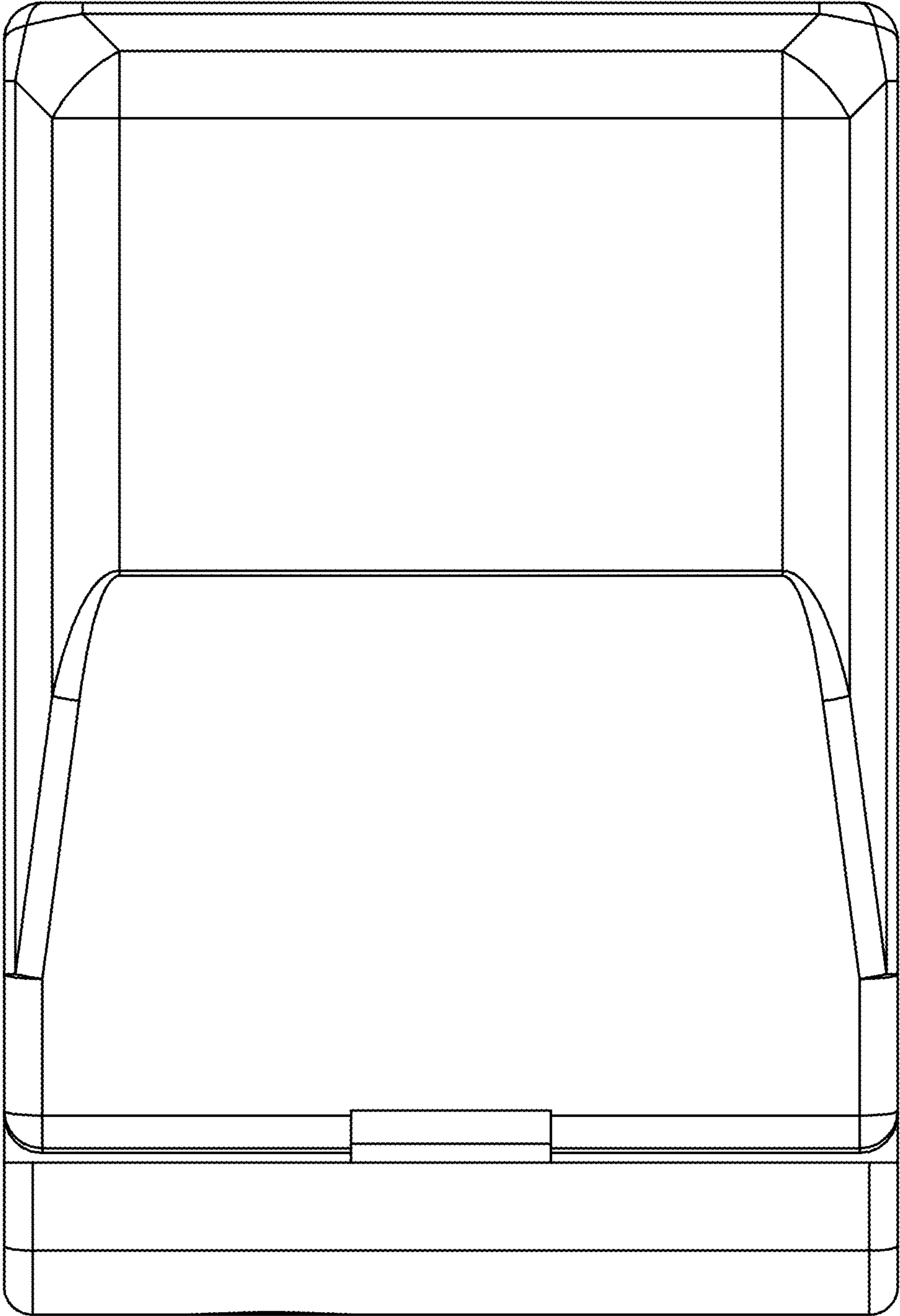


Fig.4

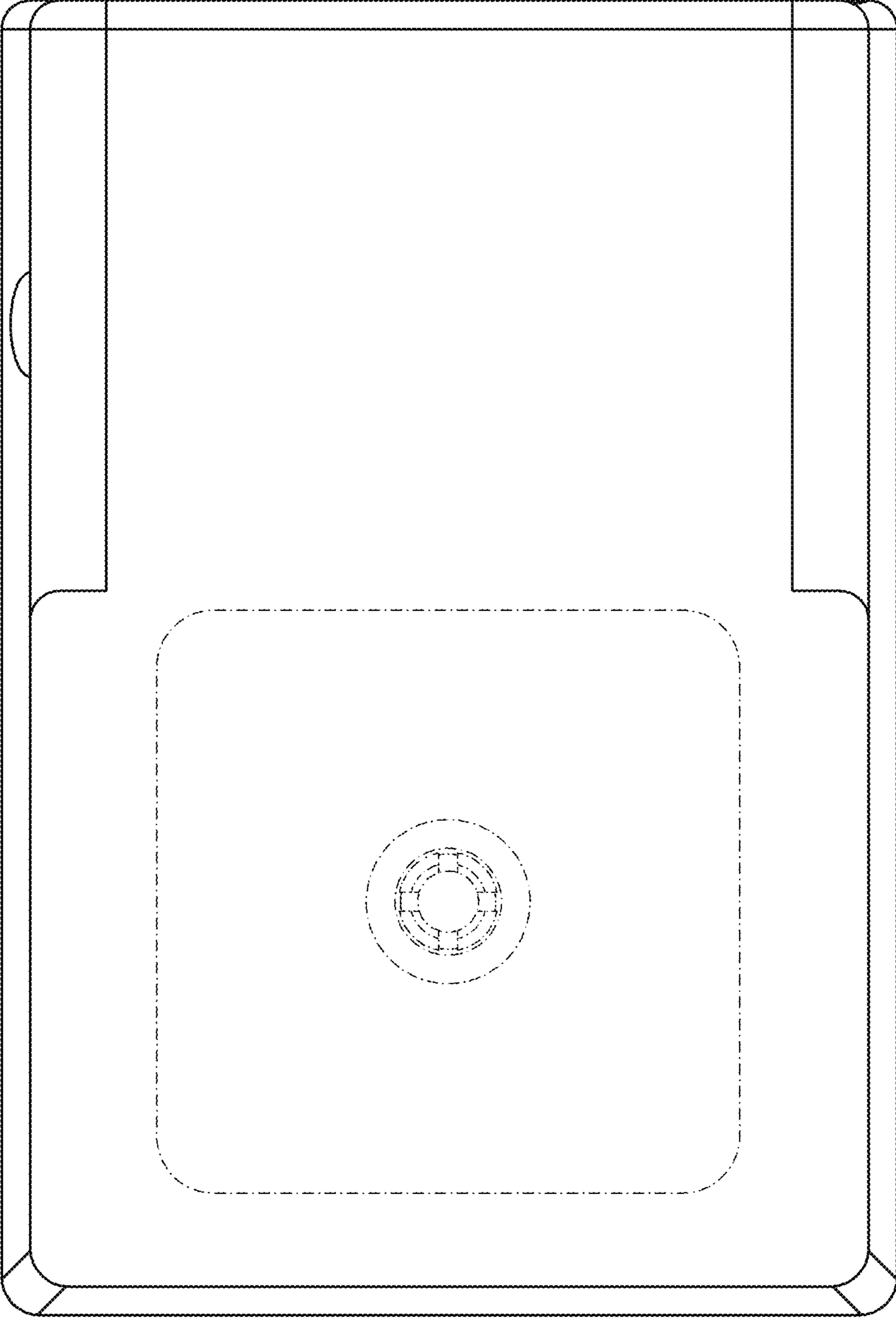


Fig.5

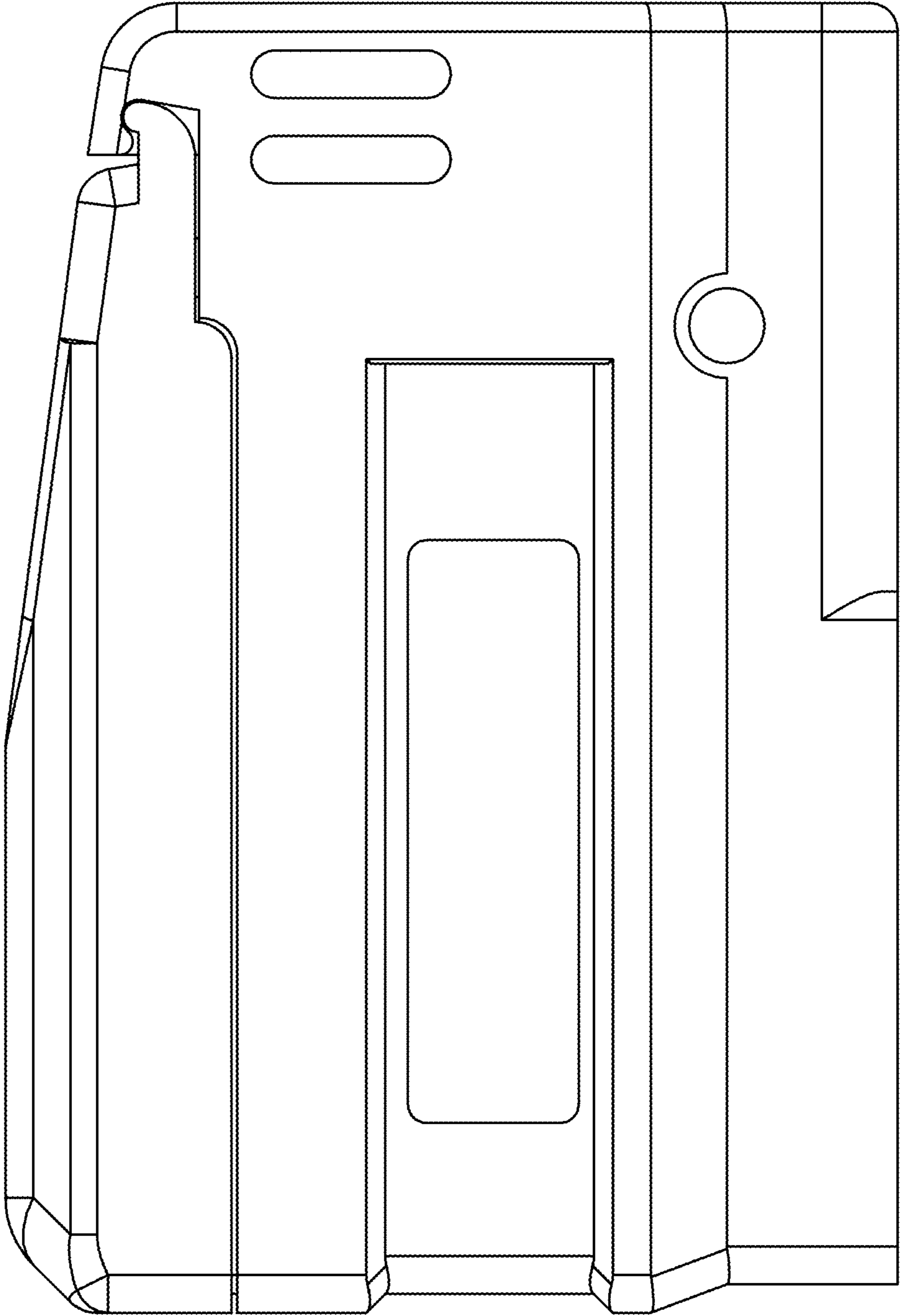


Fig.6

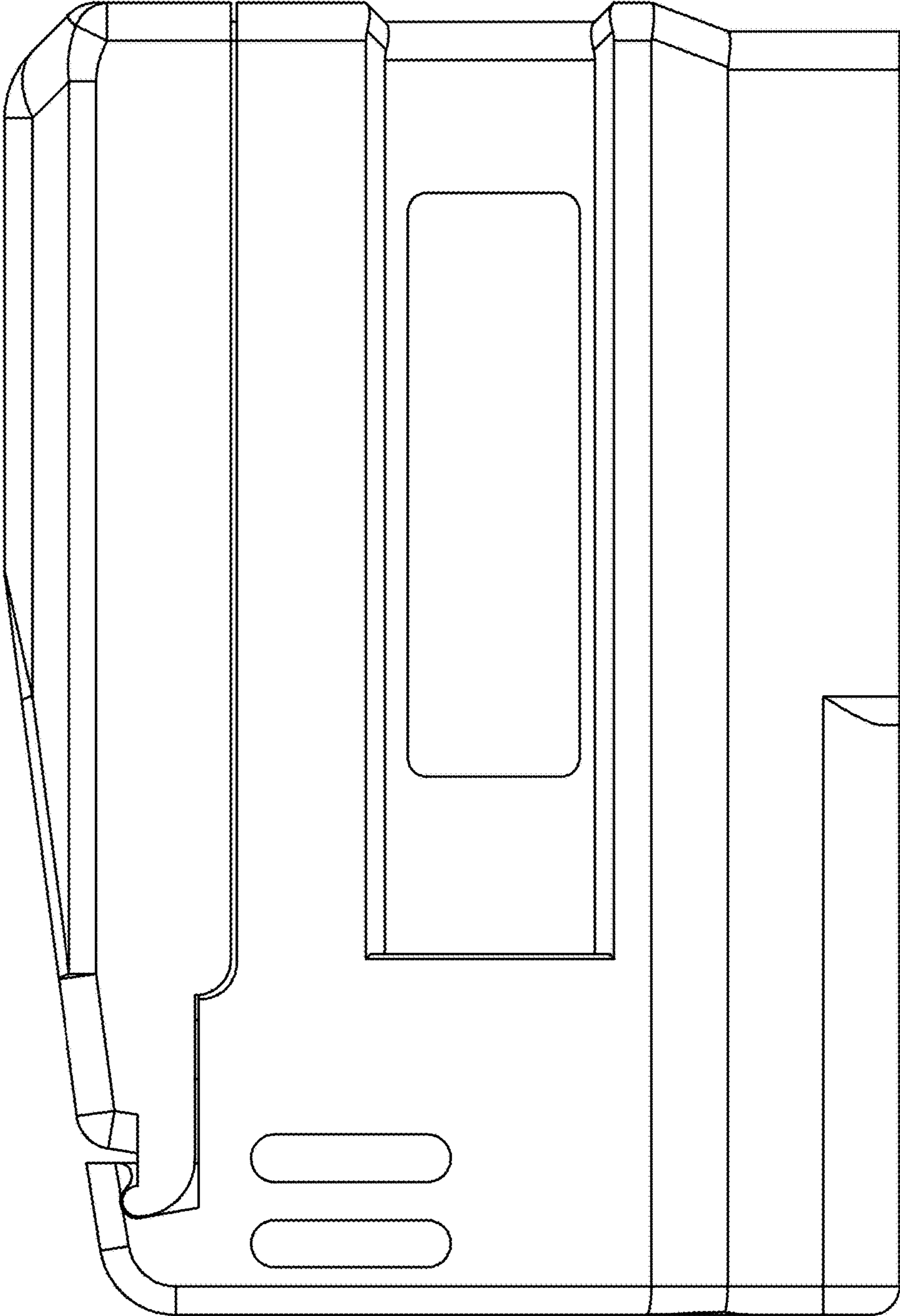


Fig.7