

US00D804437S

(12) **United States Design Patent** (10) **Patent No.:** **US D804,437 S**
Kantor et al. (45) **Date of Patent:** **** Dec. 5, 2017**

(54) **CIRCUIT BOARD**

(71) Applicant: **Norton (Waterford) Limited,**
Waterford (IE)

(72) Inventors: **Erica Jamie Kantor**, Cambridge (GB);
Steven David Gardner, Peterborough
(GB); **Ross William Weir**, Cambridge
(GB)

(73) Assignee: **Norton (Waterford) Limited,**
Waterford (IE)

(**) Term: **15 Years**

(21) Appl. No.: **29/579,617**

(22) Filed: **Sep. 30, 2016**

(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**

USPC D13/182; 361/748, 752, 760, 761, 807,
361/808, 809; 174/250, 253, 255;
363/144, 147

CPC H05K 3/30; H05K 3/301; H05K 3/284;
H05K 1/18; H05K 1/181; H05K 1/182;
H05K 1/183; H05K 1/185; H05K 1/00;
H05K 7/1417; H05K 7/02; H05K 7/12;
H05K 7/06; H01L 2924/14

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,979,090 A * 12/1990 Huss H05K 1/0265
174/255
5,119,286 A * 6/1992 Huss H01L 25/112
257/E25.025
D359,476 S * 6/1995 Sakashita D13/182
D459,706 S * 7/2002 Ebihara D13/182

D466,093 S * 11/2002 Ebihara D13/182
D471,167 S * 3/2003 Ebihara D13/182
D471,524 S * 3/2003 Ebihara D13/182
D505,925 S * 6/2005 Koo D13/182
D570,307 S * 6/2008 Kobayashi D13/180
D576,577 S * 9/2008 Kobayashi D13/182
D597,504 S * 8/2009 Kobayashi D13/182
D637,566 S * 5/2011 Cleghorn D13/182
D639,756 S * 6/2011 Greene, Jr. D13/182
D642,546 S * 8/2011 Greene, Jr. D13/182
D647,072 S * 10/2011 Bentley D13/182
D745,476 S * 12/2015 Ronse D13/182
D753,073 S * 4/2016 Sponring D13/182
2002/0131253 A1 * 9/2002 Kobayashi H05K 1/0271
361/760
2007/0294889 A1 * 12/2007 Schmitt H01L 25/50
29/831
2008/0080151 A1 * 4/2008 Shimizu H05K 1/0263
361/760

(Continued)

Primary Examiner — Elizabeth J Oswecki

(74) *Attorney, Agent, or Firm* — Baker Hostetler LLP;
Gregory A. Grissett

(57) **CLAIM**

The ornamental design for a circuit board, as shown and described.

DESCRIPTION

FIG. 1 is a top, front, right side perspective view of a circuit board showing our new design;

FIG. 2 is a front elevation view thereof;

FIG. 3 is a rear elevation view thereof;

FIG. 4 is a left side elevation view thereof;

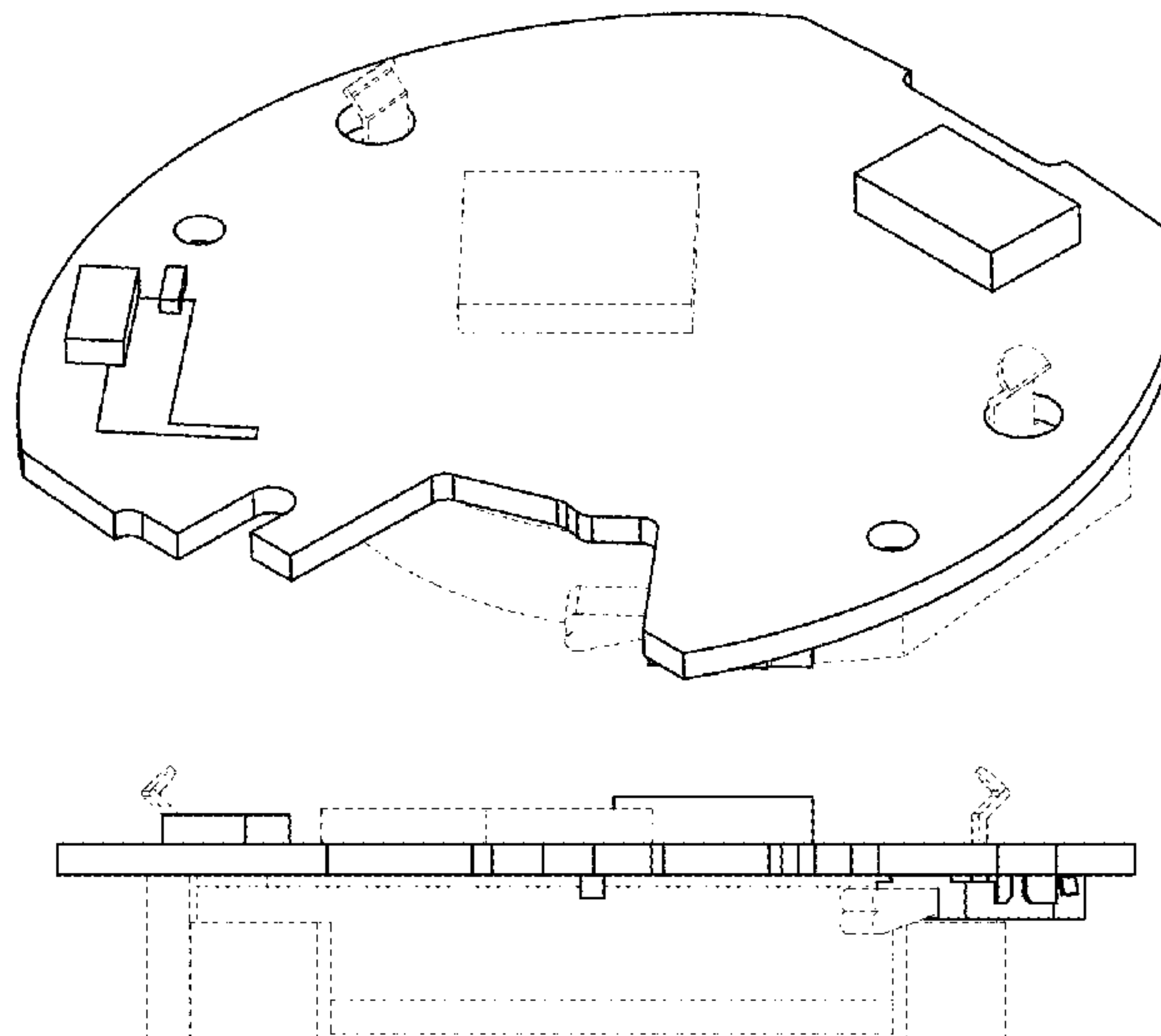
FIG. 5 is a right side elevation view thereof.

FIG. 6 is a top plan view thereof; and,

FIG. 7 is a bottom plan view thereof.

The dashed line portion of the drawings is included to show unclaimed subject matter only for the purpose of illustrating environment and forms no part of the claimed design.

1 Claim, 3 Drawing Sheets



(56)

References Cited

U.S. PATENT DOCUMENTS

2008/0144290 A1 * 6/2008 Brandt B60R 16/0239
361/720
2009/0268390 A1 * 10/2009 King G06F 13/409
361/679.33

* cited by examiner

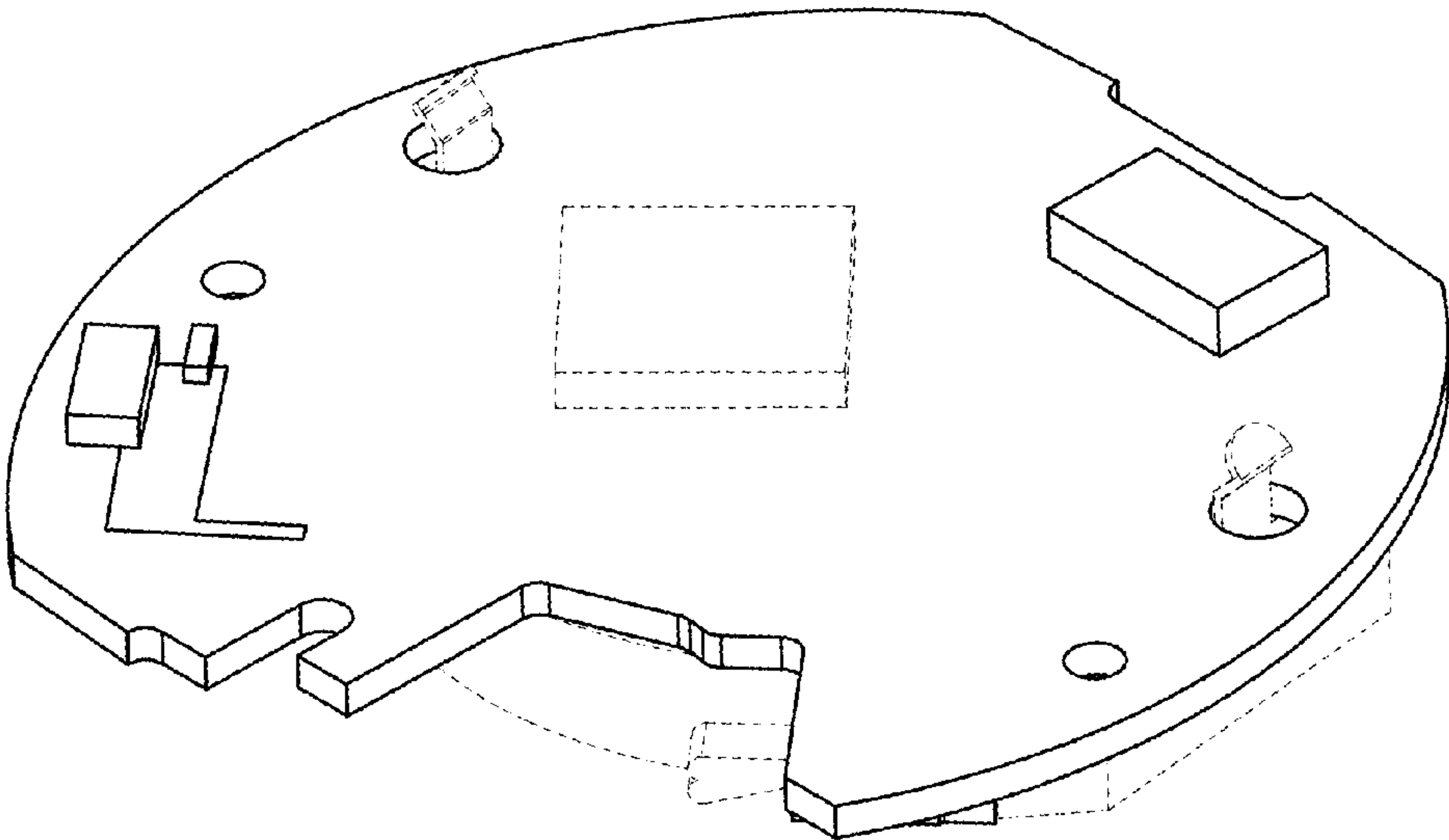


Fig.1

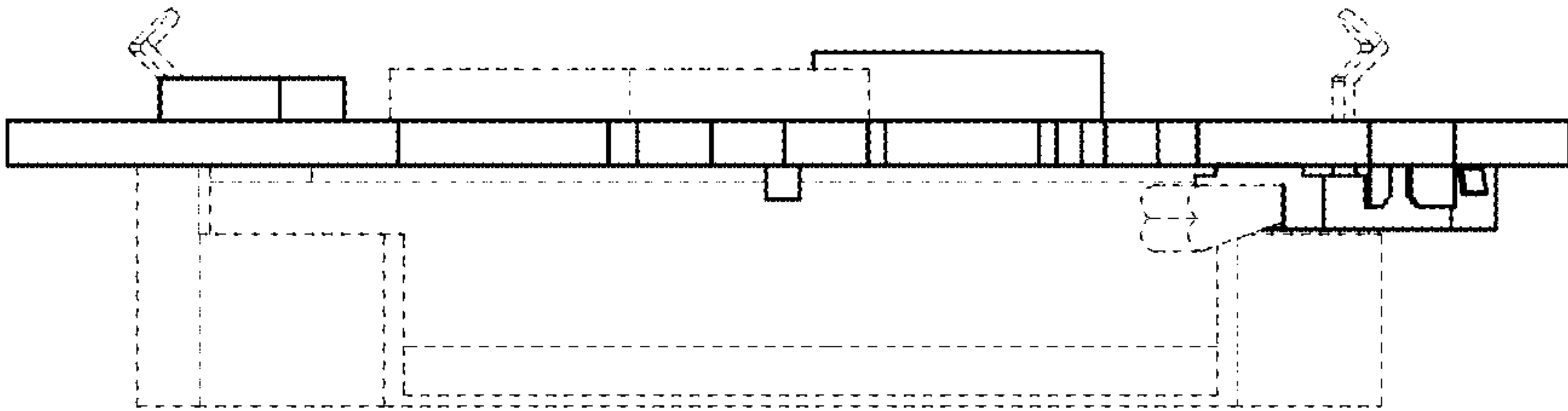


Fig.2

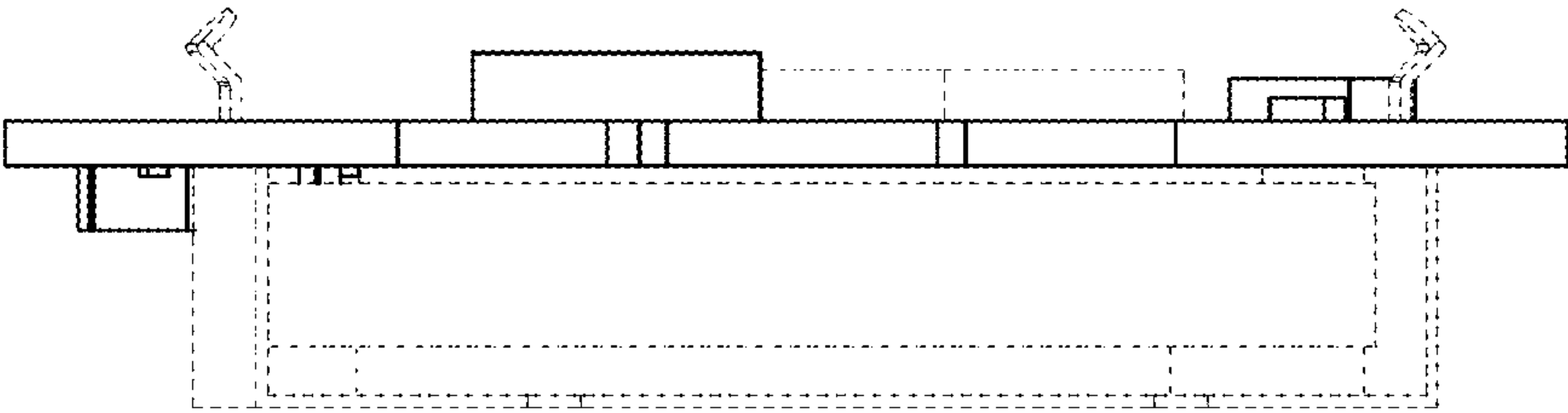


Fig.3

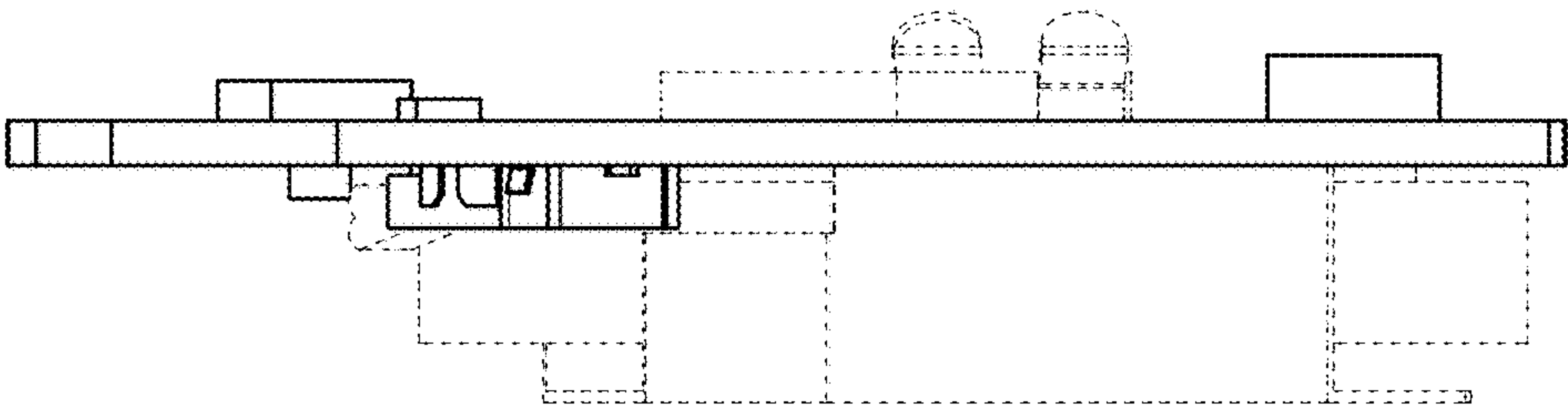


Fig.4

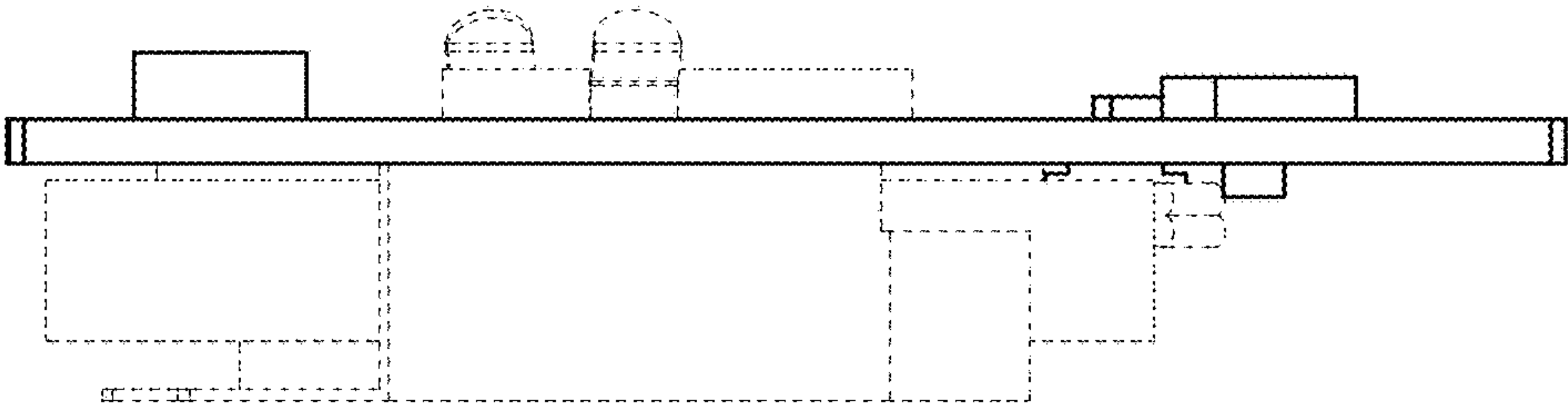


Fig.5

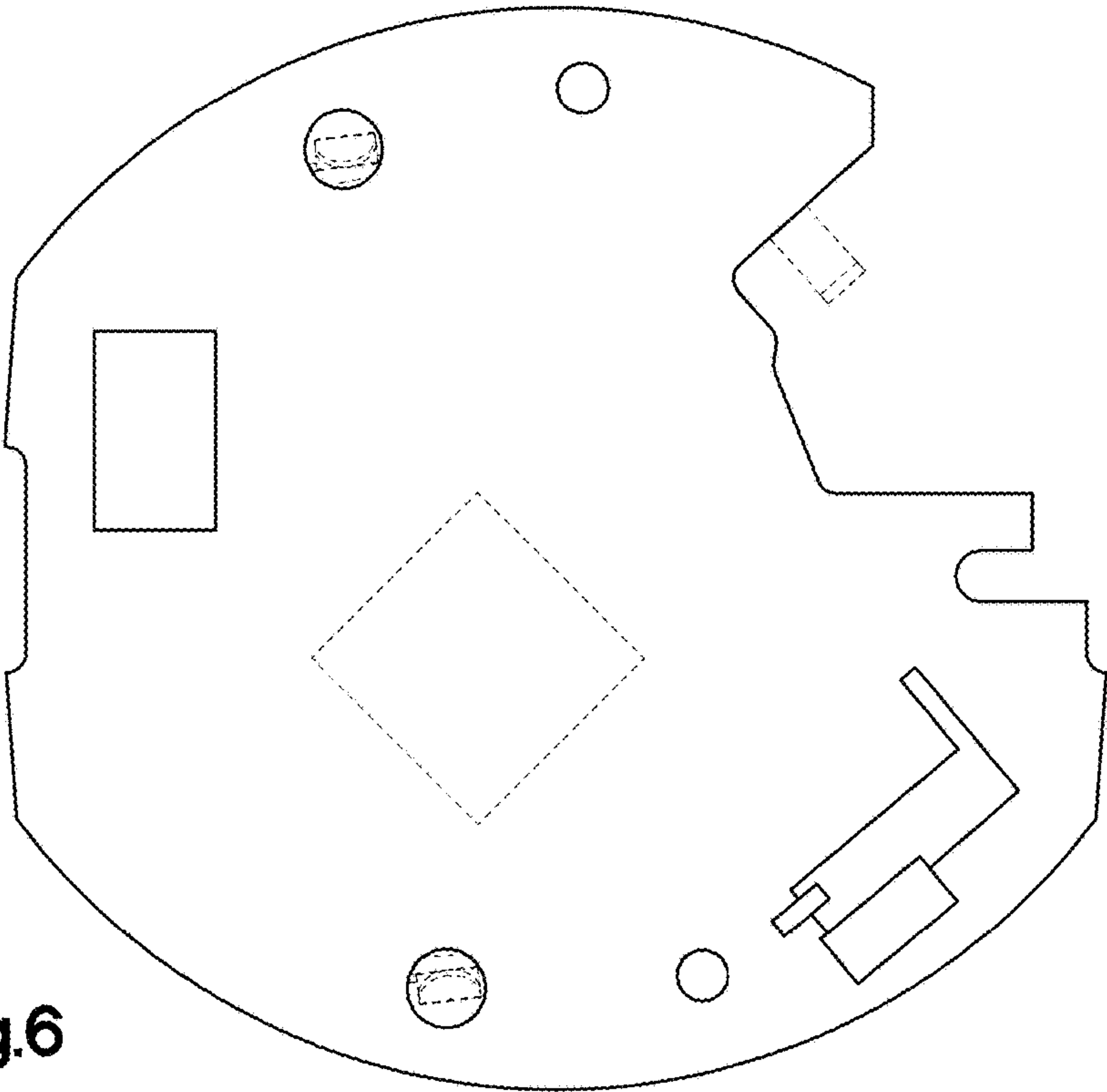


Fig.6

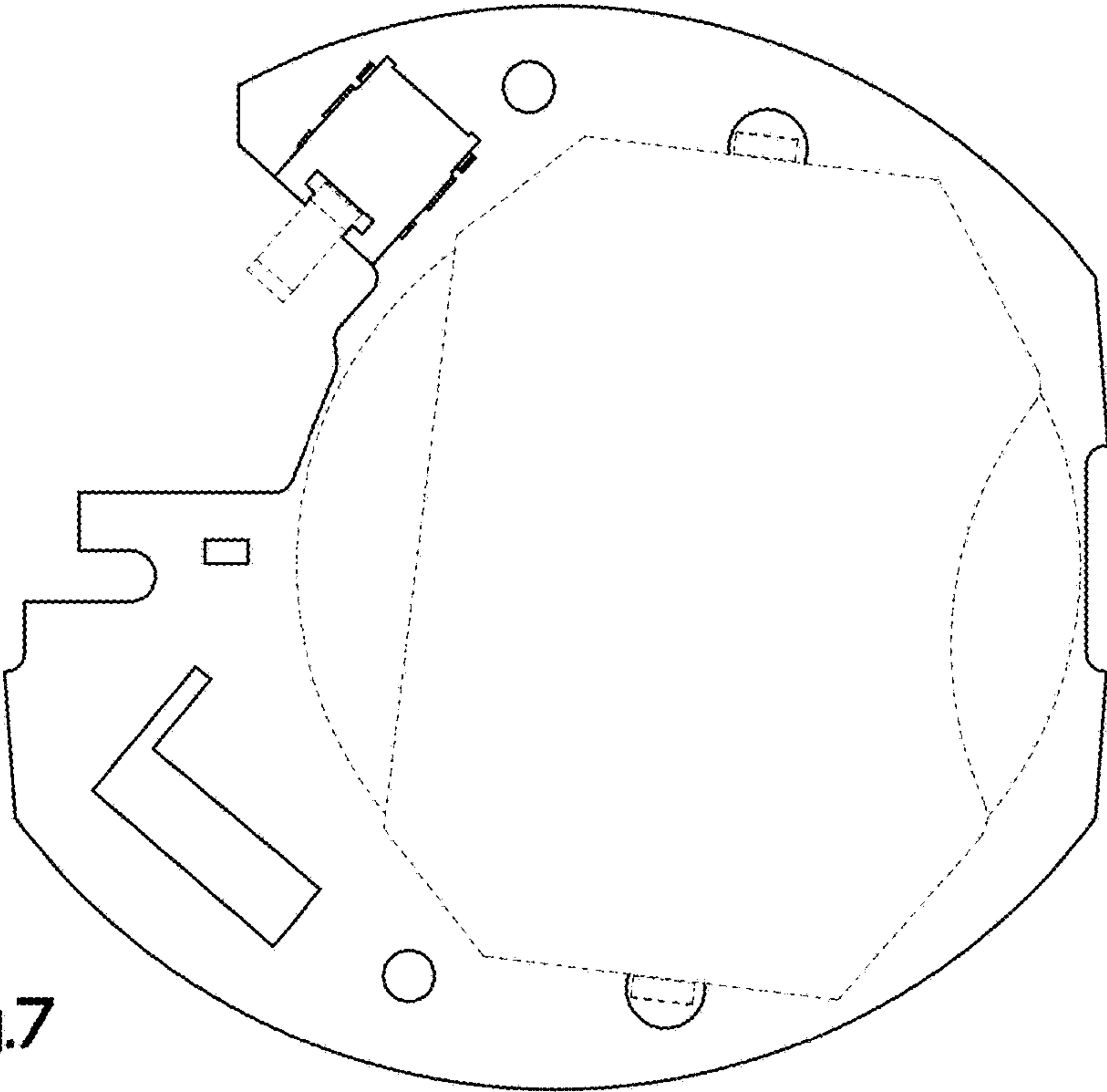


Fig.7