



US00D803708S

(12) **United States Design Patent**
Madrid

(10) **Patent No.:** **US D803,708 S**

(45) **Date of Patent:** **** Nov. 28, 2017**

(54) **ELECTRONICS ENCLOSURE**

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(**) Term: **15 Years**

(21) Appl. No.: **29/577,126**

(22) Filed: **Sep. 9, 2016**

(51) **LOC (10) Cl.** **10-04**

(52) **U.S. Cl.**
USPC **D10/70; D14/356**

(58) **Field of Classification Search**
USPC D14/356-358, 426-428, 432, 440, 447,
D14/496, 250, 251-253; D10/46, 47, 65,
D10/70, 75, 80, 104.1, 106.2, 106.3,
D10/106.4, 106.6, 106.9, 114.9, 121;
D13/184, 199; D22/108, 117, 199;
D3/201, 215, 217, 218, 221-223, 228,
D3/273

CPC F41A 17/06; F41A 17/063; F41C 33/029;
F41C 33/0209

See application file for complete search history.

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(57) **CLAIM**

The ornamental design for a electronics enclosure, as shown and described.

DESCRIPTION

FIG. 1 is a perspective view of the electronics enclosure of the present invention;

FIG. 2 is a front view of the electronics enclosure of the present invention;

FIG. 3 is a back view of the electronics enclosure of the present invention;

FIG. 4 is a right side view of the electronics enclosure of the present invention;

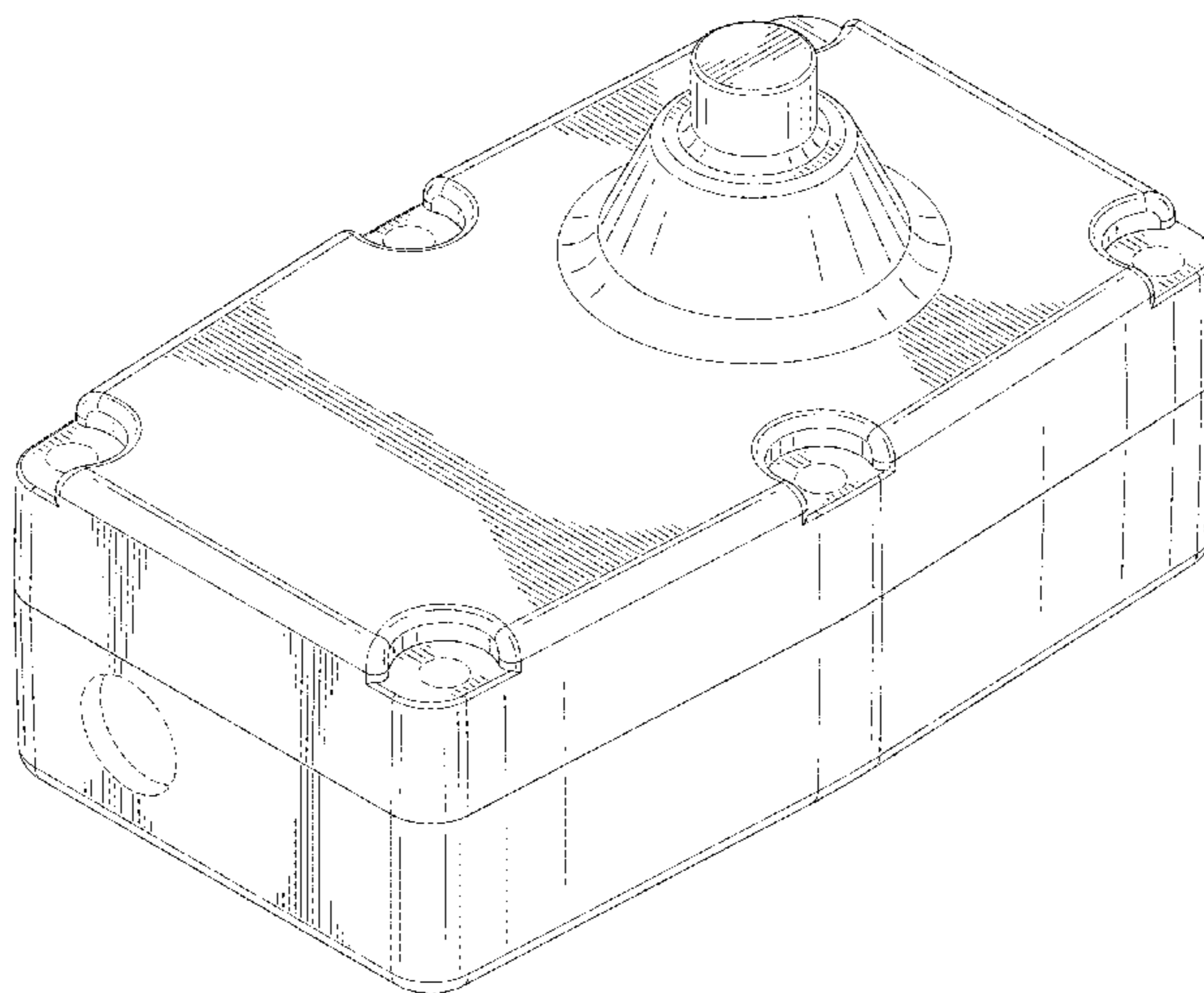
FIG. 5 is a left side view of the electronics enclosure of the present invention;

FIG. 6 is a top view of the electronics enclosure of the present invention; and,

FIG. 7 is a bottom view of the electronics enclosure of the present invention.

The broken lines depicting a data port in FIGS. 1 and 2, and attachment holes in FIGS. 1 and 6, represent structural portions of the electronics enclosure that form no part of the claimed design.

1 Claim, 5 Drawing Sheets



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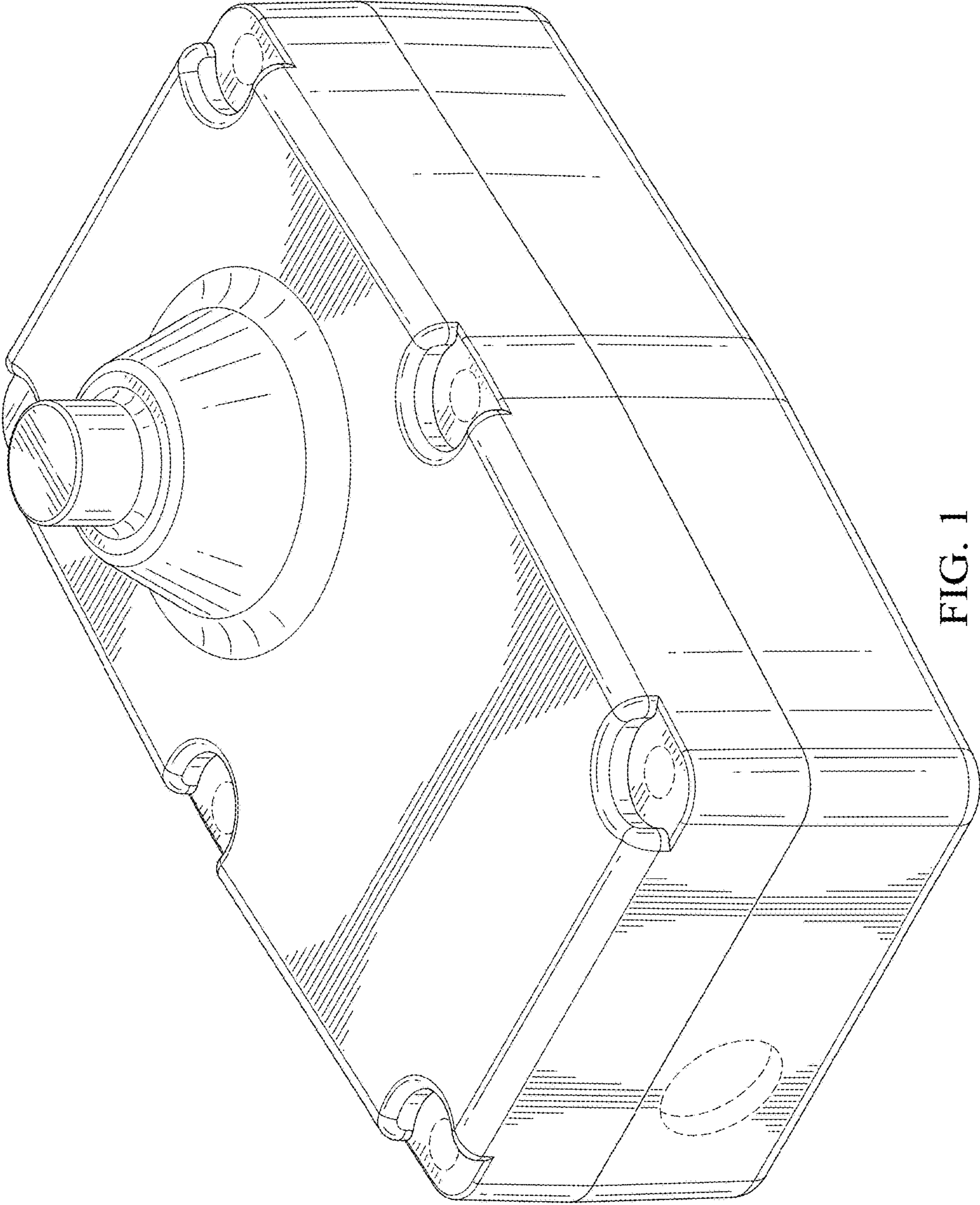


FIG. 1

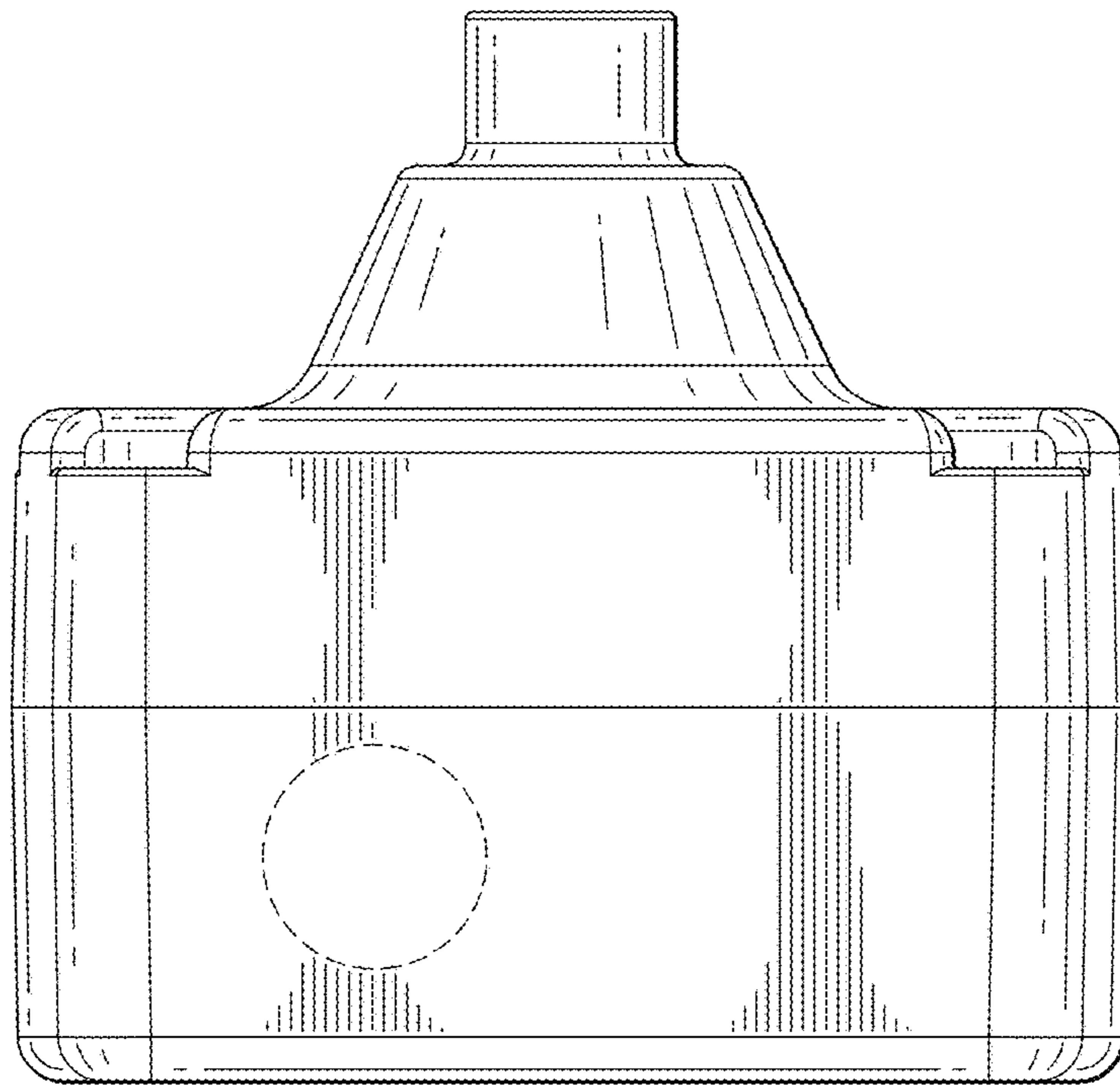


FIG. 2

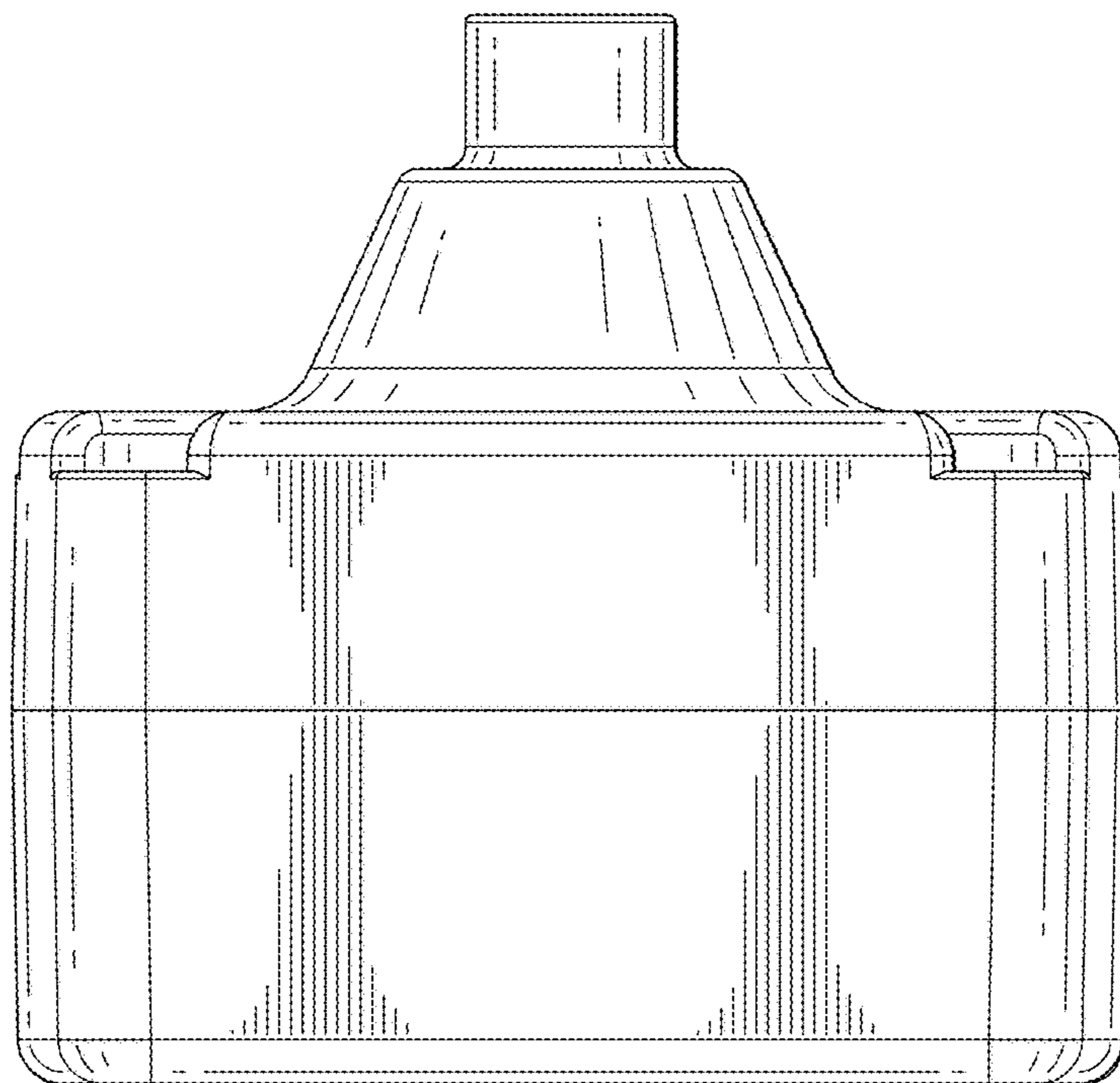


FIG. 3

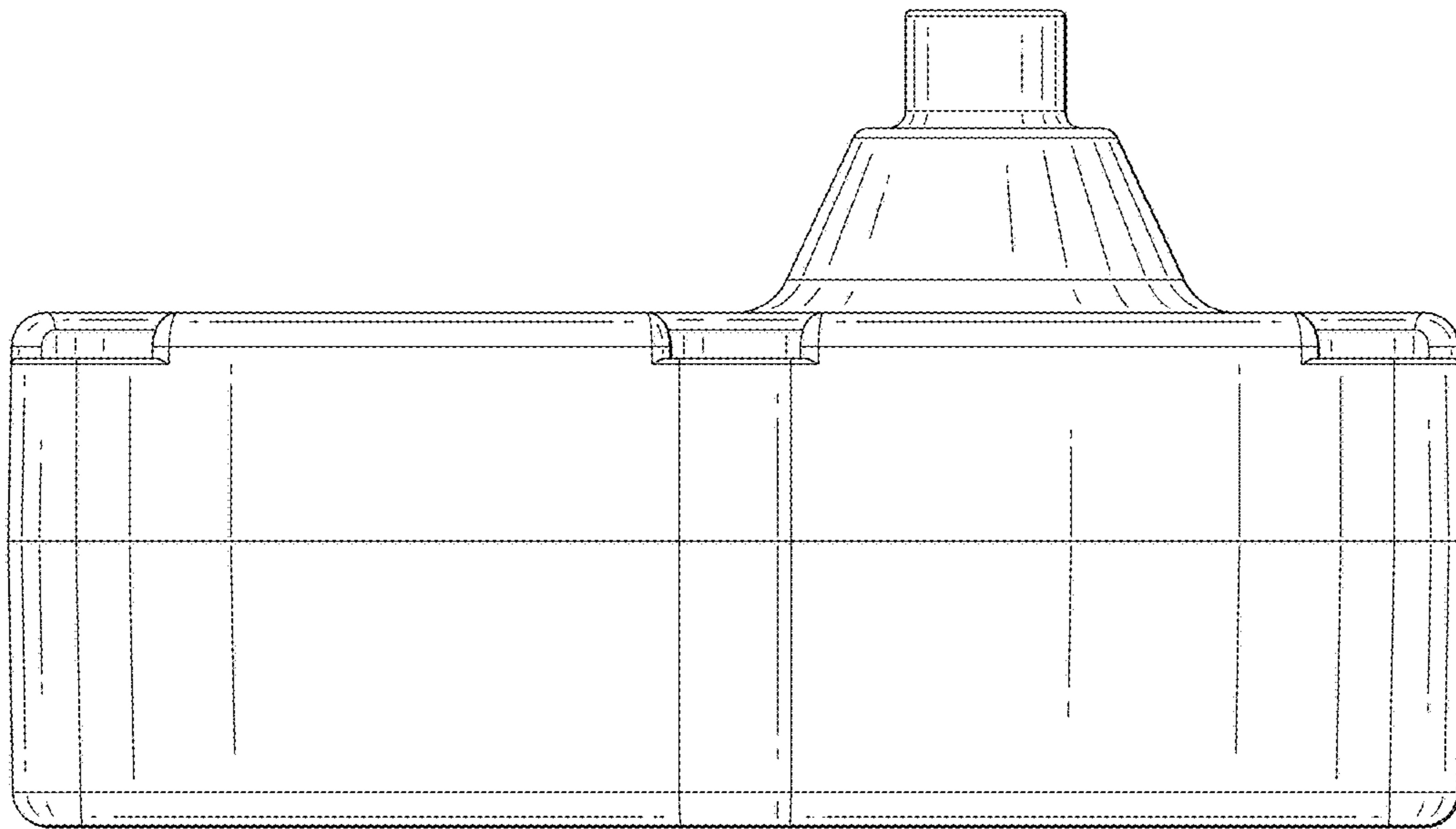


FIG. 4

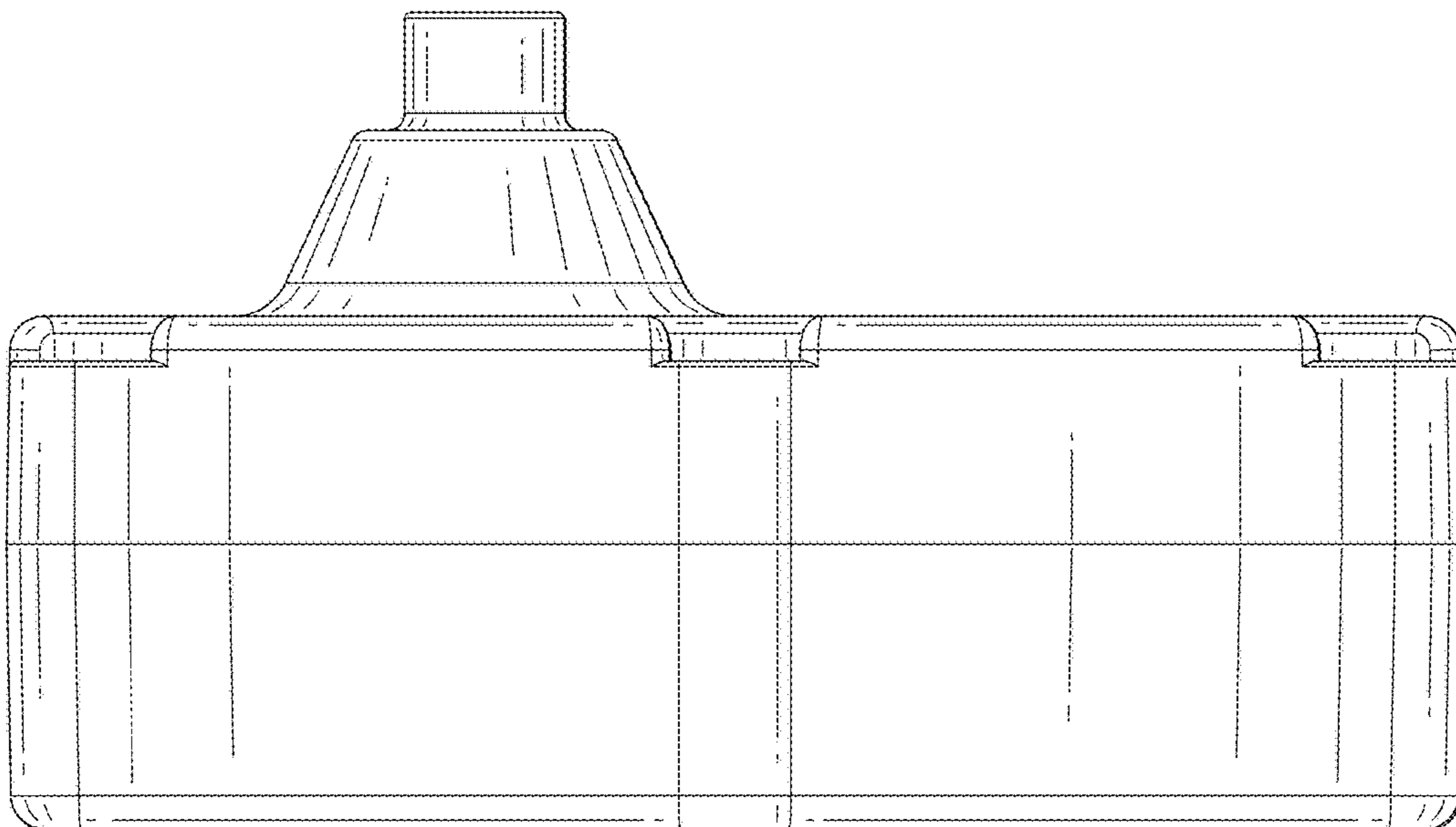


FIG. 5

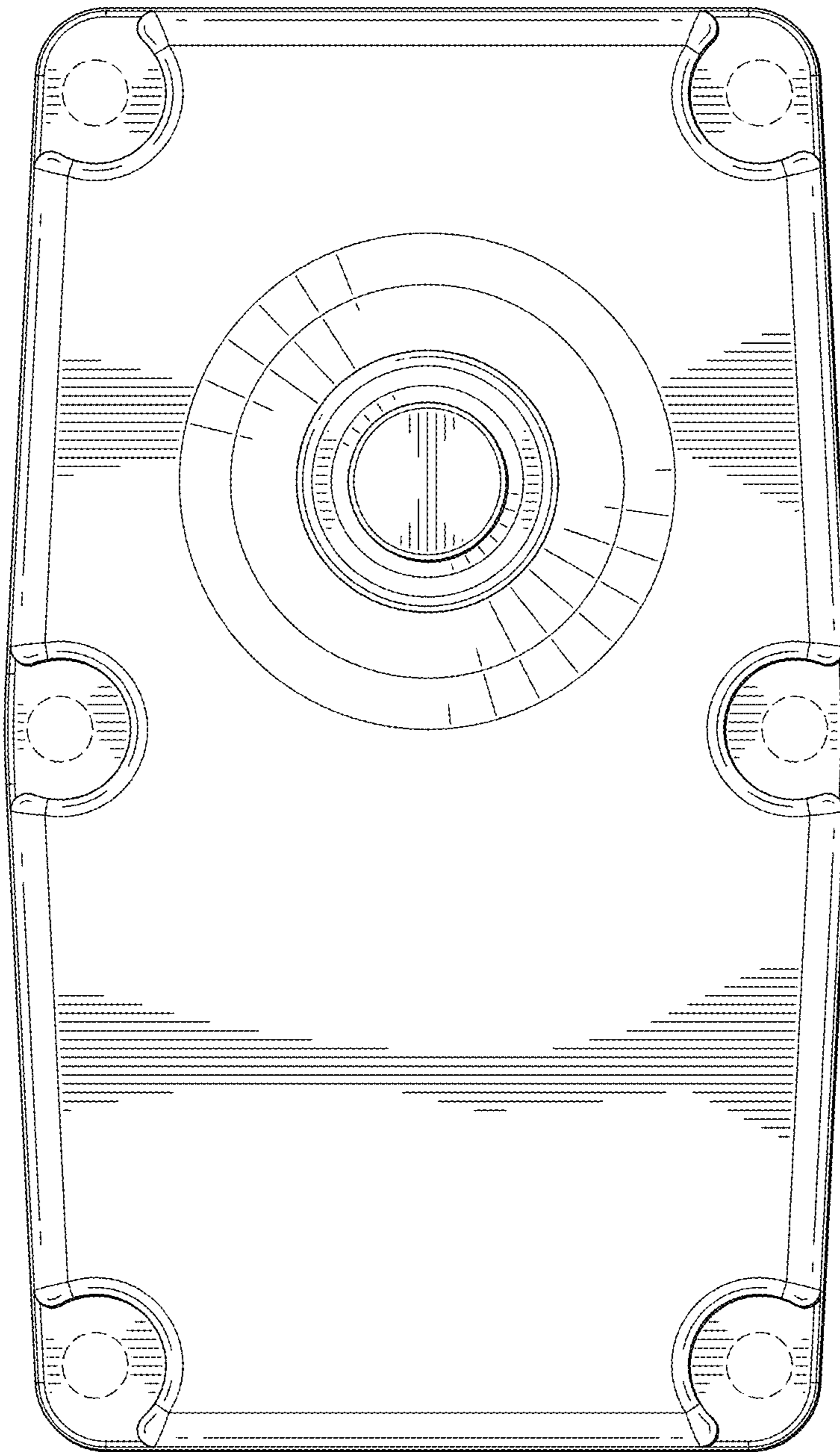


FIG. 6

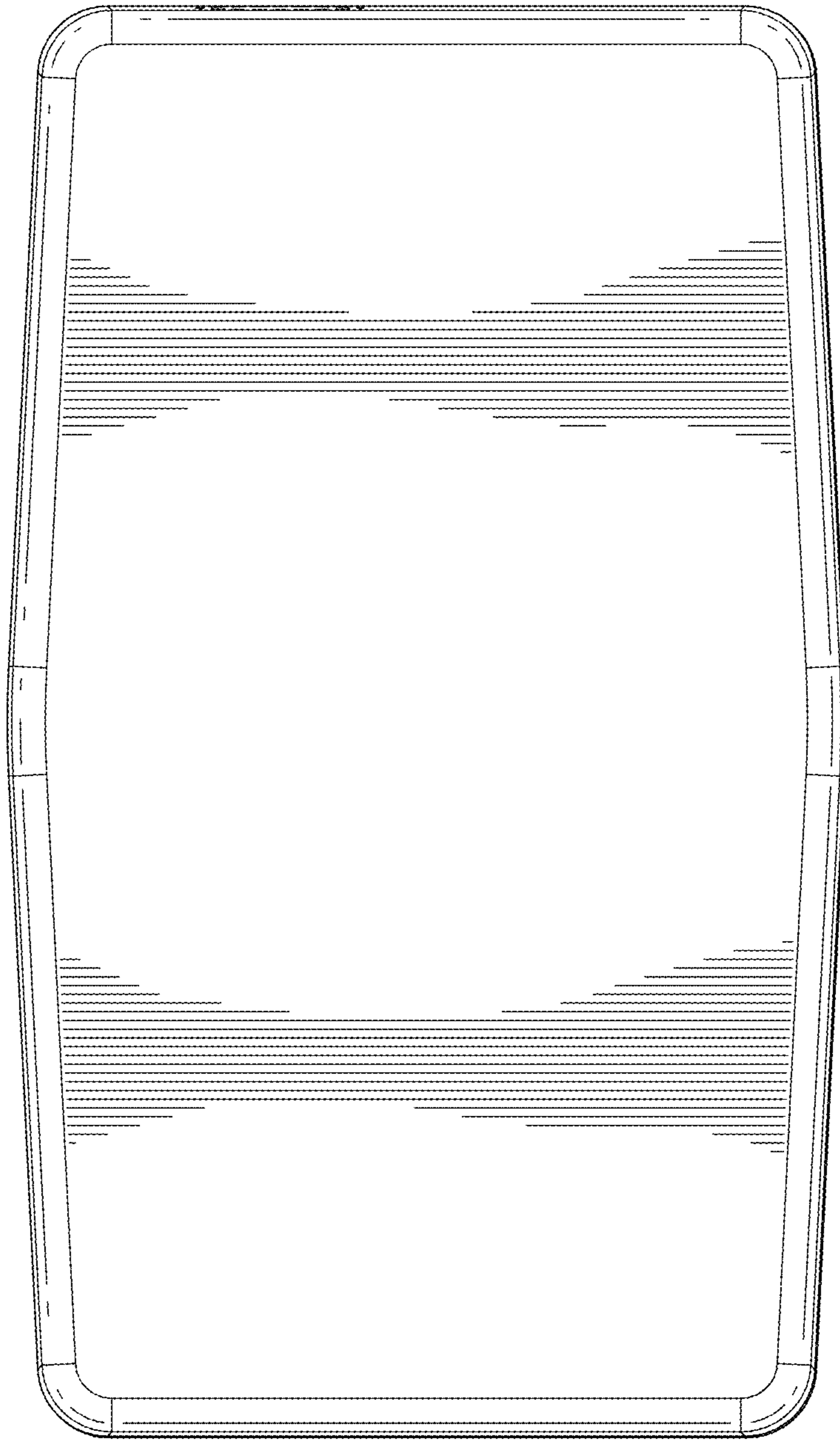


FIG. 7