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Li et al.

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(54) **PRINTED CIRCUIT BOARD OF SOLID-STATE MEMORY**

(71) Applicant: **Transcend Information, Inc.**, Taipei (TW)

(72) Inventors: **Tseng-Ho Li**, New Taipei (TW); **Chi-Yu Lin**, New Taipei (TW)

(73) Assignee: **Transcend Information, Inc.**, Taipei (TW)

(**) Term: **15 Years**

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(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

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USPC D13/182; 361/748, 752, 760, 761, 807, 361/749, 764, 736, 720, 722, 750, 762, 361/763, 751; 174/250, 253, 255, 68.1, 174/256, 257; 363/144, 147; 700/22; 318/567, 568.1
CPC H05K 3/284; H05K 3/30; H05K 3/301; H05K 3/303; H05K 1/18; H05K 1/181; H05K 1/182; H05K 1/183; H05K 1/185; H05K 1/00; H05K 1/02; H05K 1/0213; H05K 1/0284; H05K 1/0286; H05K 1/0287; H05K 1/11; H05K 1/189; H05K 7/1417; H05K 7/02; H05K 7/12; H05K 7/06; H05K 7/00; H05K 2201/05; H05K 2201/057; H05K 2201/09018; H01L 2924/14
See application file for complete search history.

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Primary Examiner — Elizabeth J Oswecki

(74) *Attorney, Agent, or Firm* — CKC & Partners Co., Ltd.

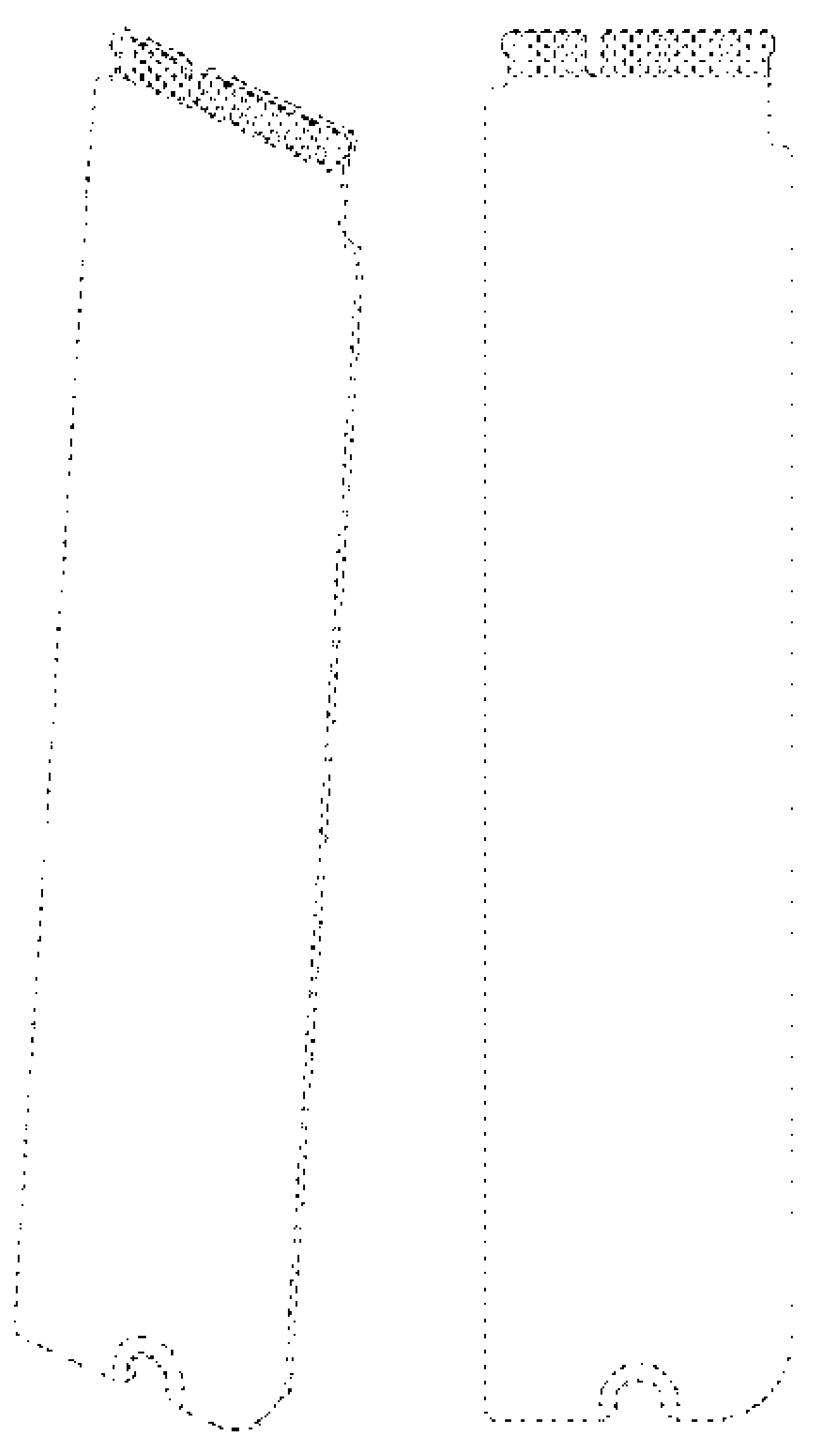
(57) CLAIM

The ornamental design for a printed circuit board of solid-state memory, as shown and described.

DESCRIPTION

FIG. **1** is a top, front, right perspective view of a printed circuit board of solid-state memory showing our new design;
FIG. **2** is a front elevational view thereof;
FIG. **3** is a rear elevational view thereof;
FIG. **4** is a left side elevational view thereof;
FIG. **5** is a right side elevational view thereof;
FIG. **6** is a top plan view thereof; and,
FIG. **7** is a bottom plan view thereof.
The broken lines represent portions of the structure that form no part of the claim.

1 Claim, 7 Drawing Sheets



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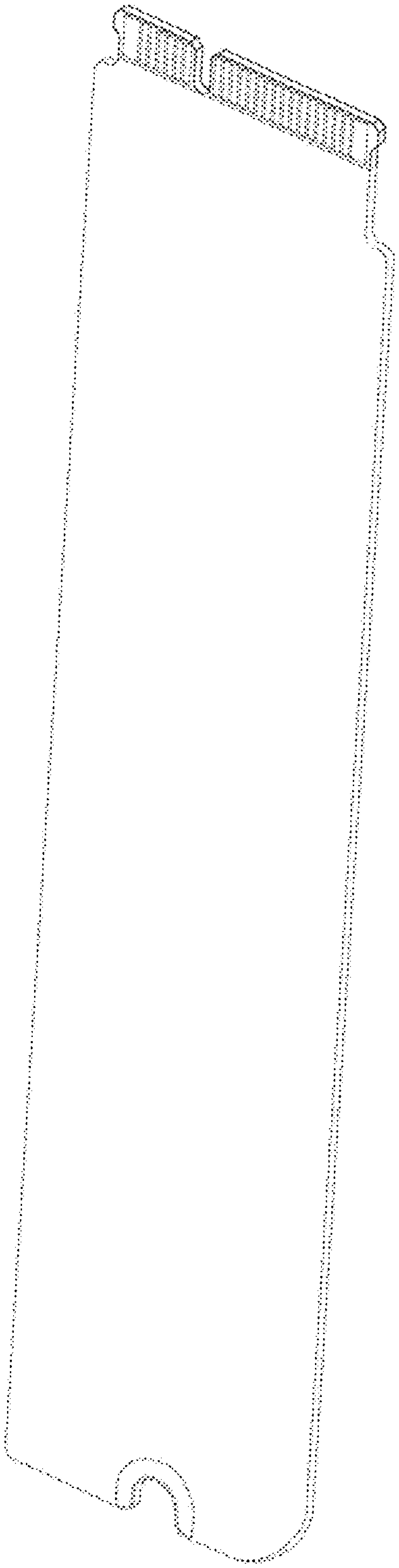

Fig. 1

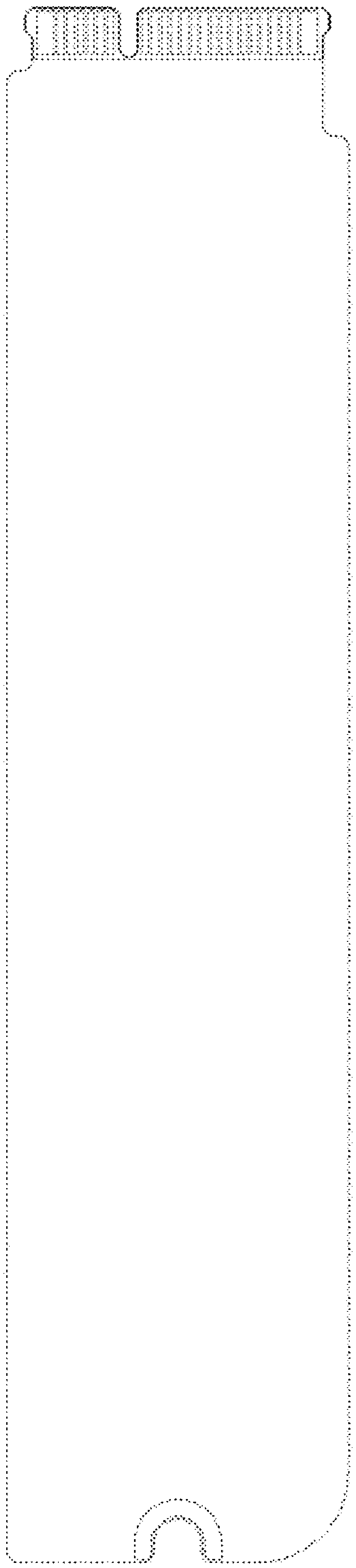

Fig. 2

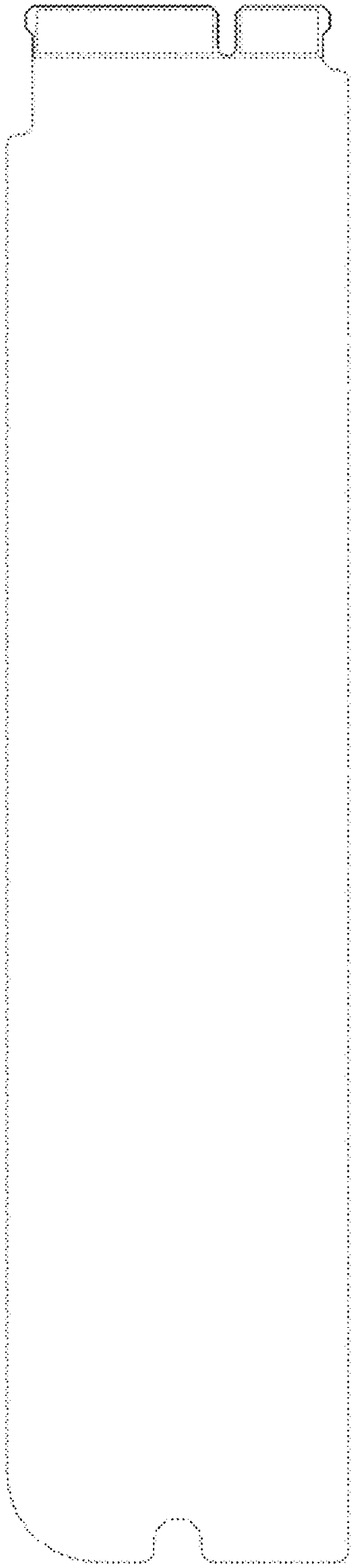

Fig. 3

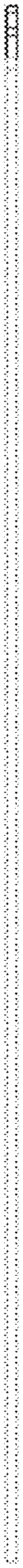

Fig. 4

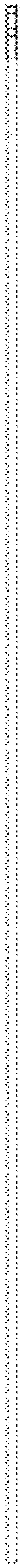

Fig. 5

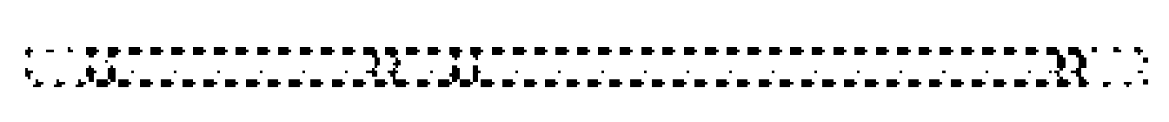

Fig. 6

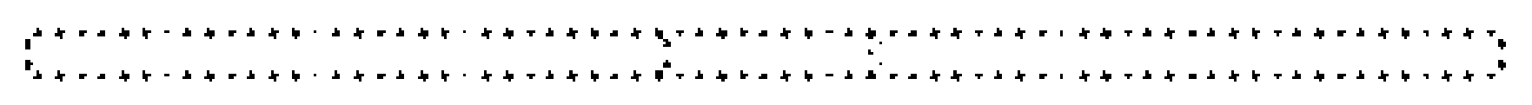

Fig. 7