



US00D794586S

(12) **United States Design Patent** (10) **Patent No.:** **US D794,586 S**  
**Takahashi et al.** (45) **Date of Patent:** **\*\* Aug. 15, 2017**

(54) **CIRCUIT BOARD**  
(71) Applicant: **MITSUBISHI ELECTRIC CORPORATION**, Tokyo (JP)  
(72) Inventors: **Kazunori Takahashi**, Tokyo (JP); **Naoki Mori**, Tokyo (JP)  
(73) Assignee: **Mitsubishi Electric Corporation**, Tokyo (JP)  
(\*\*) Term: **15 Years**

D292,698 S \* 11/1987 DeVita ..... D13/182  
5,296,652 A \* 3/1994 Miller, Jr. .... H05K 3/325  
174/260  
D357,228 S \* 4/1995 Anton ..... D13/182  
D359,476 S \* 6/1995 Sakashita ..... D13/182  
D376,134 S \* 12/1996 Anton ..... D13/182  
D396,449 S \* 7/1998 Taylor ..... D13/182  
D430,856 S \* 9/2000 Wilkerson ..... D13/182  
6,613,988 B2 \* 9/2003 Powers ..... H01R 23/68  
174/254  
D485,536 S \* 1/2004 Dang ..... D13/182  
6,760,225 B1 \* 7/2004 Chen ..... H05K 1/0209  
174/252

(Continued)

(21) Appl. No.: **29/560,294**

*Primary Examiner* — Elizabeth J Oswecki

(22) Filed: **Apr. 5, 2016**

(74) *Attorney, Agent, or Firm* — Stuebaker & Brackett PC

(30) **Foreign Application Priority Data**

Nov. 12, 2015 (JP) ..... 2015-025297

(51) **LOC (10) Cl.** ..... **13-03**

(52) **U.S. Cl.**  
USPC ..... **D13/182**

(58) **Field of Classification Search**  
USPC ..... D13/182; 174/68.1, 250, 253, 255, 256;  
318/567, 568.1; 361/600, 601, 718, 719,  
361/720, 728, 736, 748, 751, 752, 760,  
361/761, 807; 439/55, 65, 68, 69, 76.1,  
439/92, 93, 95  
CPC ..... H05K 3/00; H05K 3/30; H05K 3/301;  
H05K 3/303; H05K 3/34; H05K 3/3405;  
H05K 3/341; H05K 3/36; H05K 3/361;  
H05K 3/363; H05K 3/40; H05K 7/14;  
H05K 7/1422; H05K 7/00; H05K 1/18;  
H05K 1/02; H05K 1/181; H05K 1/182;  
H05K 1/183; H05K 1/184; H05K 1/189;  
H05K 1/00  
See application file for complete search history.

(57) **CLAIM**

The ornamental design for a circuit board, as shown and described.

**DESCRIPTION**

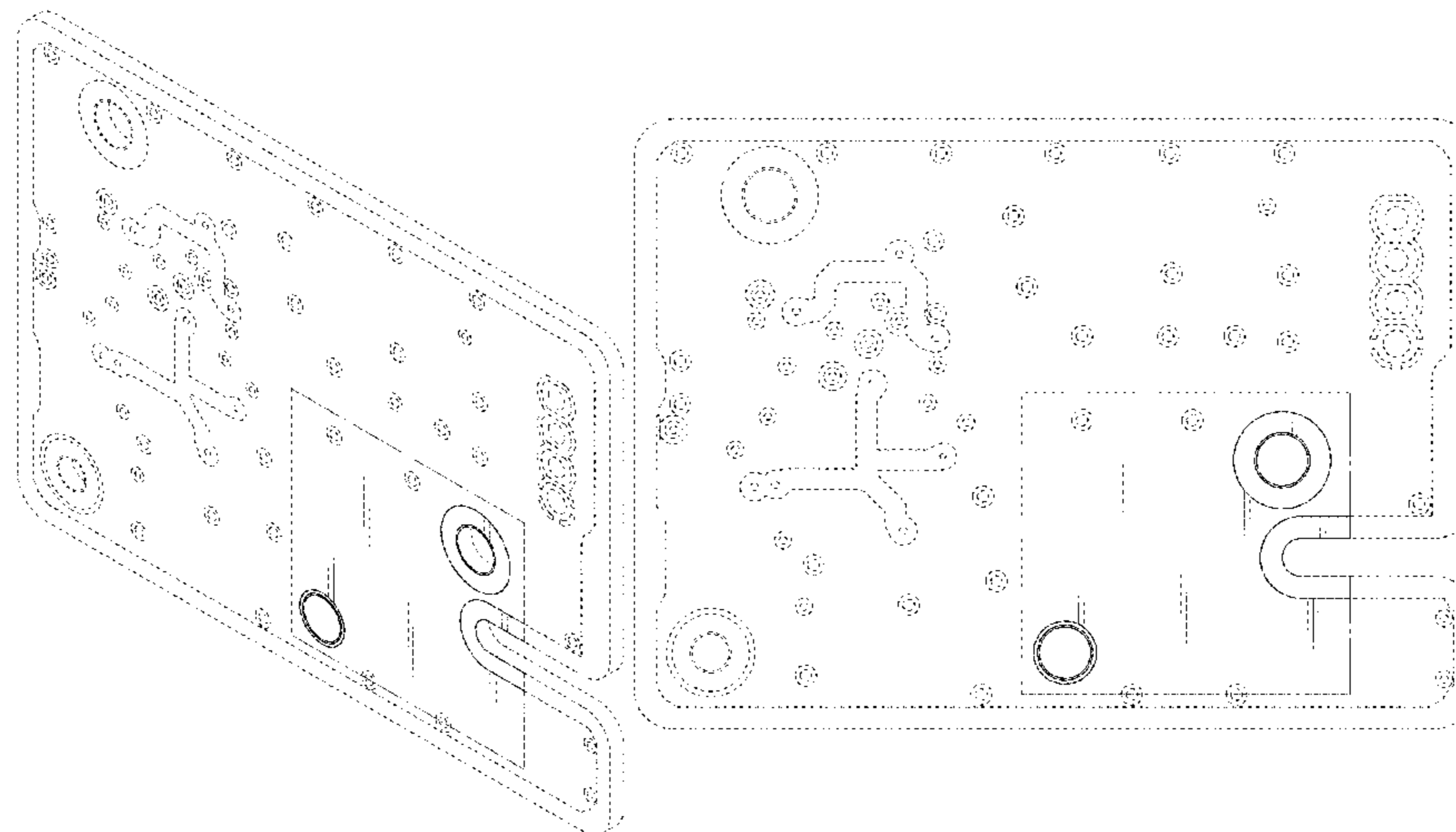
FIG. 1 is a rear, top, left side perspective view of a circuit board showing our new design;  
FIG. 2 is a front view thereof;  
FIG. 3 is a rear view thereof;  
FIG. 4 is a left side view thereof;  
FIG. 5 is a right side view thereof;  
FIG. 6 is a top view thereof;  
FIG. 7 is a bottom view thereof; and,  
FIG. 8 is another perspective view shown in a used condition in a device shown in broken lines.  
The broken line showing of the circuit board is included for the purpose of illustrating portions of the circuit board and forms no part of the claimed design. The dot and dashed lines mean a boundary between the claimed portion and the non-claimed portion.

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

3,072,734 A \* 1/1963 Fox ..... H02B 1/043  
174/254  
D255,351 S \* 6/1980 Pettijohn ..... D13/182

**1 Claim, 6 Drawing Sheets**



(56)

**References Cited**

U.S. PATENT DOCUMENTS

D508,681	S	*	8/2005	Enderlein	.....	D13/182
D525,213	S	*	7/2006	Enderlein	.....	D13/182
D611,014	S	*	3/2010	Huang	.....	D13/182
D639,756	S	*	6/2011	Greene, Jr.	.....	D13/182
D642,546	S	*	8/2011	Greene, Jr.	.....	D13/182
D738,833	S	*	9/2015	Quintana	.....	D13/182
D774,478	S	*	12/2016	Li	.....	D13/182
2009/0268390	A1	*	10/2009	King	.....	G06F 13/409 361/679.33

\* cited by examiner

Fig. 1

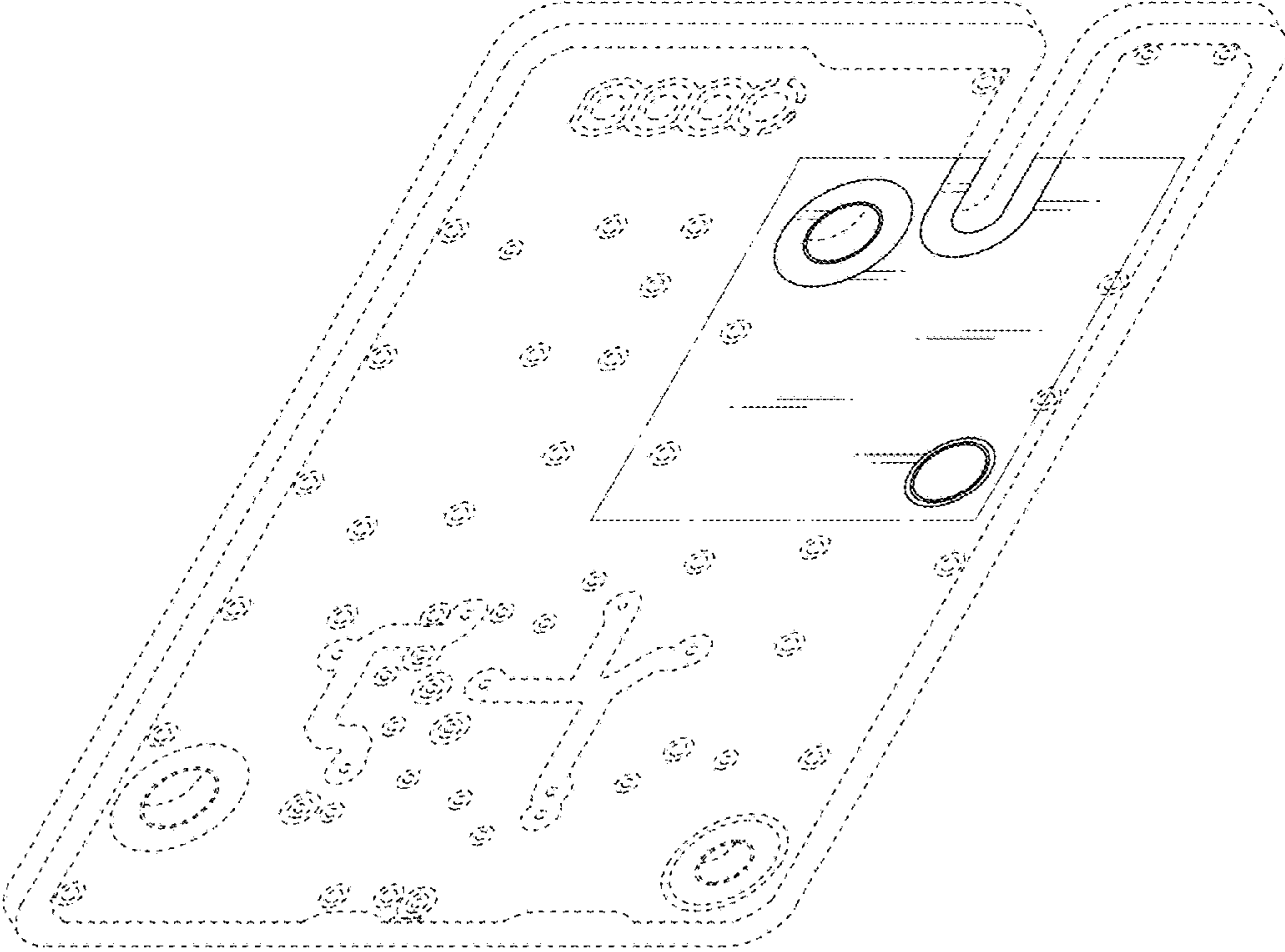


Fig. 2

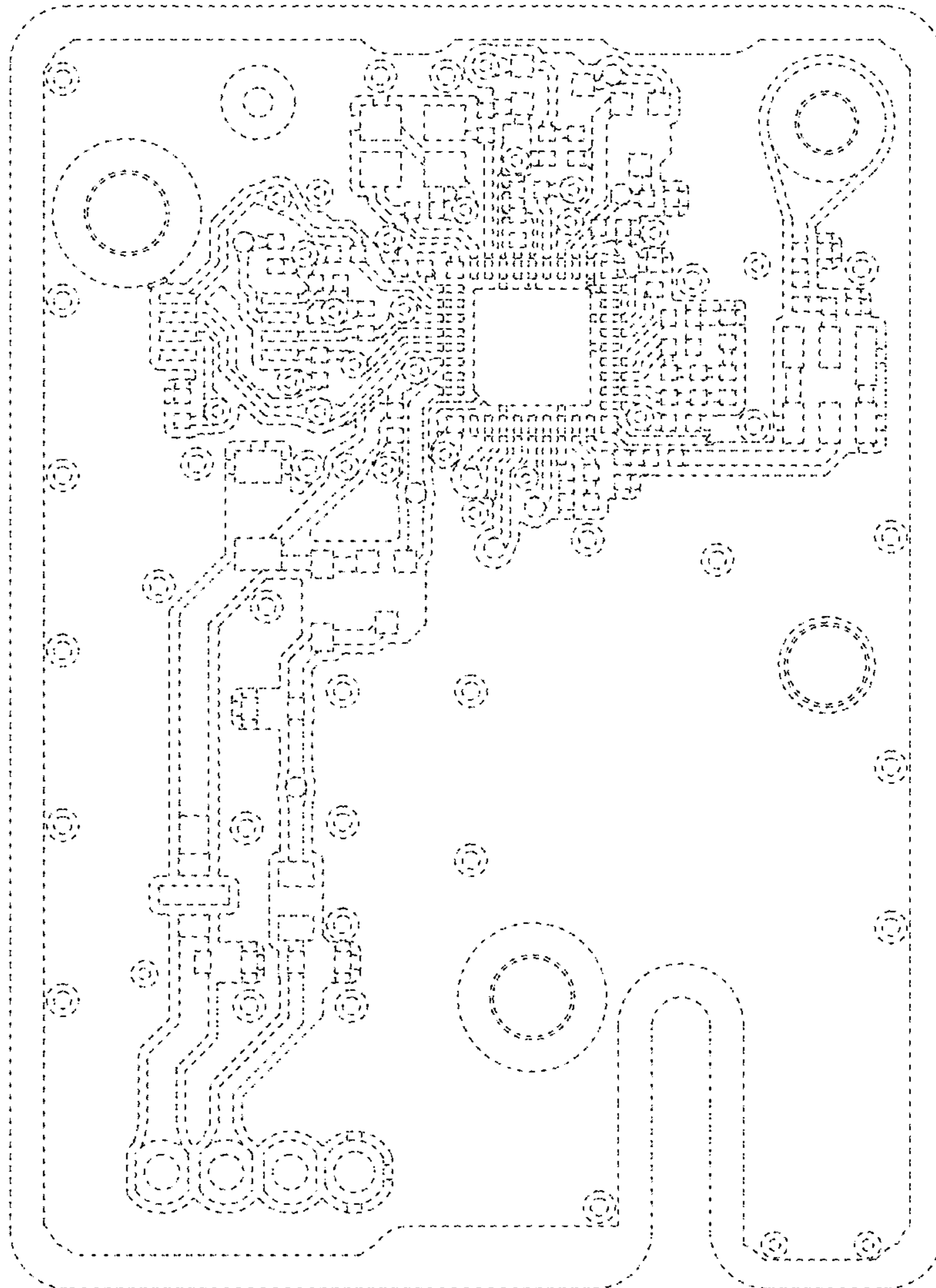


Fig. 3

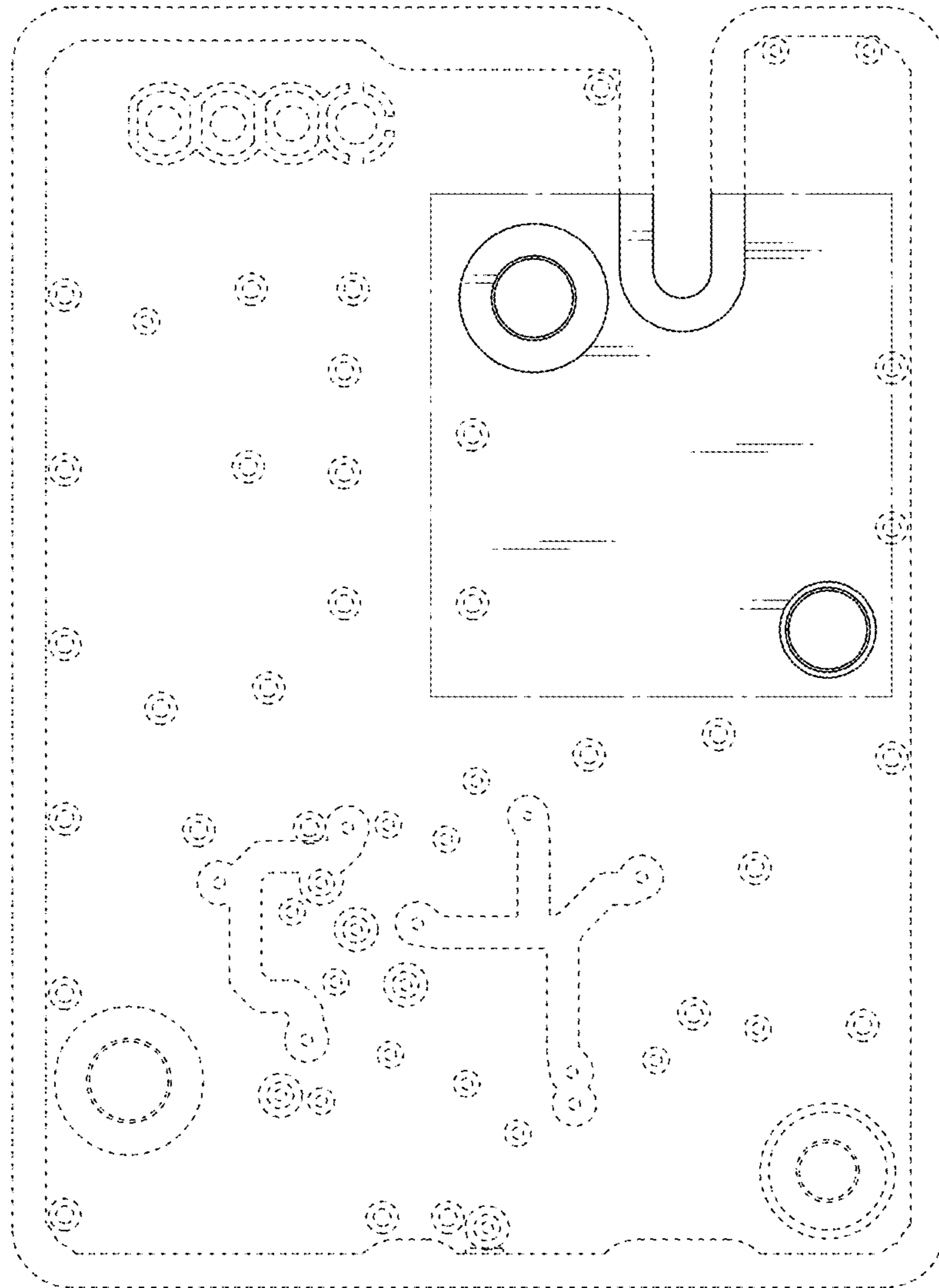


Fig. 5

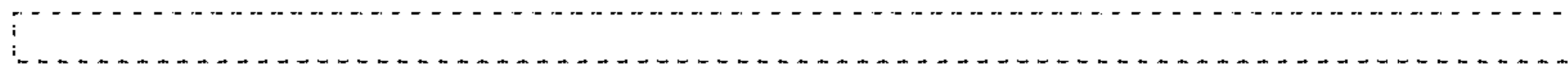


Fig. 4

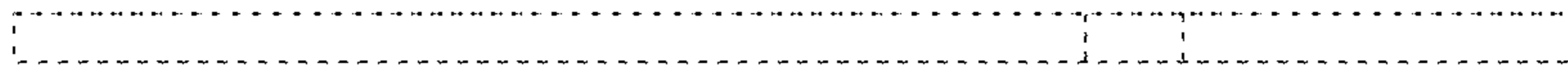




Fig. 6

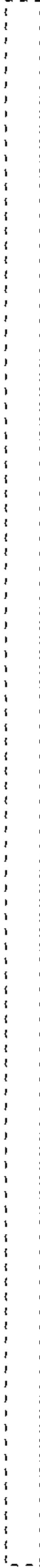


Fig. 7

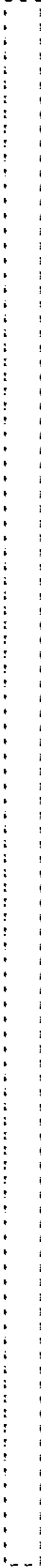


Fig. 8

