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Murata et al.

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(54) **HEATER FOR SEMICONDUCTOR THERMAL PROCESS**

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(**) Term: **15 Years**

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(30) **Foreign Application Priority Data**

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(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/179, 182; D15/144, 144.1, 199; D30/151, 152; D11/130; 414/935–941, 414/217, 147; 392/407, 409, 416, 418; 219/385, 624, 630, 638
CPC ... H01L 21/67; H01L 21/67011; H01L 21/02; H01L 21/02002; H01L 21/67098; H01L 21/67109; H01L 21/00; H01L 23/34; H01L 23/345; H01L 23/3677; C23C 16/4586; C23C 16/46; C23C 16/466; C23C 16/481; C30B 13/20; H05B 6/36; H05B 6/362; H05B 6/44
See application file for complete search history.

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(57) **CLAIM**

The ornamental design for a heater for semiconductor thermal process, as shown and described.

DESCRIPTION

FIG. **1** is a front, bottom, right side perspective view of a heater for semiconductor thermal process showing our new design;
FIG. **2** is a front elevational view thereof;
FIG. **3** is a rear elevational view thereof;
FIG. **4** is a left side elevational view thereof;
FIG. **5** is a right side elevational view thereof;
FIG. **6** is a top plan view thereof; and,
FIG. **7** is a bottom plan view thereof.
The dashed-dot-dashed lines represent the boundary lines of the claimed design.

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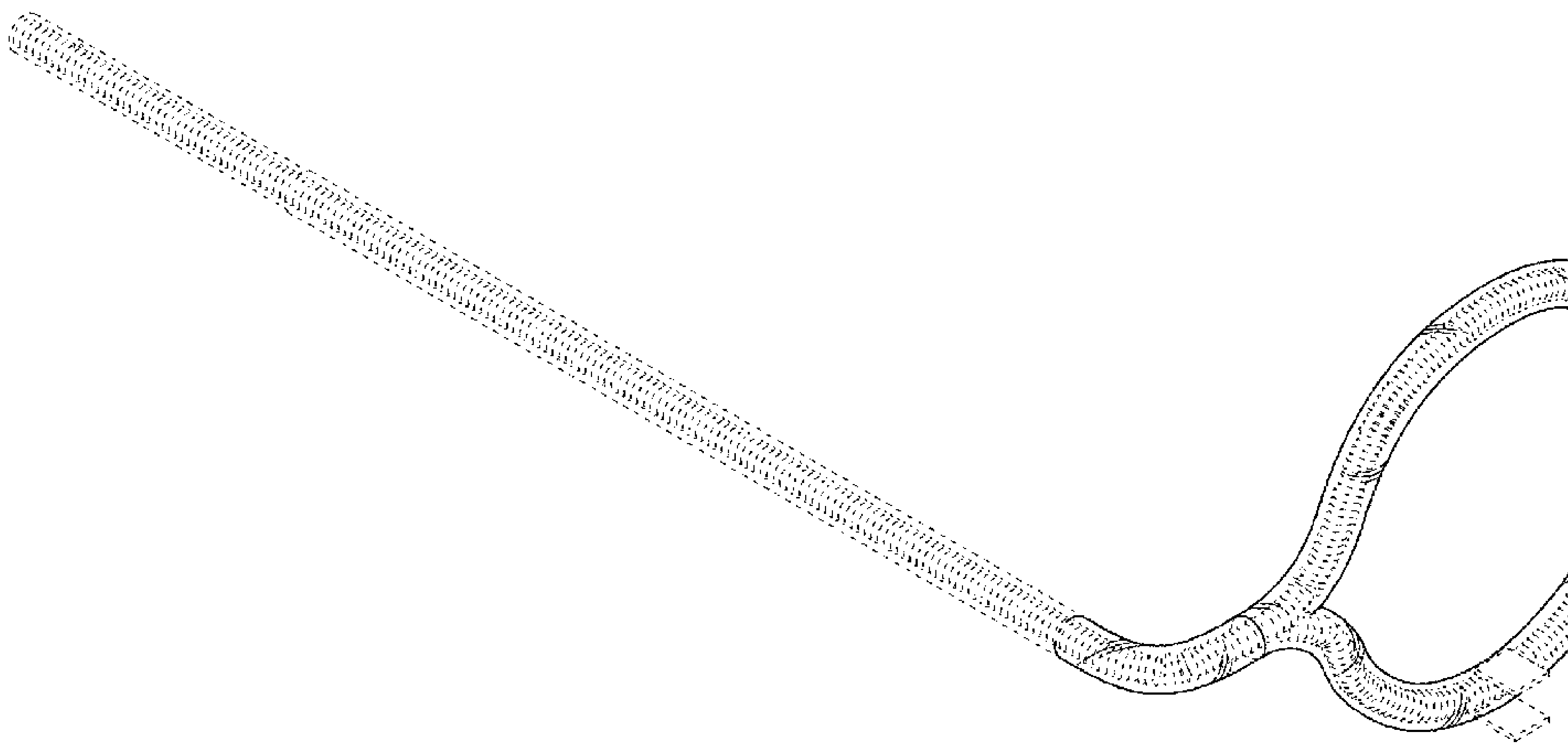

The broken lines shown in the drawings represent portions of the heater for semiconductor thermal process that form no part of the claimed design.

1 Claim, 5 Drawing Sheets

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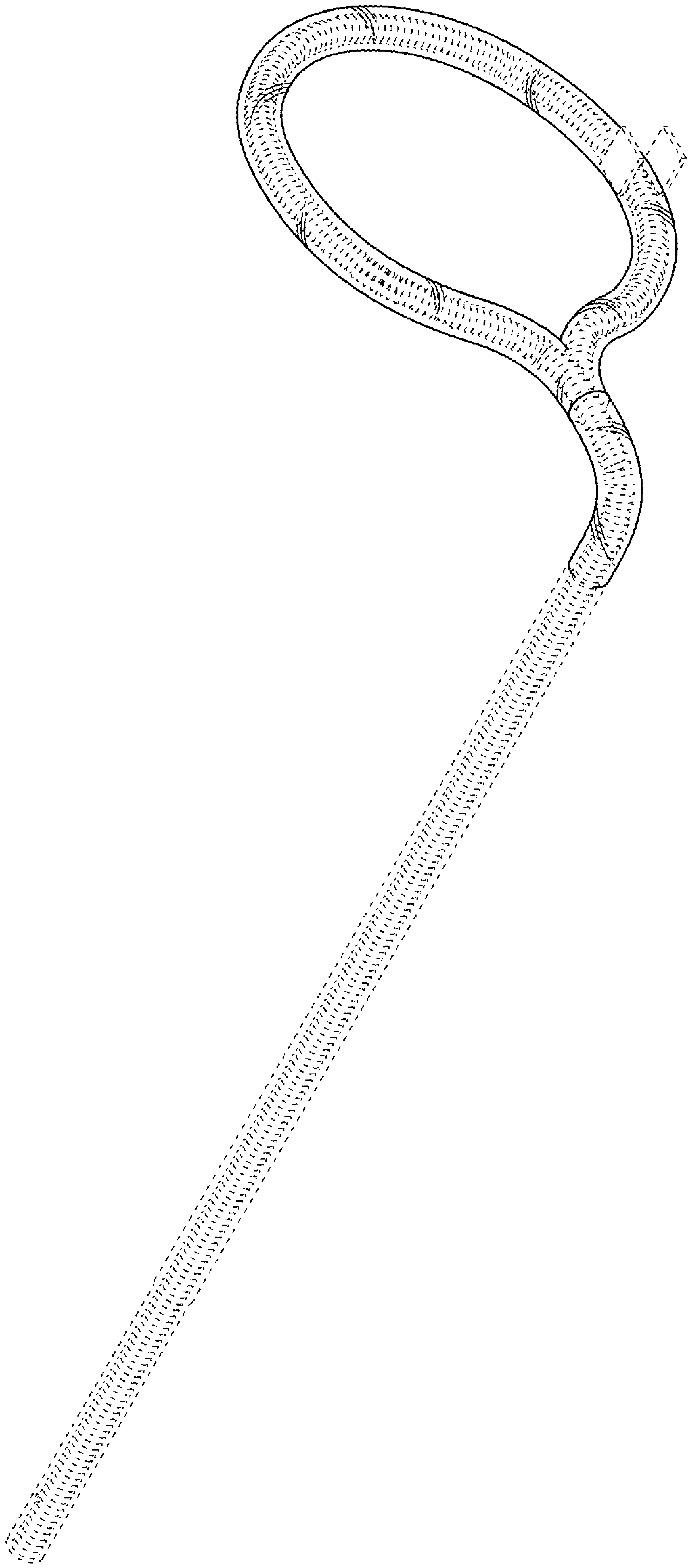

FIG. 1

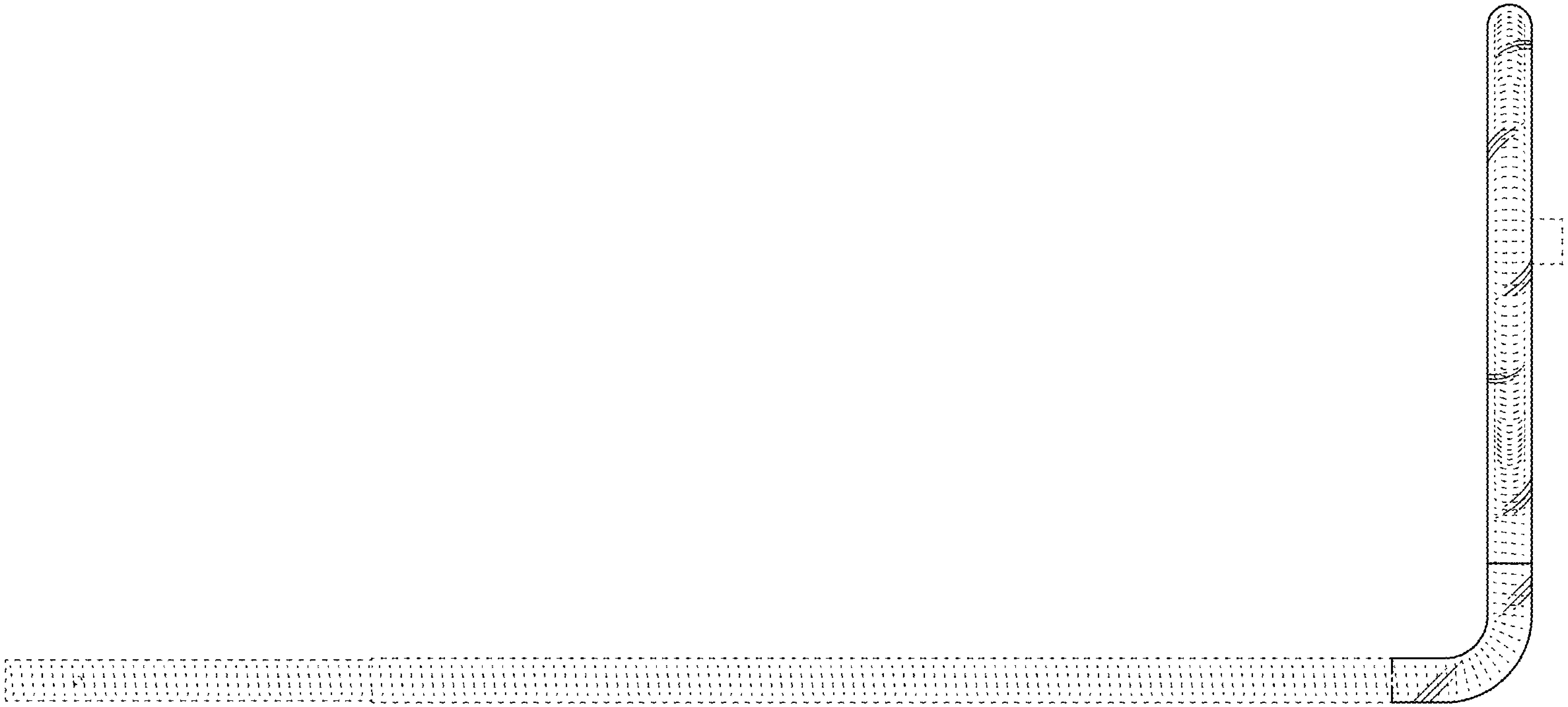

FIG. 2

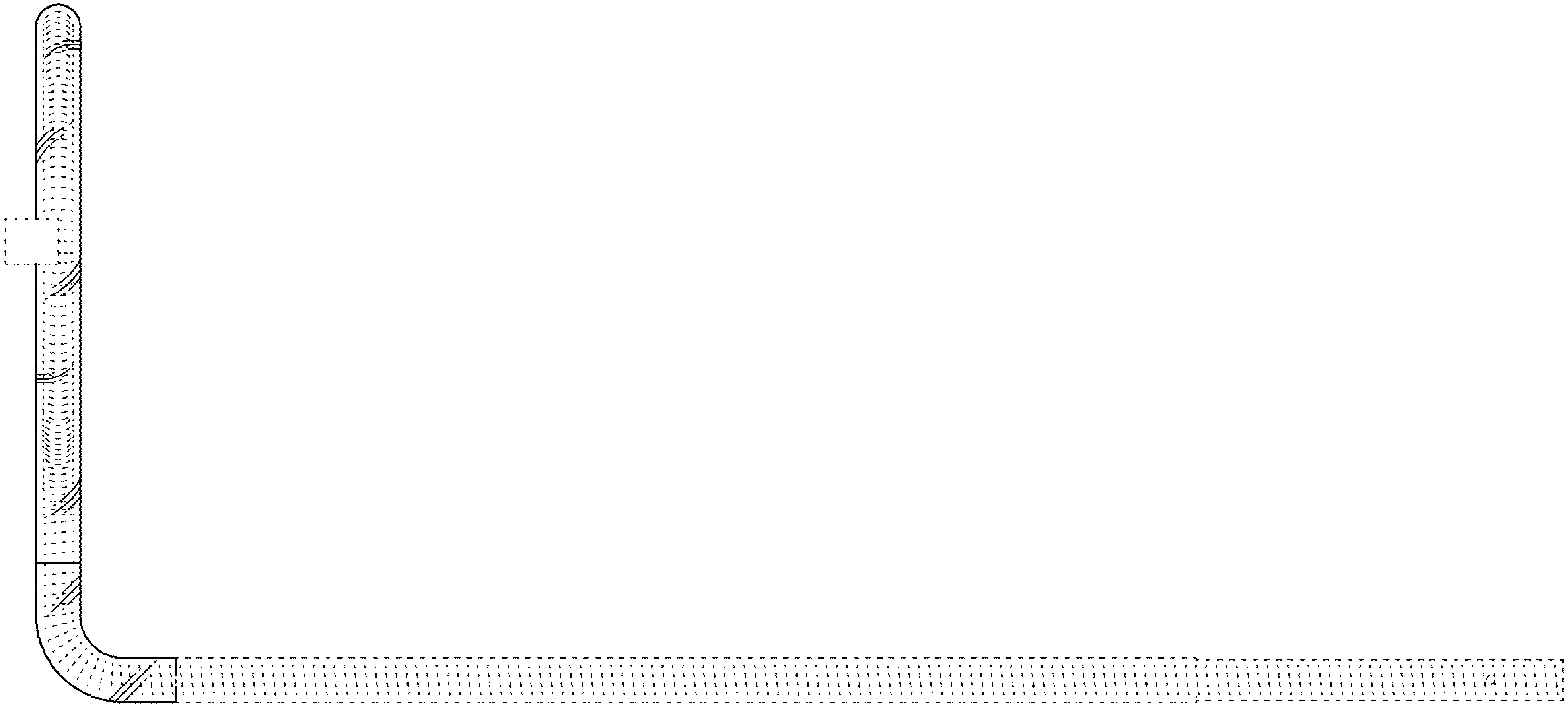

FIG. 3

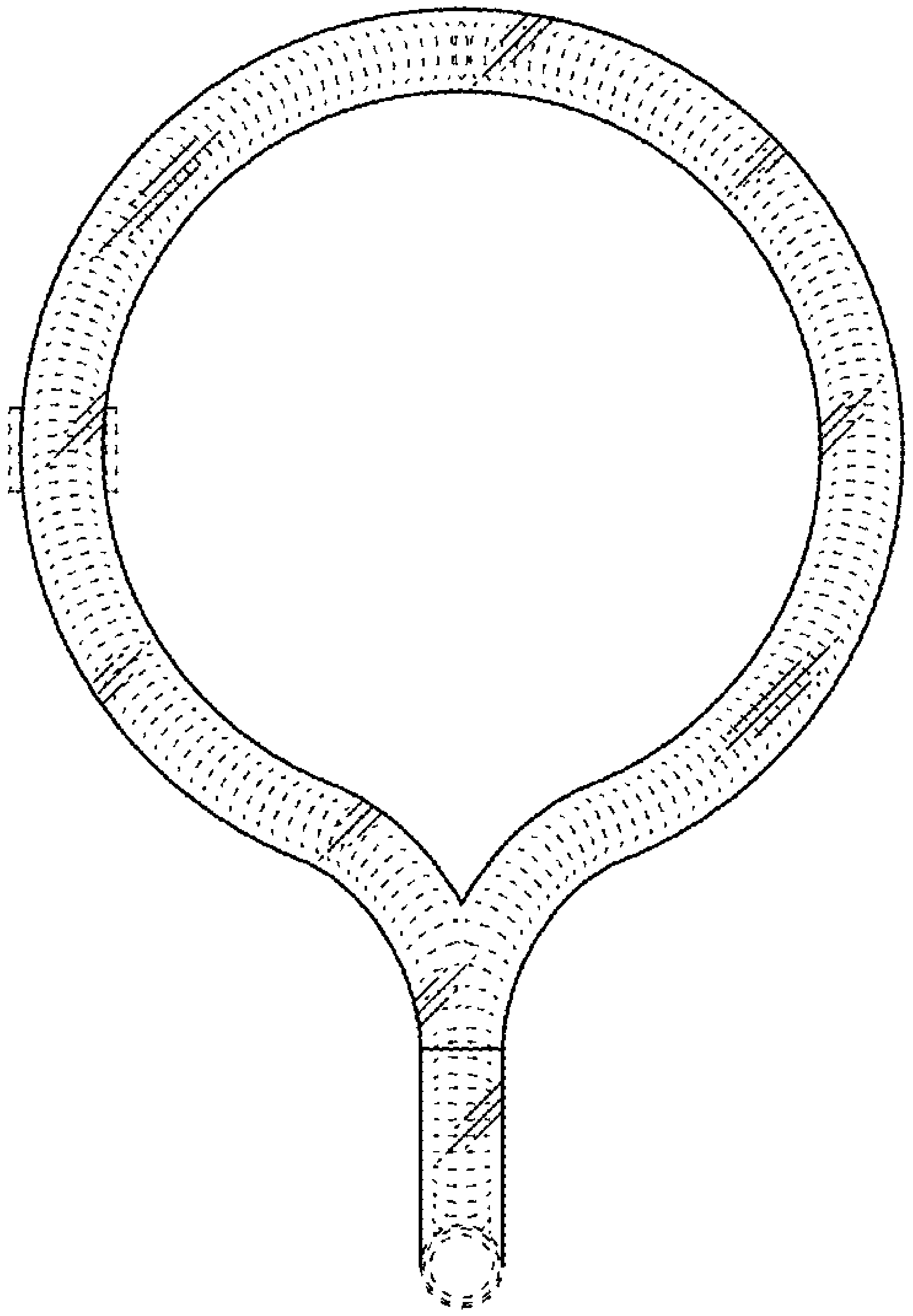

FIG. 4

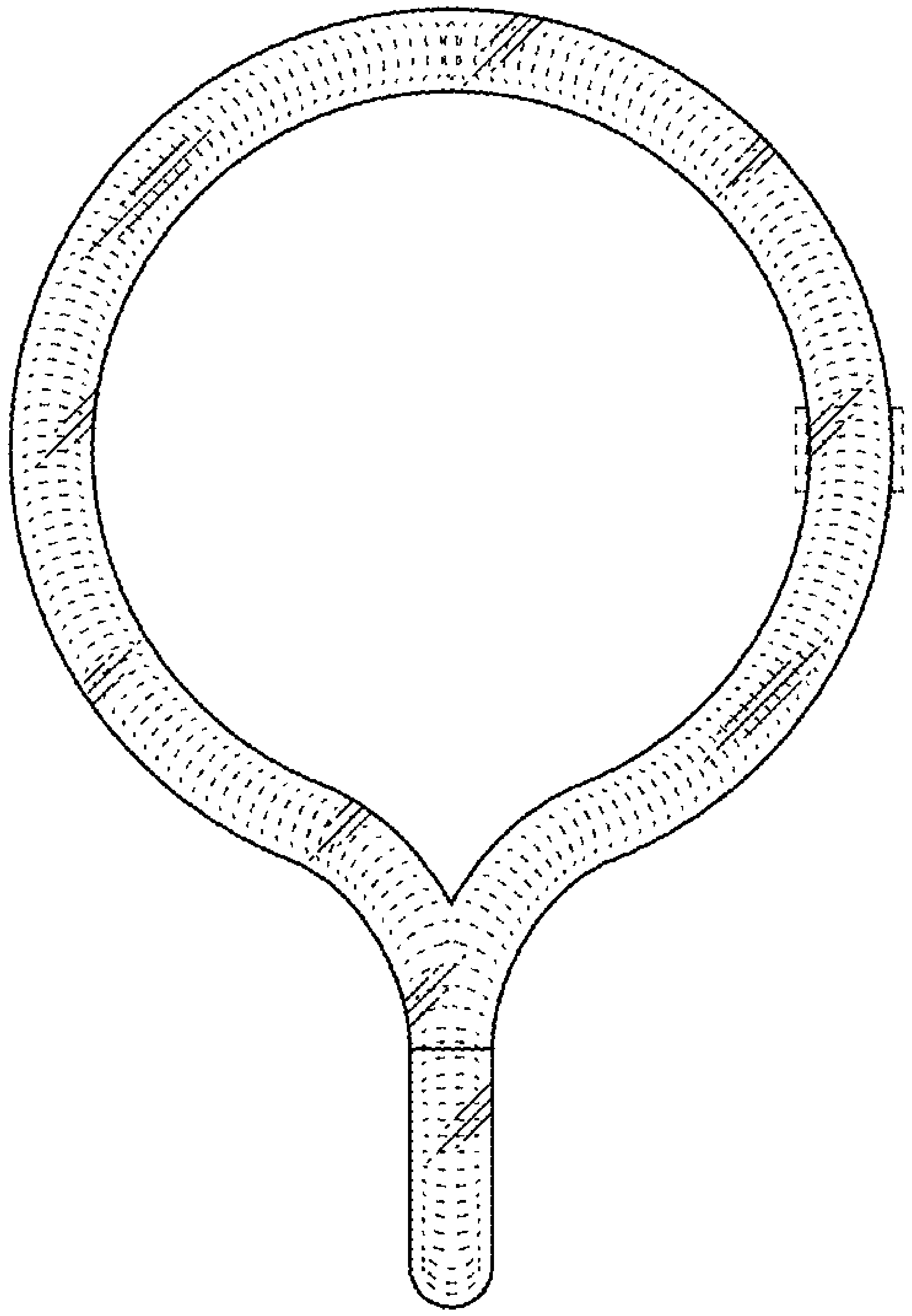

FIG. 5

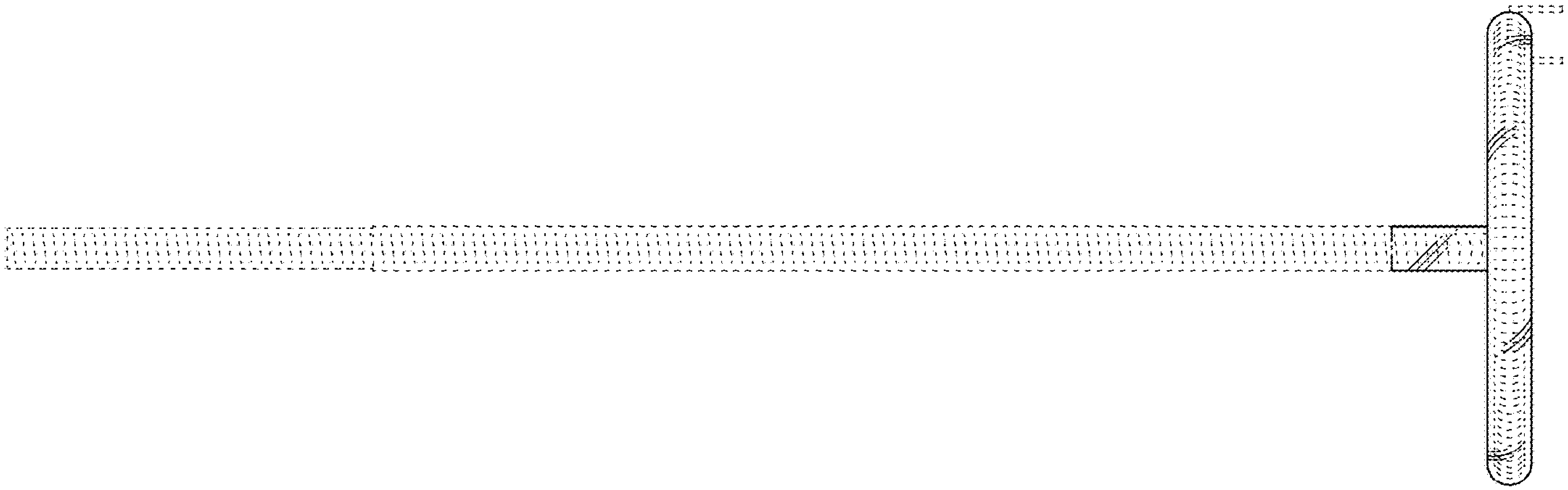

FIG. 6

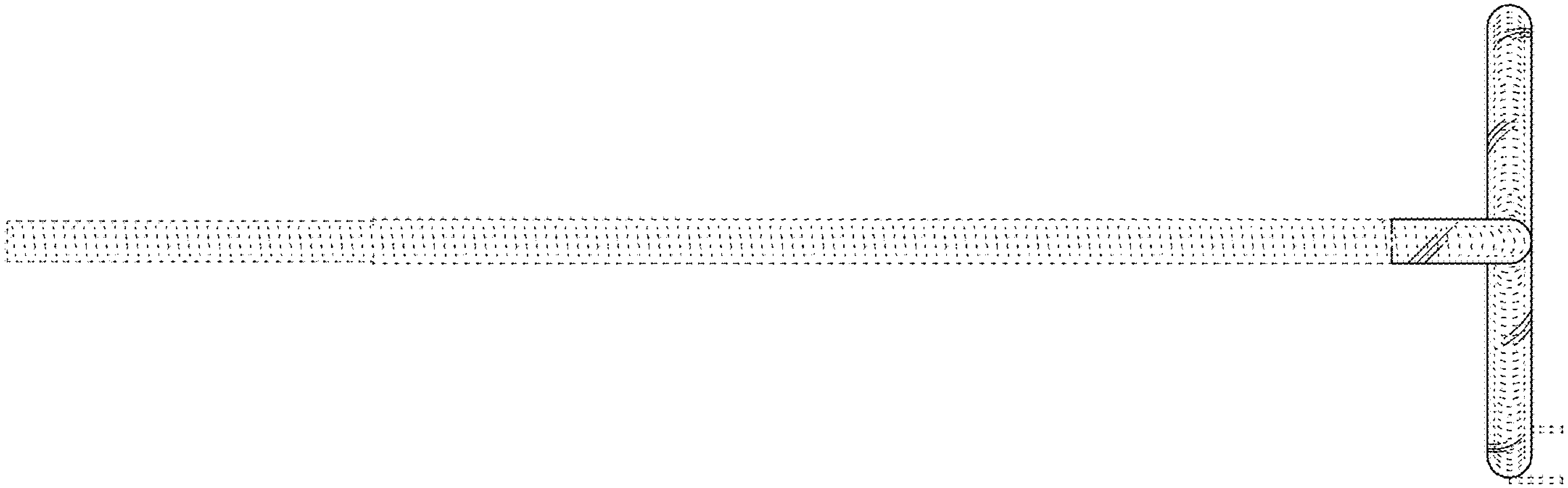

FIG. 7