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(12) **United States Design Patent**
Matsumoto et al.

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(54) **SUBSTRATE FOR AN ELECTRONIC CIRCUIT**

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(**) Term: **15 Years**

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(30) **Foreign Application Priority Data**

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(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/110, 118, 123, 133, 146, 147, 173,
D13/182, 184, 199; D14/436
CPC C09K 19/00; C09K 19/02; G06F 1/16; G06F
1/183; G06F 1/184; G06F 1/187; G11B
33/12; G11B 33/123; G11B 33/124;
G11B 33/125; G11C 7/22; G11C 14/00;
G11C 16/10; G11C 16/14; G11C 16/26;
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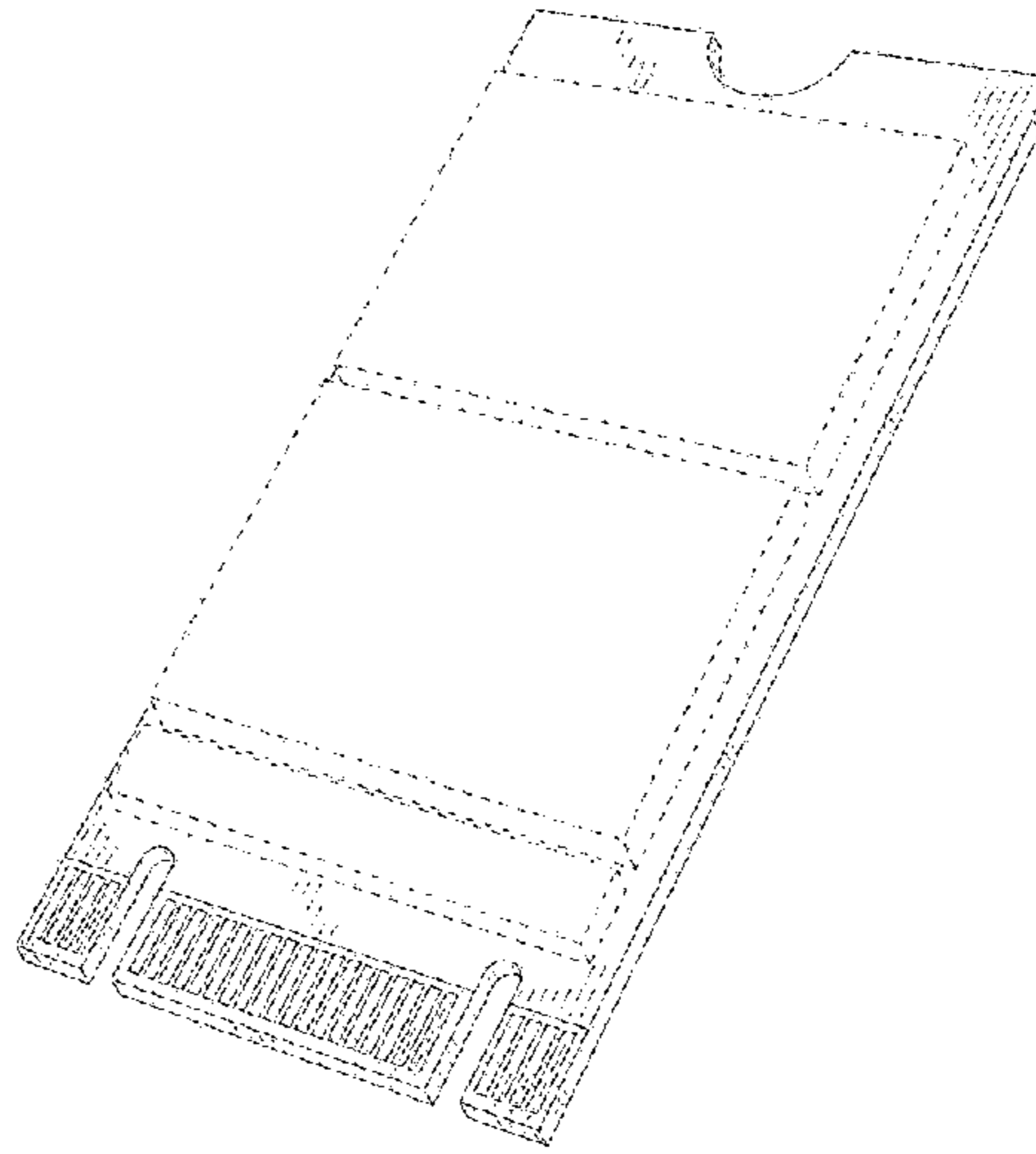
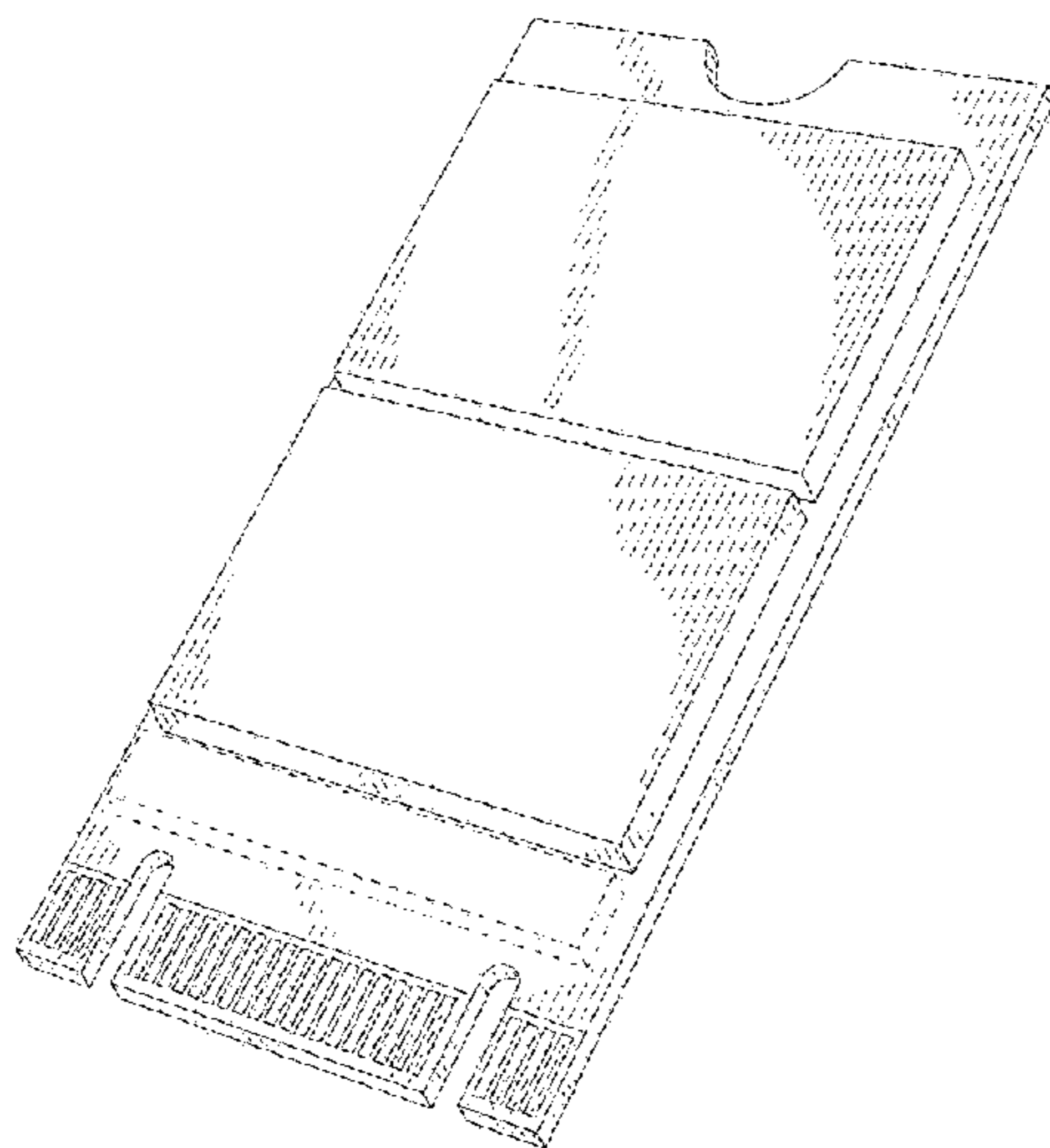
(57) **CLAIM**

The ornamental design for a substrate for an electronic circuit, as shown and described.

DESCRIPTION

FIG. 1 is a front, bottom and right side perspective view of a substrate for an electronic circuit, showing our new design; FIG. 2 is a rear, bottom and left side perspective view thereof; FIG. 3 is a front view thereof; FIG. 4 is a rear view thereof; FIG. 5 is a top view thereof; FIG. 6 is bottom view thereof; FIG. 7 is a right side view thereof, the left side being symmetrical; FIG. 8 is a cross sectional view thereof, taken along line 8-8 in FIG. 3; and, FIG. 9 is a cross sectional view thereof, taken along line 9-9 in FIG. 3.
The broken line portion of the figure drawings is included to show portions of the article that form no part of the claimed design.

1 Claim, 6 Drawing Sheets



(58) **Field of Classification Search**

CPC G11C 16/30; G11C 29/12; H01L 23/00;
 H01L 23/28; H01L 23/29; H01L 23/298;
 H01L 23/31; H01L 23/34; H01L 25/00;
 H01L 25/065; H01L 25/072; H01L 25/18;
 H05K 1/111; H05K 1/112; H05K 3/00;
 H05K 5/00; H05K 7/00; H05K 7/12
 See application file for complete search history.

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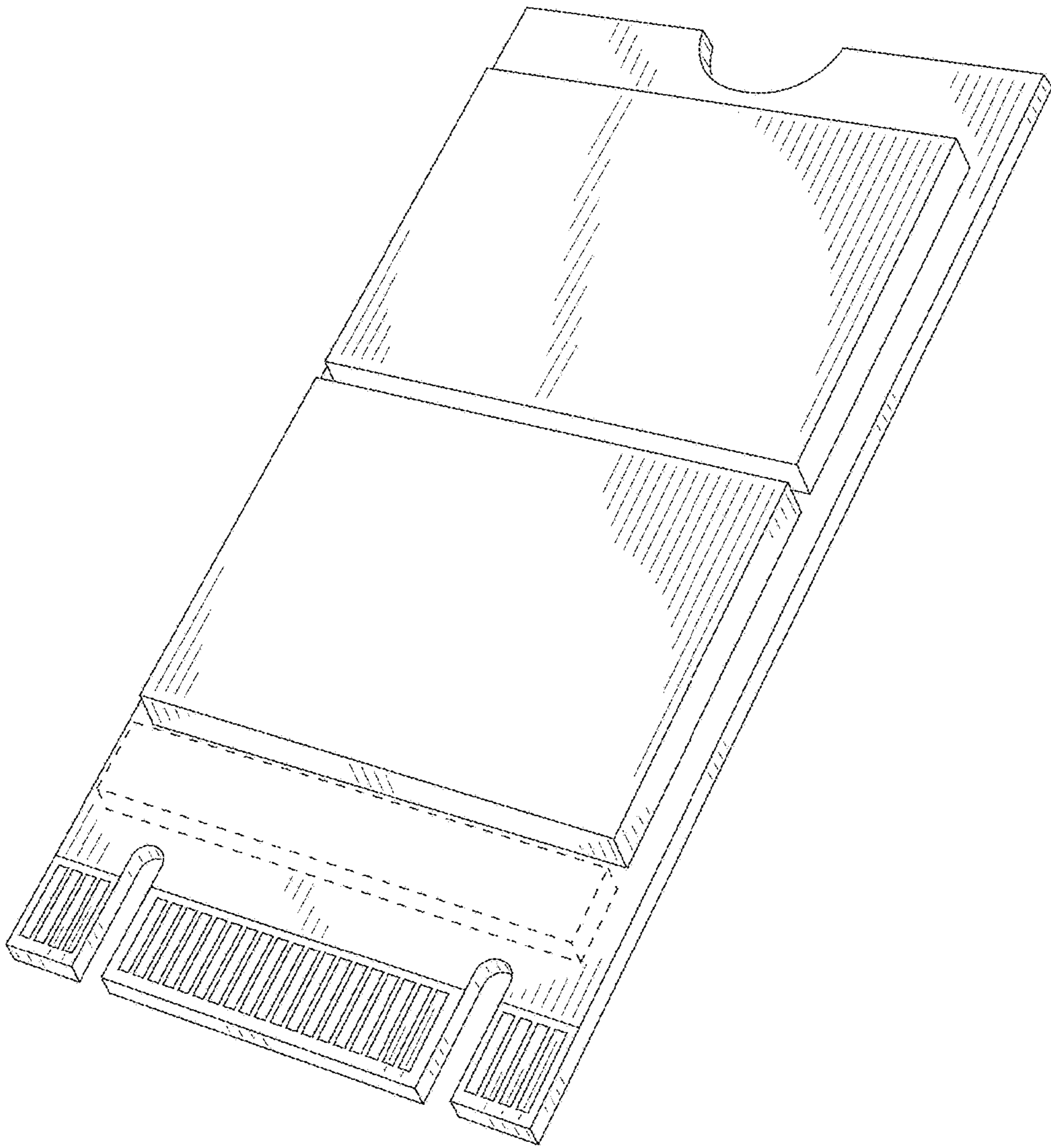


Fig. 1

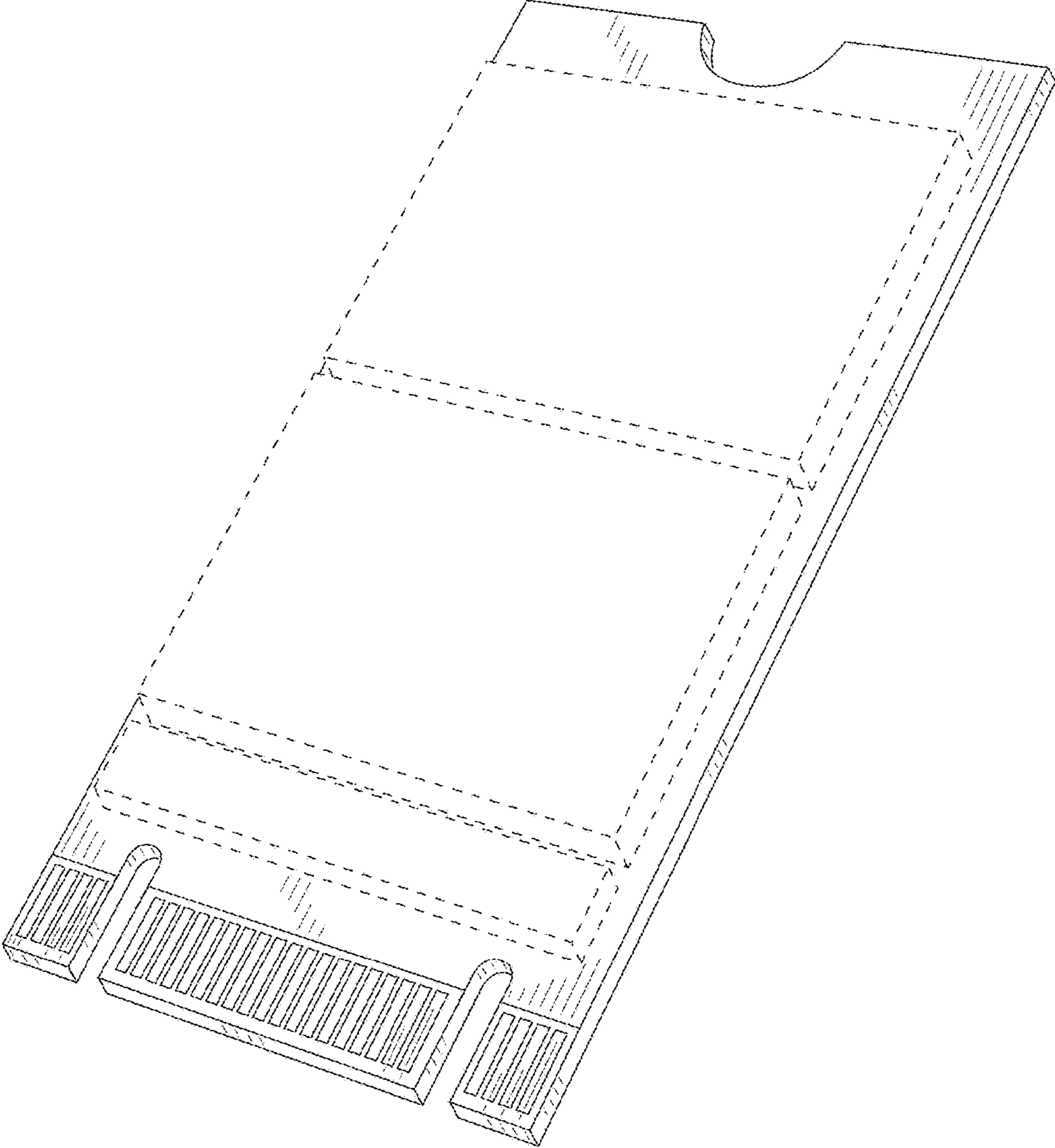


Fig.2

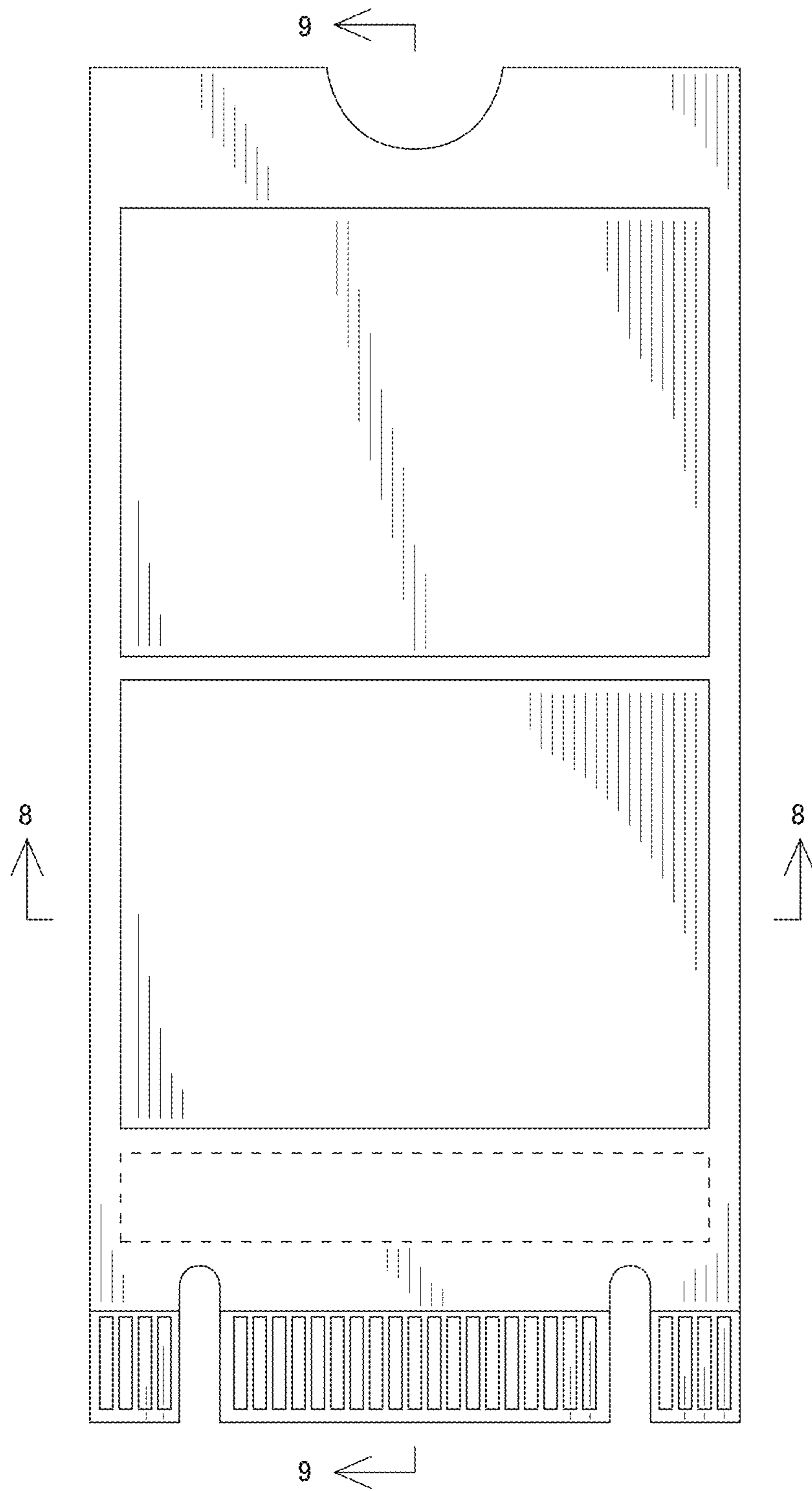


Fig. 3

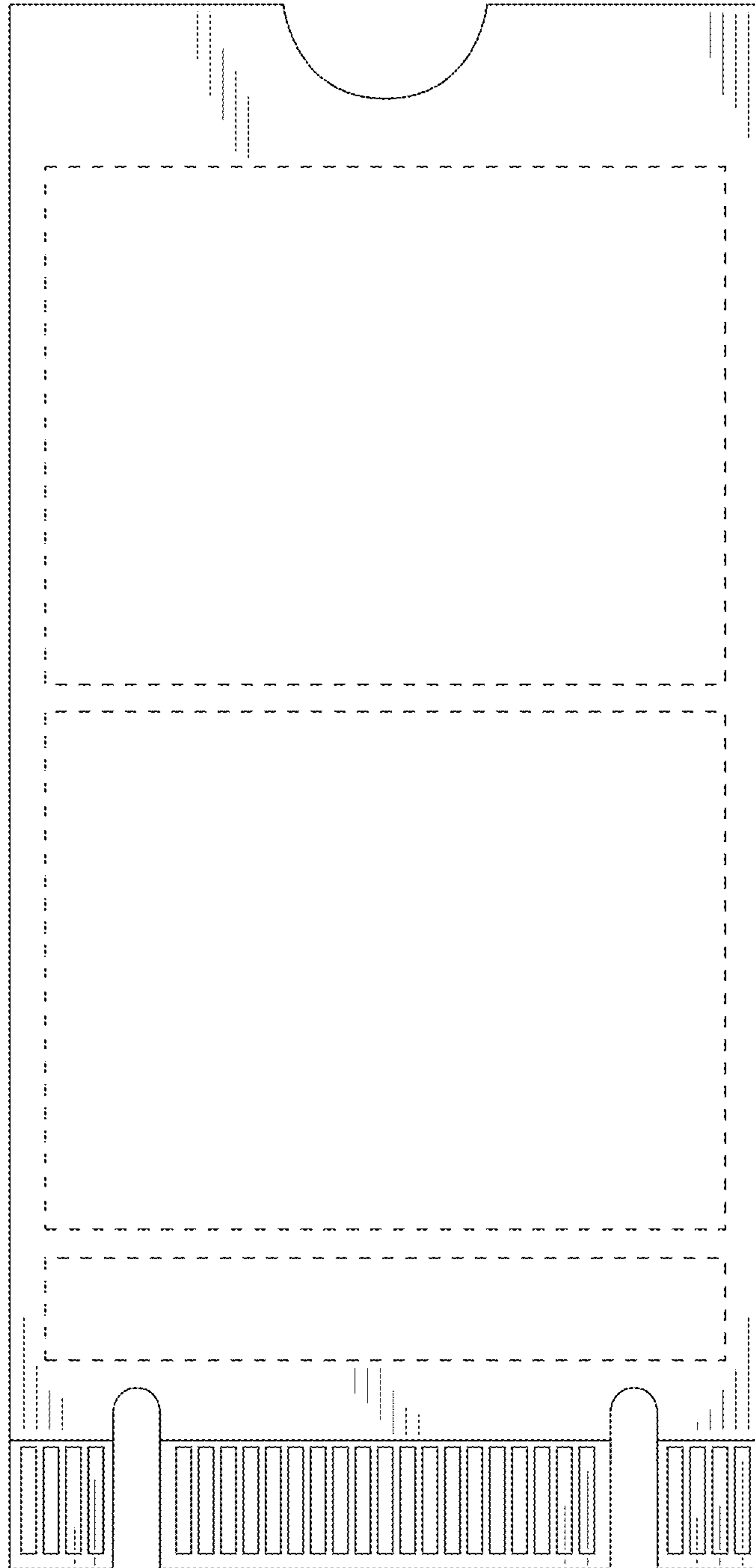


Fig.4

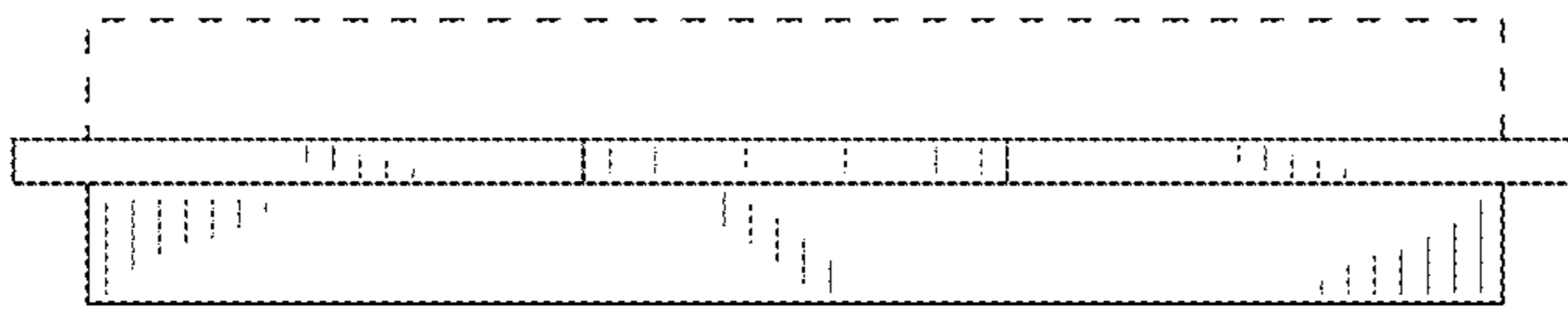


Fig. 5

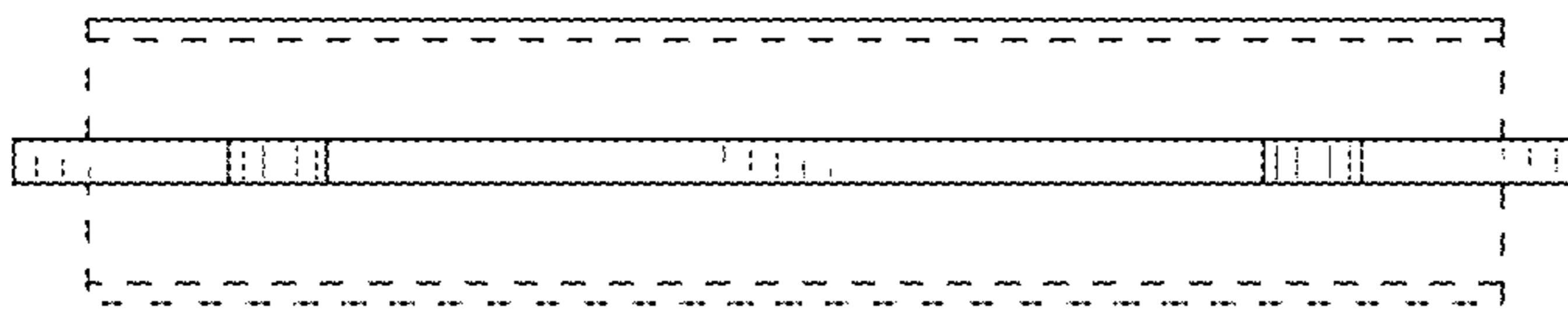


Fig. 6

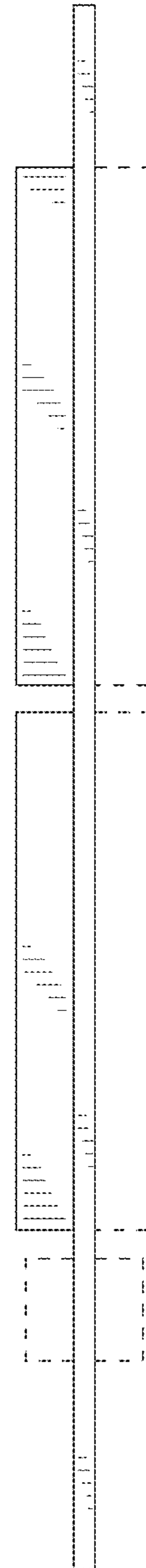


Fig. 7

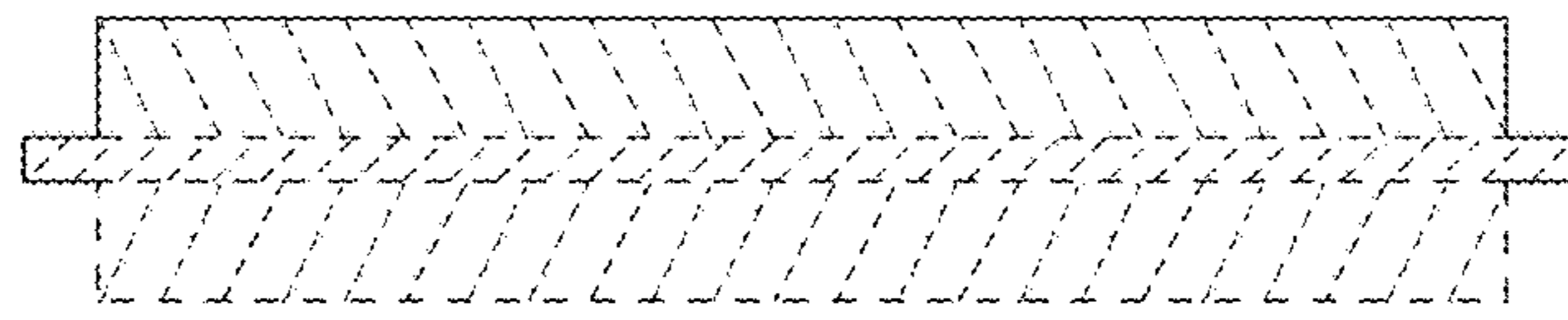


Fig. 8

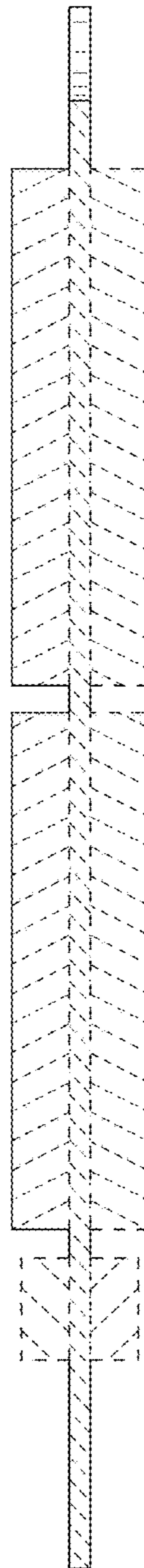


Fig. 9