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(12) **United States Design Patent** (10) **Patent No.:** **US D786,810 S**  
**Motoyama et al.** (45) **Date of Patent:** **\*\* May 16, 2017**

(54) **DUMMY WAFER** 4,244,761 A \* 1/1981 Remi ..... F27D 1/0009  
156/325  
(71) Applicant: **Tokyo Electron Limited**, Tokyo (JP) 4,374,906 A 2/1983 Breault et al.  
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(\*\*) Term: **14 Years**

(21) Appl. No.: **29/524,912**

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(30) **Foreign Application Priority Data**

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(51) **LOC (10) Cl.** ..... **13-03**

(52) **U.S. Cl.**  
USPC ..... **D13/182**

(58) **Field of Classification Search**  
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CPC ... C23C 16/26; C23C 30/005; C23C 14/0641;  
B82Y 30/00; C04B 41/52; C04B 41/89;  
C04B 41/009; C04B 35/803; B32B 27/36;  
B32B 27/08; B32B 27/32; B32B 7/02;  
B32B 9/00; B32B 18/00; G11B 5/716;  
B60R 21/2644; A61F 2/30767; A61F  
2/3094; A61F 2002/3098

See application file for complete search history.

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(57) **CLAIM**

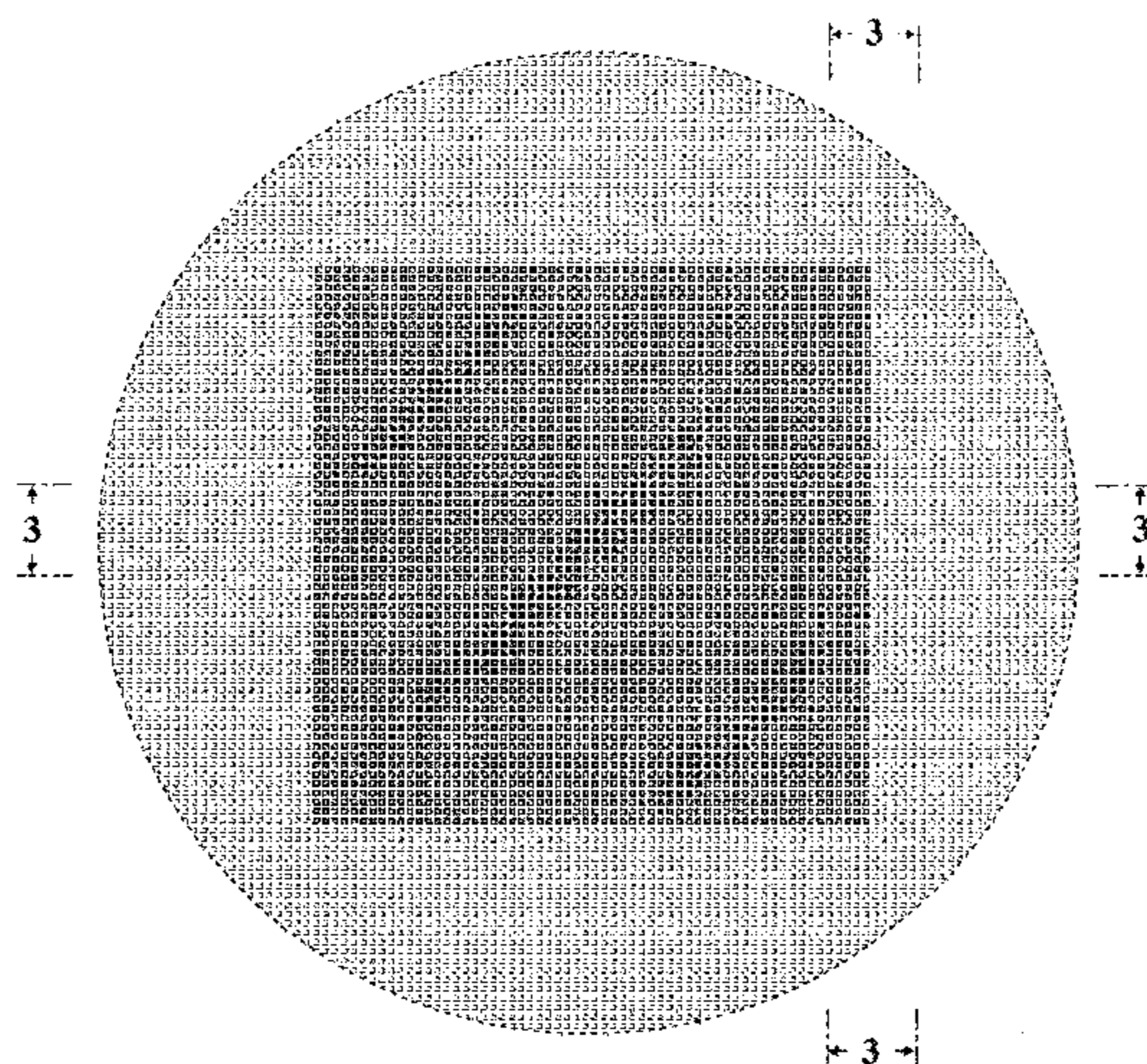
The ornamental design for a dummy wafer, as shown and described.

**DESCRIPTION**

FIG. 1 is a top plan view of a dummy wafer showing our new design;  
FIG. 2 is a front view thereof;  
FIG. 3 is an enlarged portion view taken along lines 3-3 in FIG. 1;  
FIG. 4 is a cross-sectional view taken along line 4-4 in FIG. 3; and,  
FIG. 5 is a cross-sectional view taken along line 5-5 in FIG. 3.

The broken lines shown in the drawings represent portions of the dummy wafer that form no part of the claimed design. Right, left and back views of the dummy wafer shown in FIG. 1 have been omitted because they are the same as the front view. The bottom view of the dummy wafer shown in FIG. 1 has been omitted because it forms no part of the claimed design.

**1 Claim, 2 Drawing Sheets**



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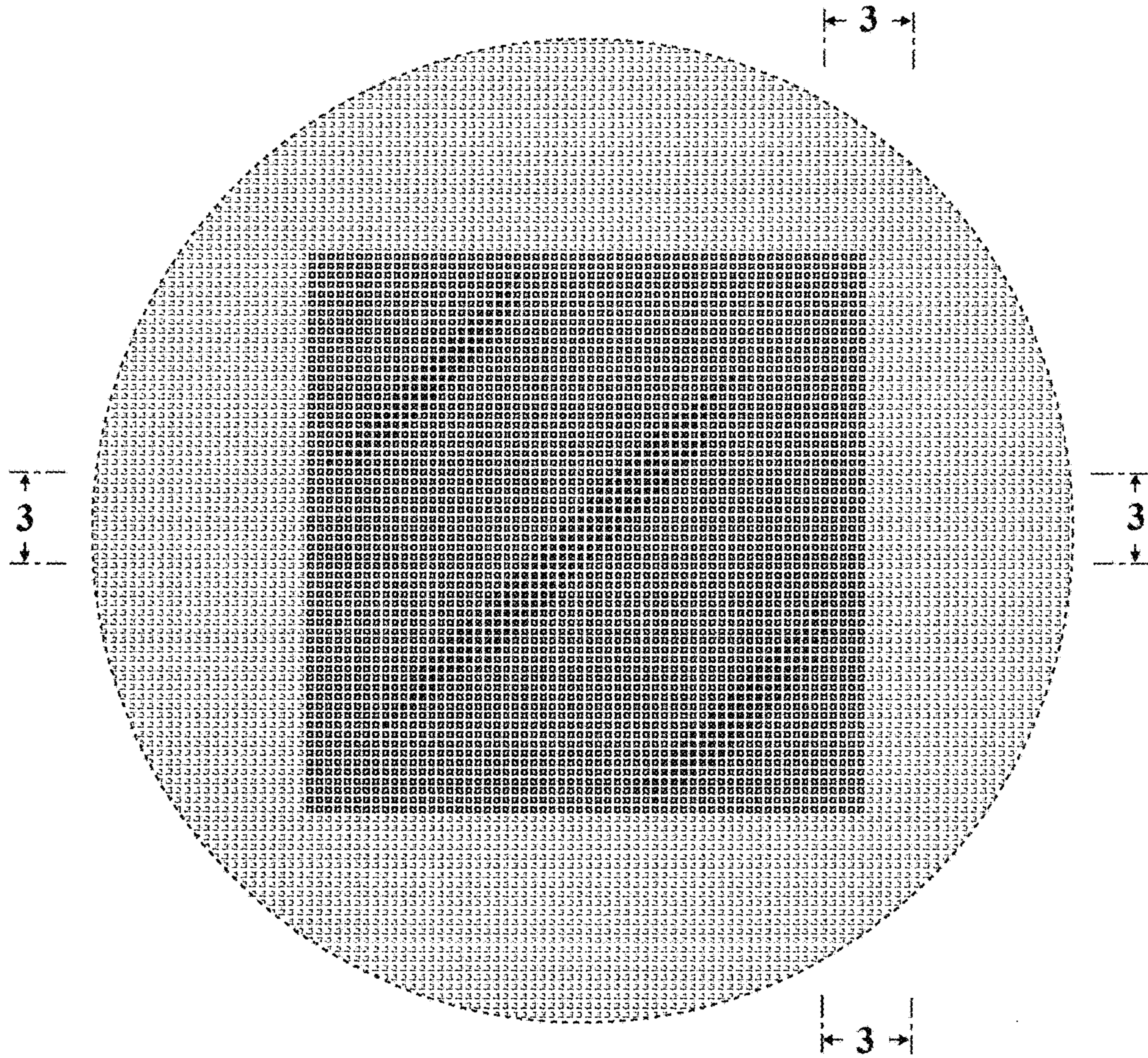
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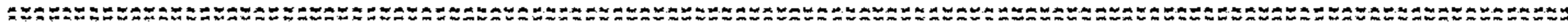
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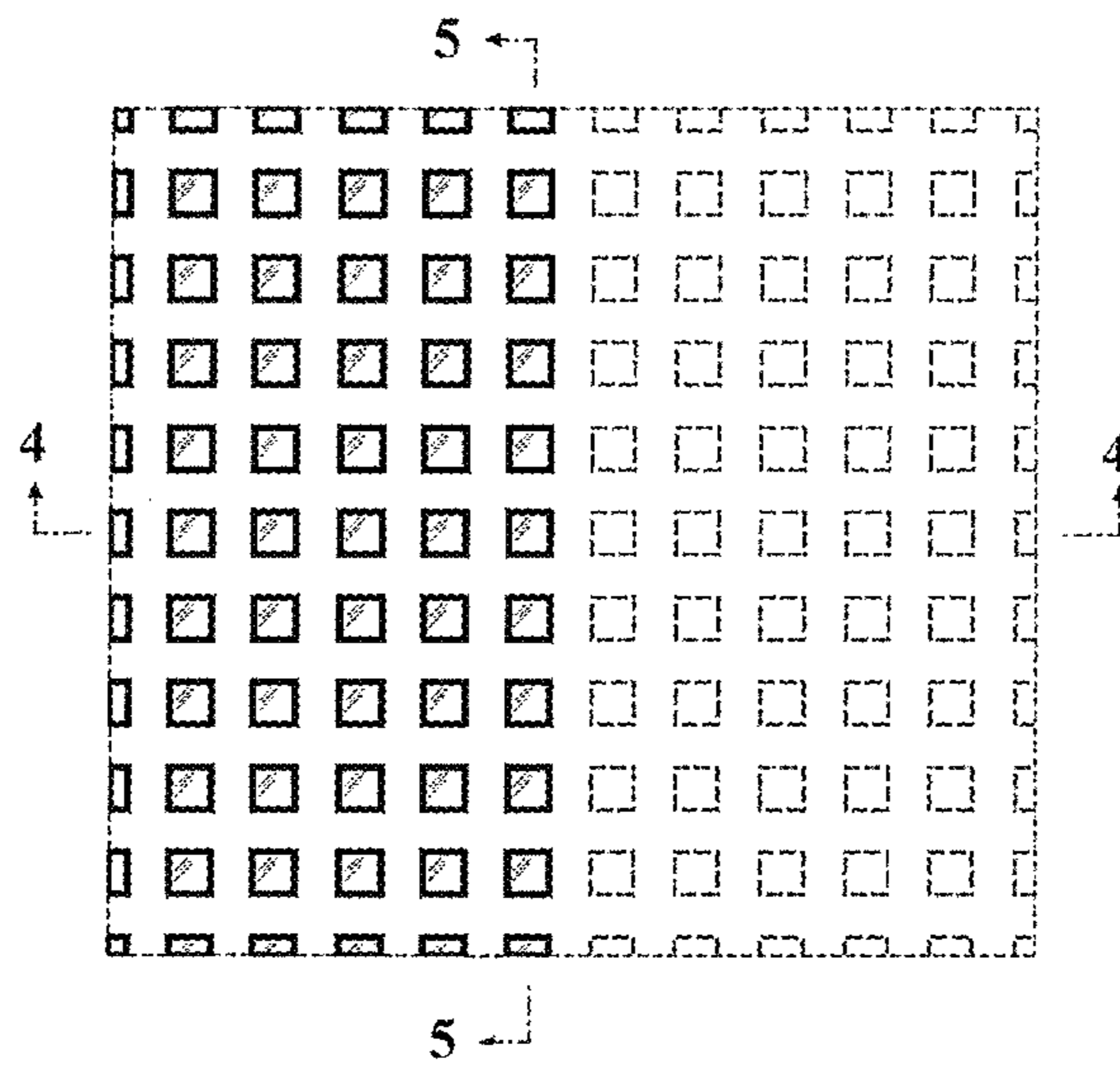
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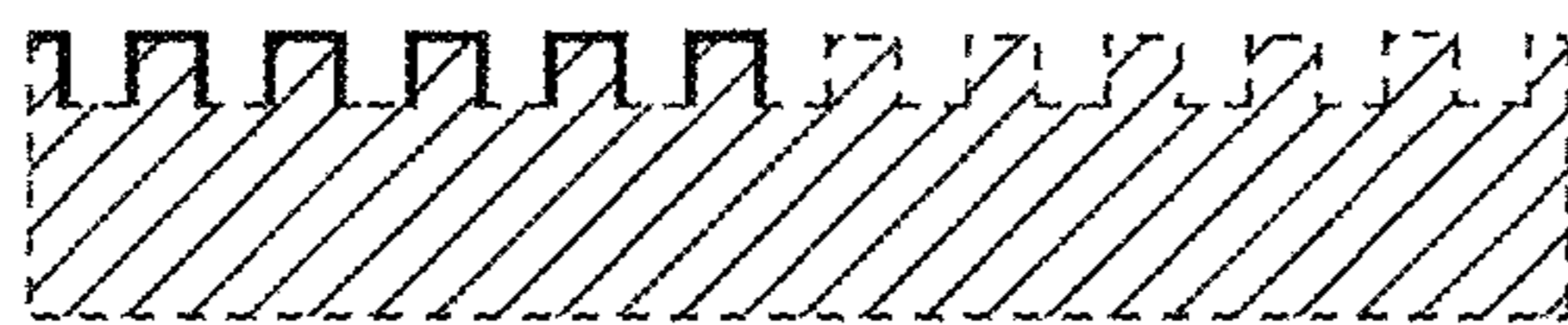
*Fig. 1*



*Fig. 2*



*Fig. 3*



*Fig. 4*



*Fig. 5*