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(12) **United States Design Patent**
Yoneyama et al.

(10) **Patent No.:** **US D783,549 S**

(45) **Date of Patent:** **** Apr. 11, 2017**

(54) **SEMICONDUCTOR DEVICE**

(56) **References Cited**

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Tokyo (JP)

U.S. PATENT DOCUMENTS

(72) Inventors: **Rei Yoneyama,** Tokyo (JP); **Takehiro Araki,** Fukuoka (JP); **Yoshitaka Kimura,** Tokyo (JP); **Akira Goto,** Fukuoka (JP); **Akihiko Yamashita,** Hyogo (JP); **Mariko Ono,** Fukuoka (JP); **Ryo Goto,** Tokyo (JP)

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(**) Term: **15 Years**

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PC

(21) Appl. No.: **29/530,661**

(57) **CLAIM**

The ornamental design for a semiconductor device, as shown and described.

(22) Filed: **Jun. 18, 2015**

DESCRIPTION

(30) **Foreign Application Priority Data**

Feb. 4, 2015 (JP) 2015-002064

(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/133, 147, 154, 182, 184, 199
CPC ... H01L 21/50; H01L 23/04; H01L 23/49844;
H01L 25/18; H01L 25/50; H01L 27/144;
H01L 29/1068; H01L 29/2003

FIG. 1 is a front, top and right side perspective view of a semiconductor device, showing our new design;
FIG. 2 is a front view thereof;
FIG. 3 is a rear view thereof;
FIG. 4 is a left side view thereof;
FIG. 5 is a right side view thereof;
FIG. 6 is a top view thereof; and,
FIG. 7 is a bottom view thereof.

The broken line in the figure drawings is included for the purpose of illustrating environment and forms no part of the claimed design.

See application file for complete search history.

1 Claim, 7 Drawing Sheets

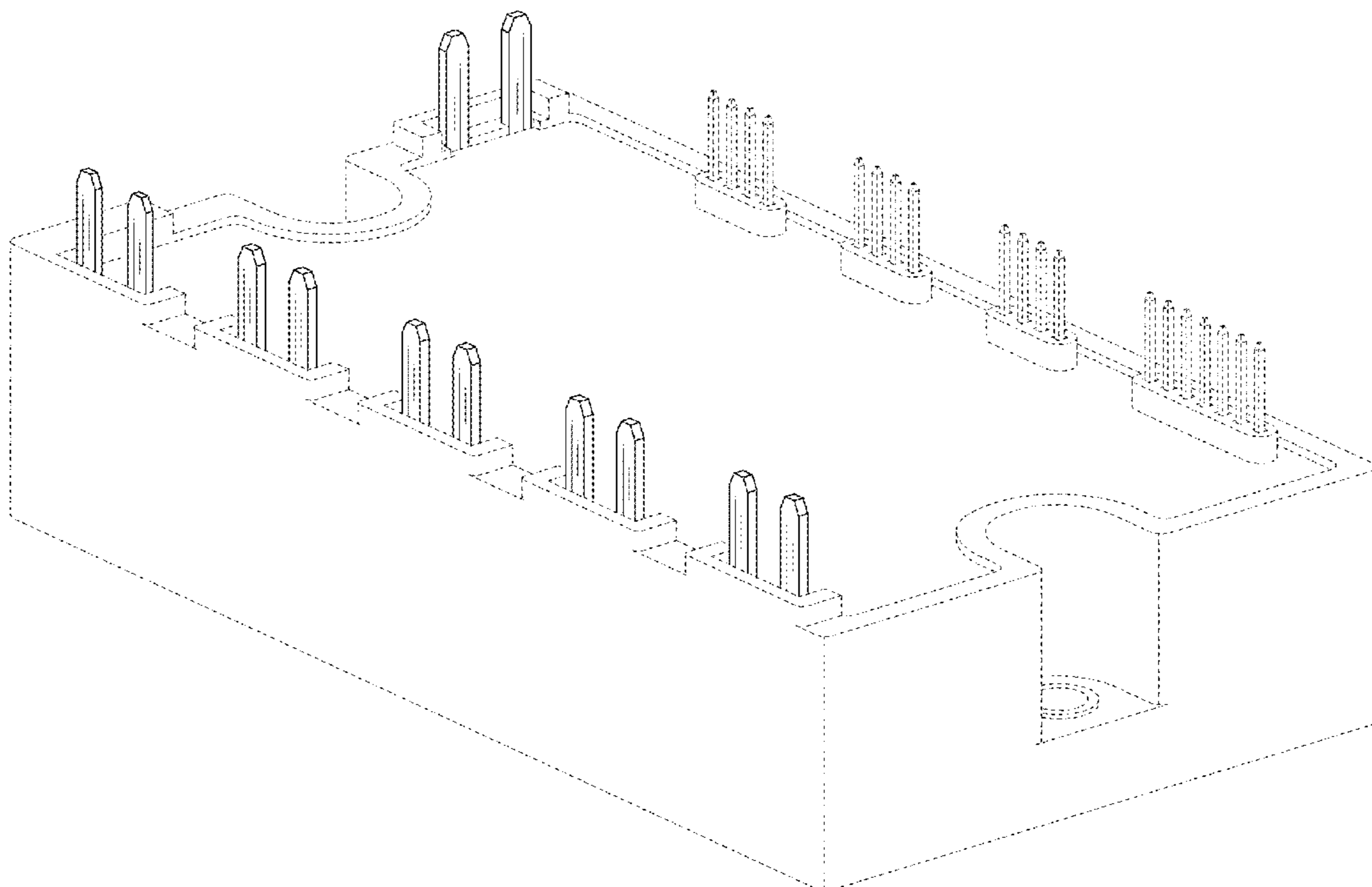


Fig. 1

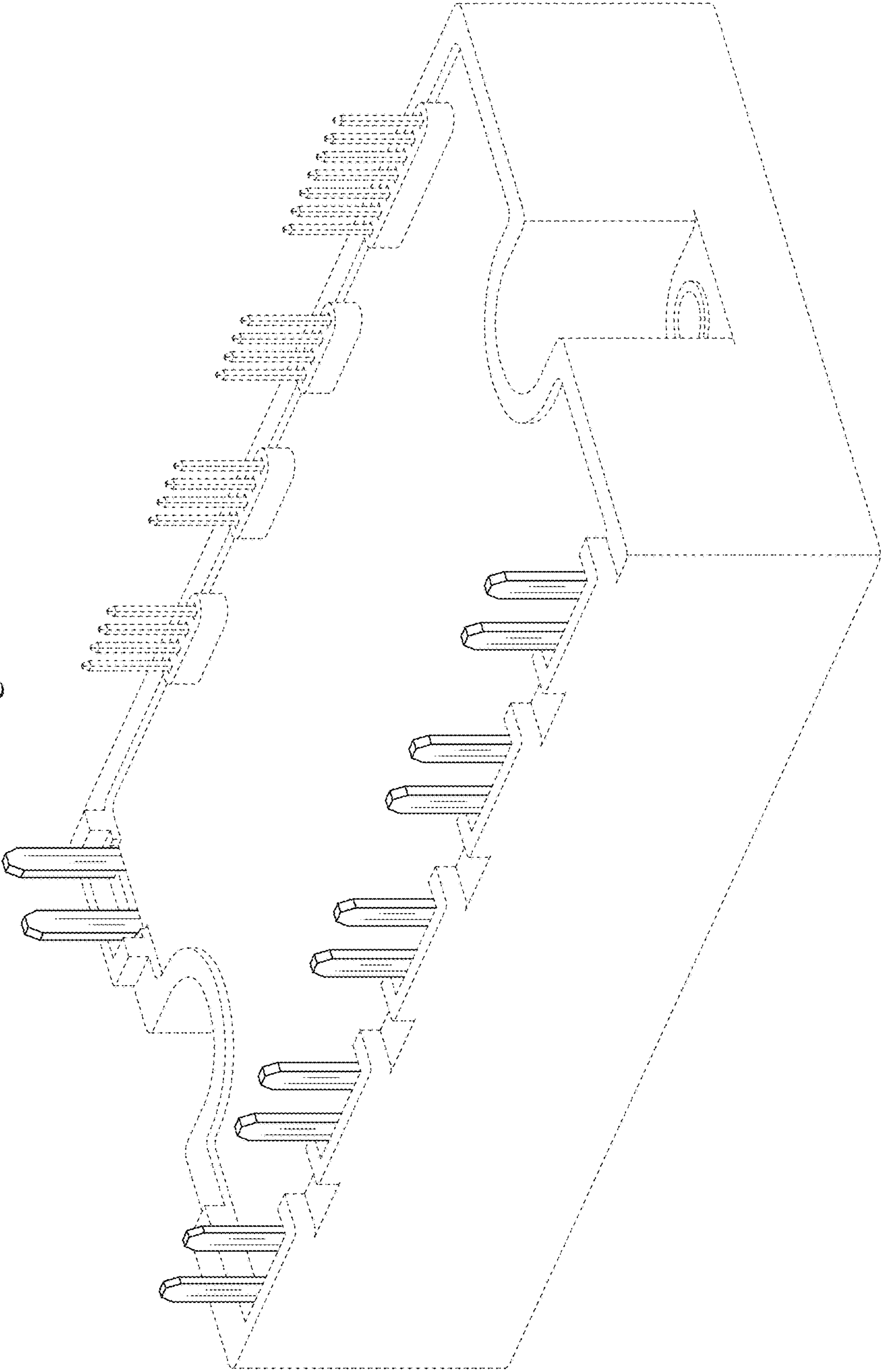


Fig. 2

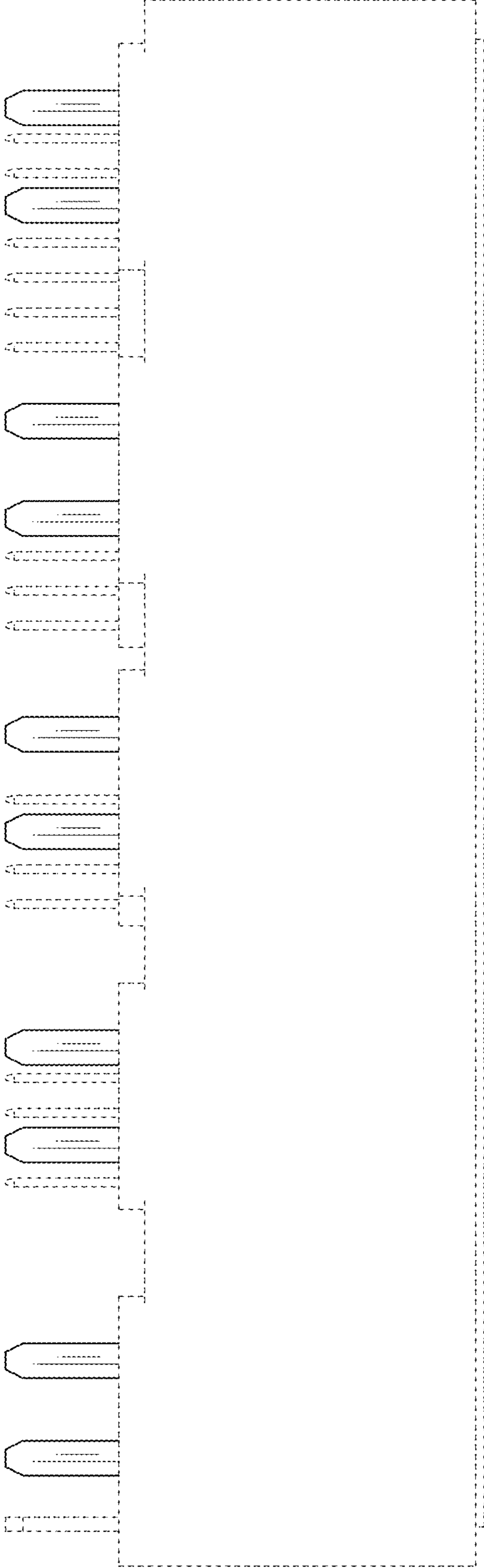


Fig. 3

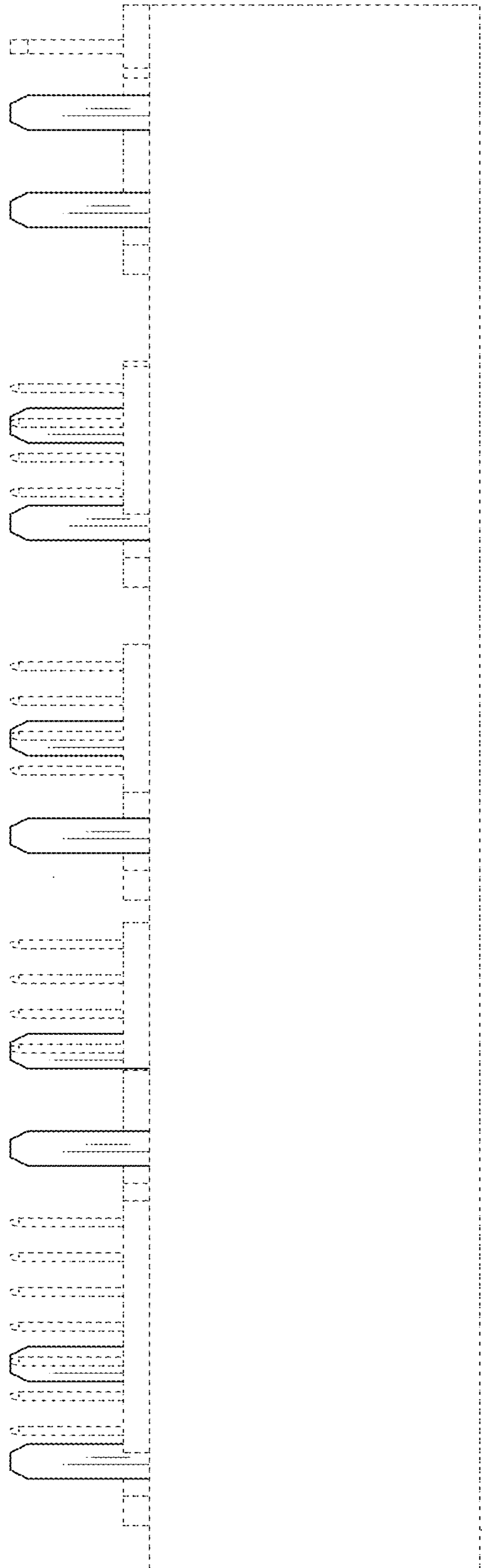


Fig. 4

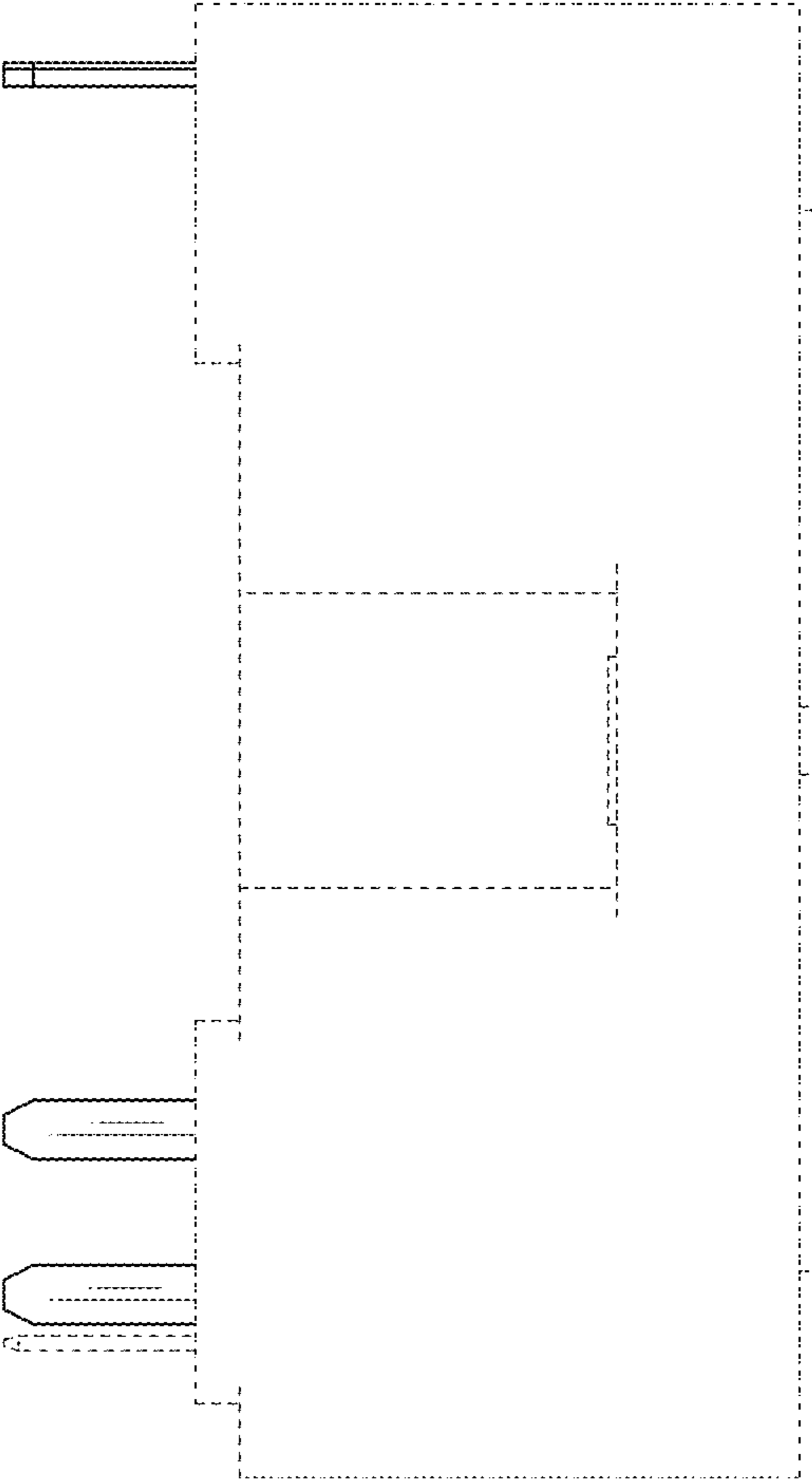


Fig. 5

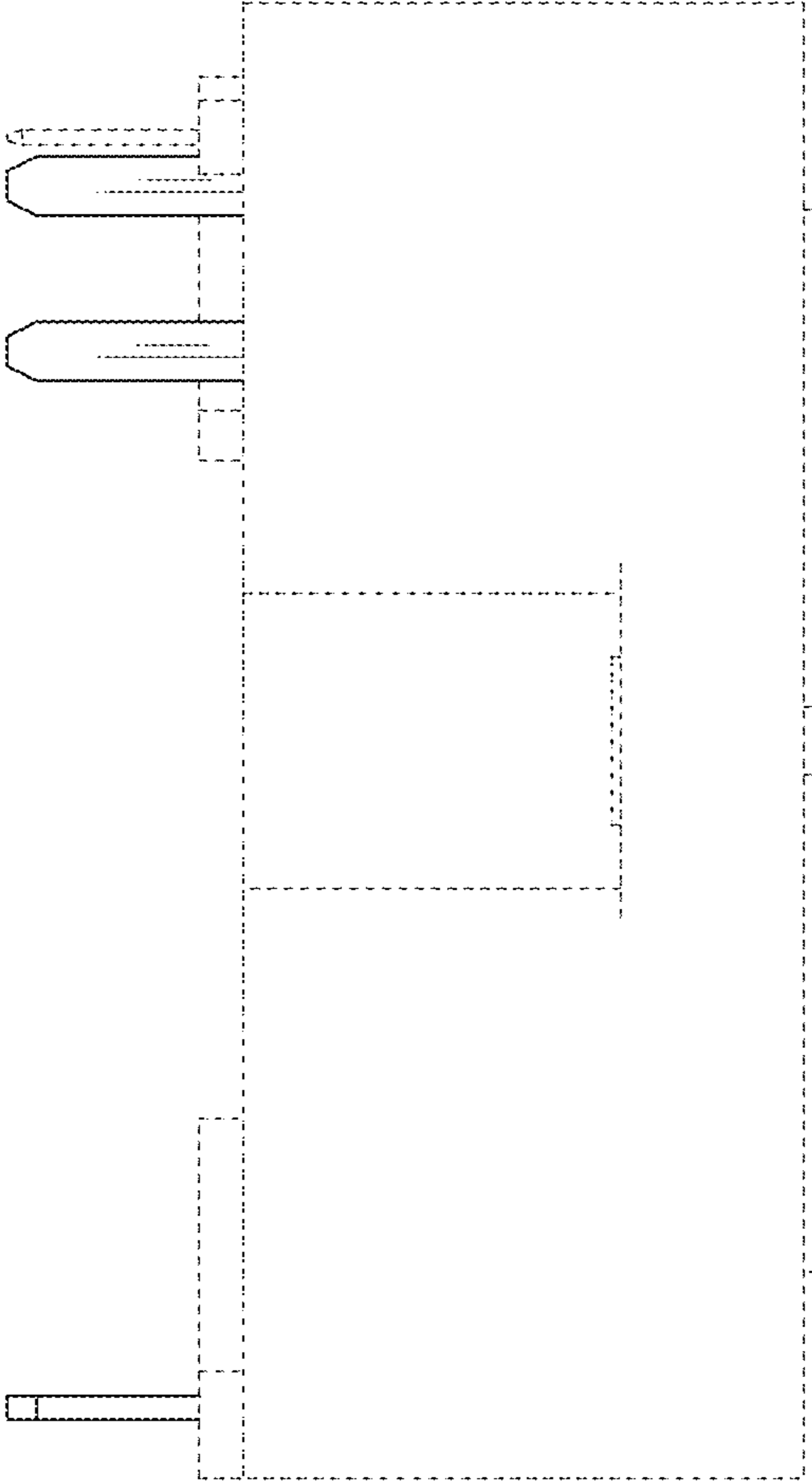


Fig. 6

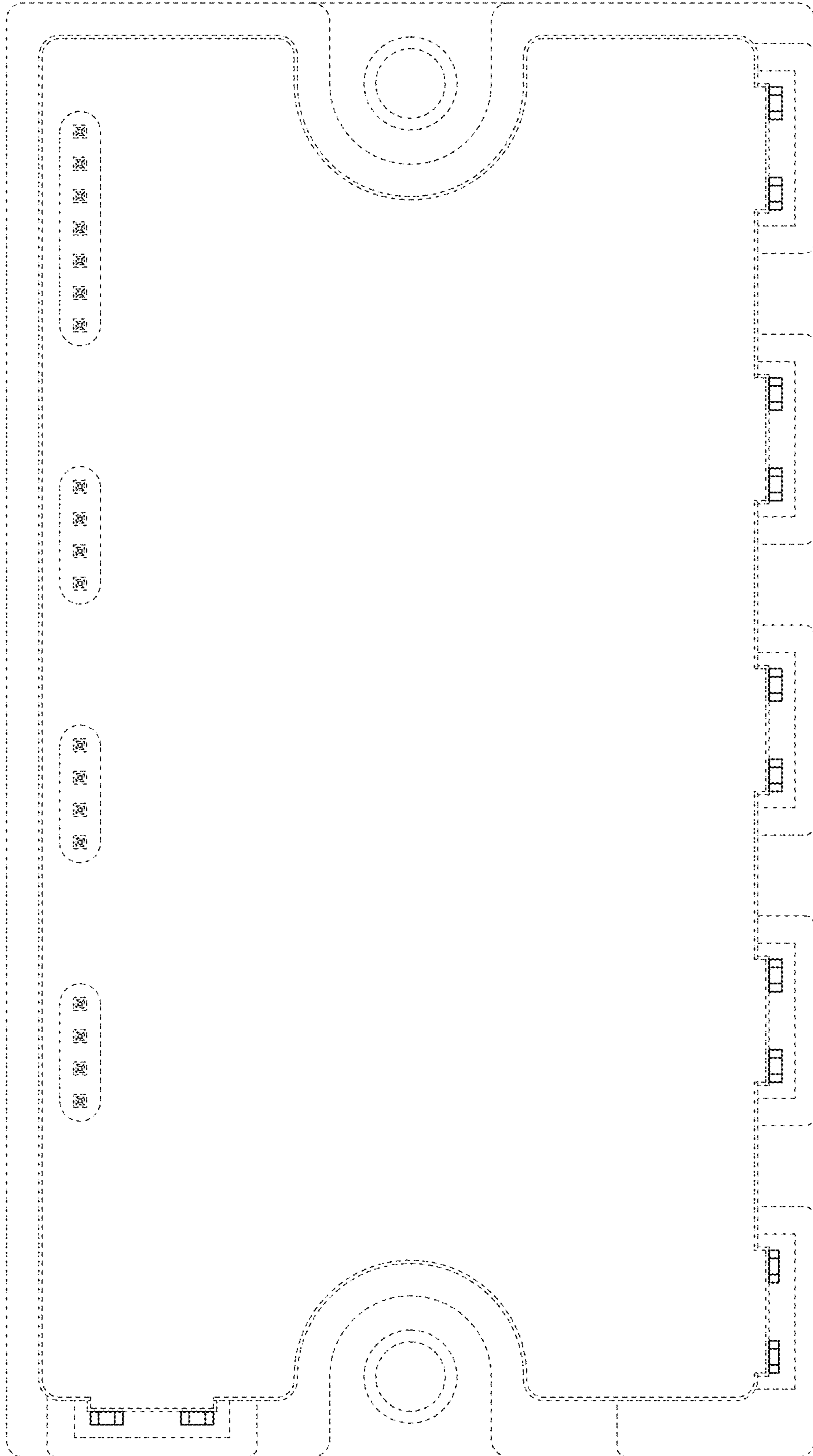


Fig. 7

