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(12) **United States Design Patent**
Waterfall et al.

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(45) **Date of Patent:** **** Mar. 7, 2017**

(54) **ELECTRONICS BOX**

(71) Applicant: **Verizon Patent and Licensing Inc.**,
Arlington, VA (US)

(72) Inventors: **Simon Waterfall**, San Francisco, CA
(US); **Suri B. Medapati**, San Jose, CA
(US); **Gregory A. James**, Phoenix, AZ
(US); **Brian G. Heintz**, White Salmon,
WA (US); **Ricardo Penate**, Pacifica,
CA (US); **Gadi Amit**, San Mateo, CA
(US); **Susan Mckinney**, San Francisco,
CA (US); **Jinwoo Kim**, San Francisco,
CA (US); **Byron Ben-Ming Hsieh**, San
Francisco, CA (US)

(73) Assignee: **Verizon Patent and Licensing Inc.**,
Basking Ridge, NJ (US)

(**) Term: **15 Years**

(21) Appl. No.: **29/531,177**

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(51) **LOC (10) Cl.** **14-03**

(52) **U.S. Cl.**
USPC **D14/125**

(58) **Field of Classification Search**
USPC D14/125, 357-358, 496, 188, 242, 432;
D13/184; 348/10, 460, 706, 731;
340/825.03; 455/6.1, 6.2; 312/223.1, 7.2
CPC H04N 5/50; H04N 5/64; H05K 5/02;
H05K 5/03; G06F 1/16
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

D284,005 S * 5/1986 Isaacs D14/251
D368,265 S * 3/1996 Fan D14/256
D577,710 S * 9/2008 Joseph D14/204
D642,121 S * 7/2011 Lee D13/108

D642,519 S * 8/2011 Woo D13/108
D666,145 S * 8/2012 Kim D13/108
D681,626 S * 5/2013 Zehner D14/253
D712,369 S * 9/2014 Yoshida D14/142
D714,788 S * 10/2014 Haller D14/434
D718,724 S * 12/2014 Clymer D13/168

(Continued)

Primary Examiner — Randall Gholson

(57) **CLAIM**

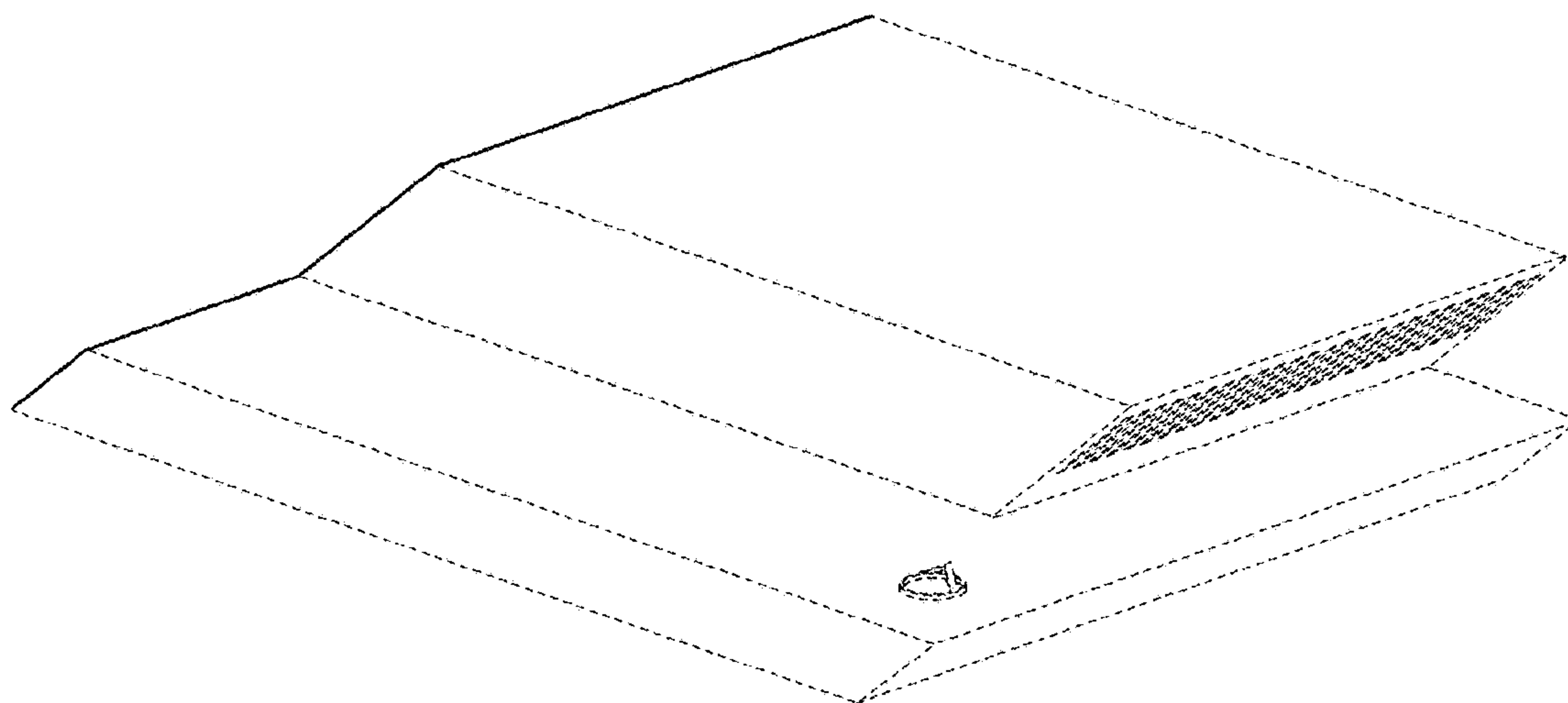
The ornamental design for an electronics box, as shown and described.

DESCRIPTION

FIG. 1 is a top isometric view of an exemplary representation of our new design;
FIG. 2 is another top isometric view of the exemplary representation thereof;
FIG. 3 is another top isometric view of the exemplary representation thereof;
FIG. 4 is another top isometric view of the exemplary representation thereof;
FIG. 5 is a bottom isometric view of the exemplary representation thereof;
FIG. 6 is another bottom isometric view of the exemplary representation thereof;
FIG. 7 is a front view of the exemplary representation thereof;
FIG. 8 is a back view of the exemplary representation thereof;
FIG. 9 is a top view of the exemplary representation thereof;
FIG. 10 is a bottom view of the exemplary representation thereof;
FIG. 11 is a first side view of the exemplary representation thereof; and,
FIG. 12 is a second side view of the exemplary representation thereof.

The broken lines depict portions of the electronics box that form no part of the claimed design.

1 Claim, 7 Drawing Sheets



(56)

References Cited

U.S. PATENT DOCUMENTS

D723,503 S * 3/2015 Jeon D14/130
D730,306 S * 5/2015 Tang D14/125
D747,763 S * 1/2016 Haller D18/4.5

* cited by examiner

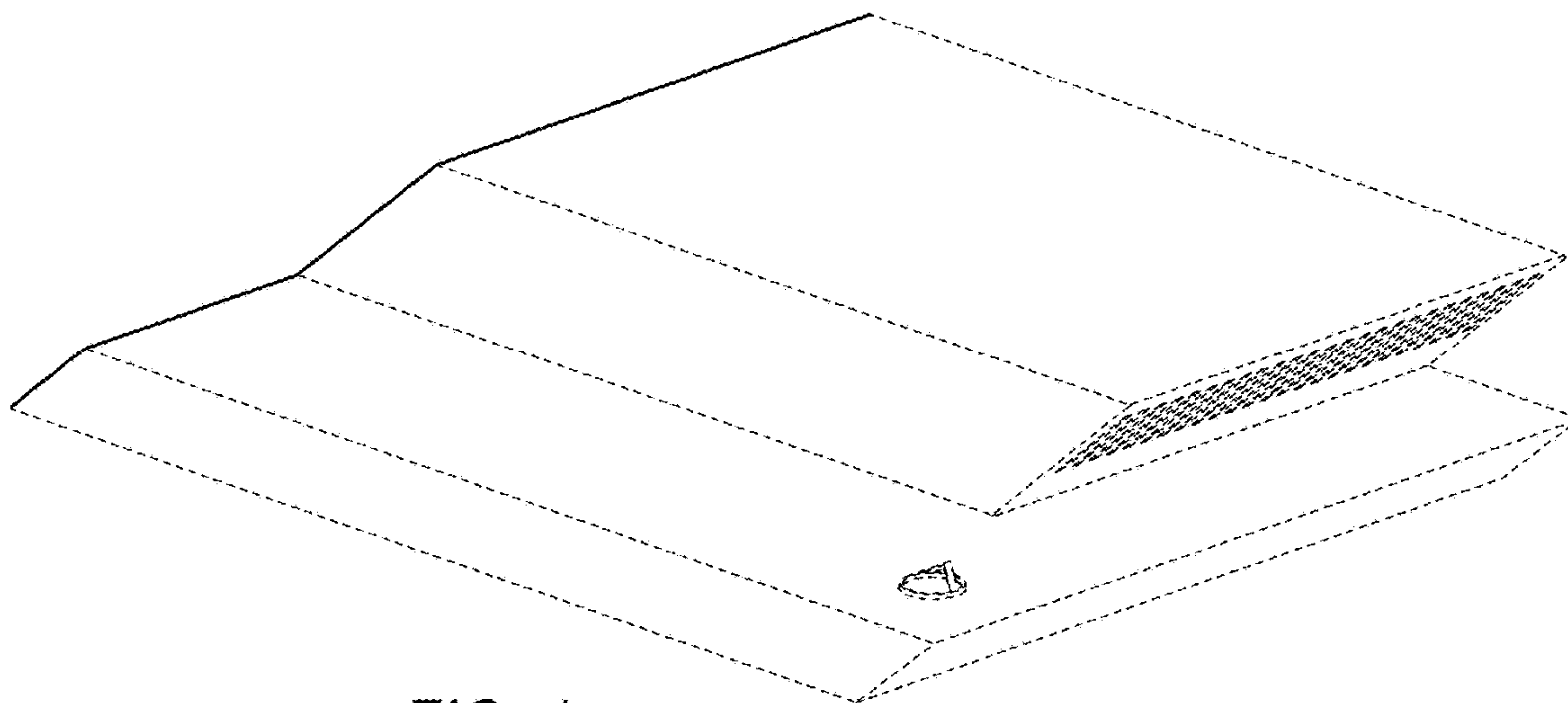


FIG. 1

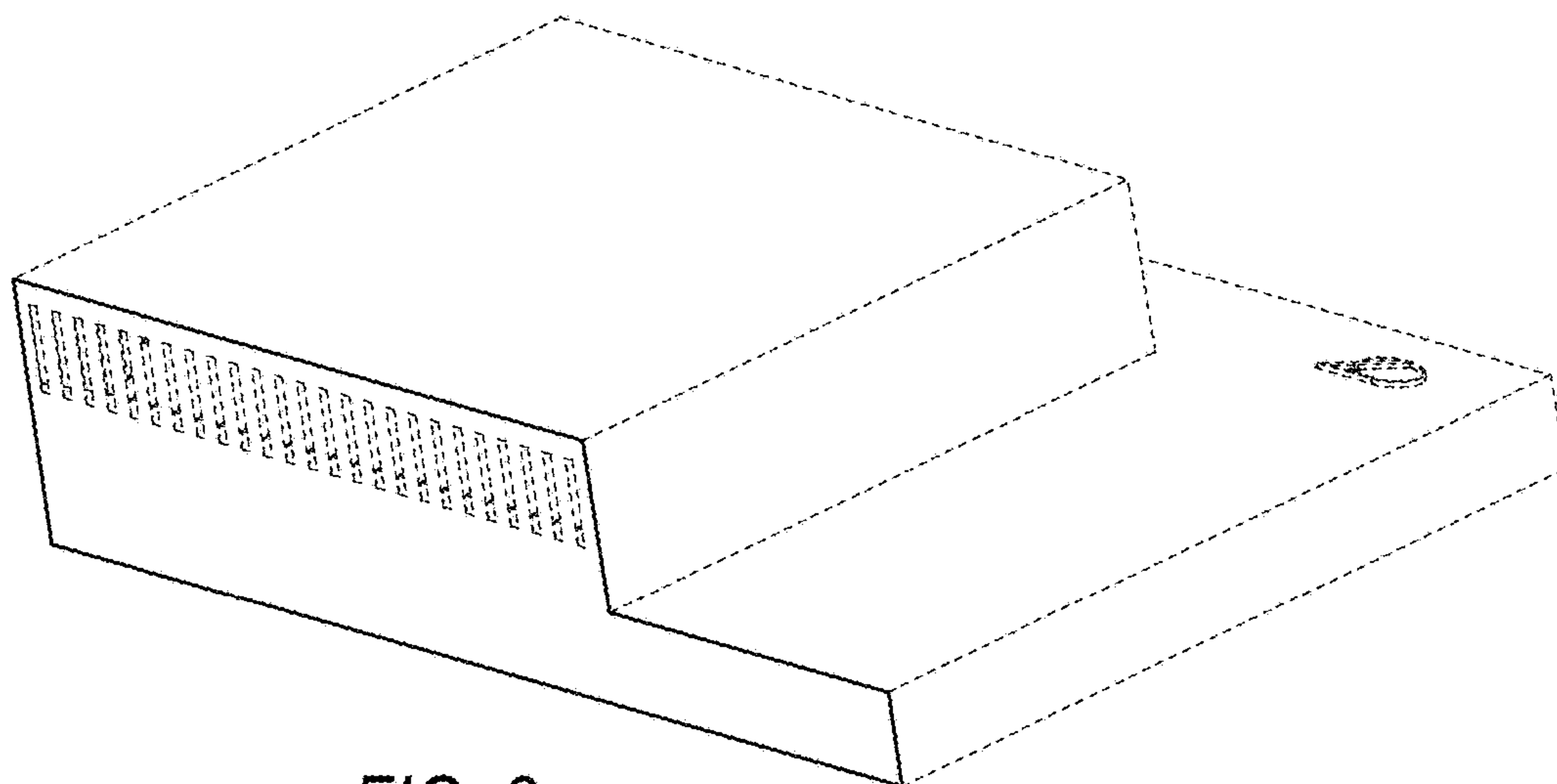


FIG. 2

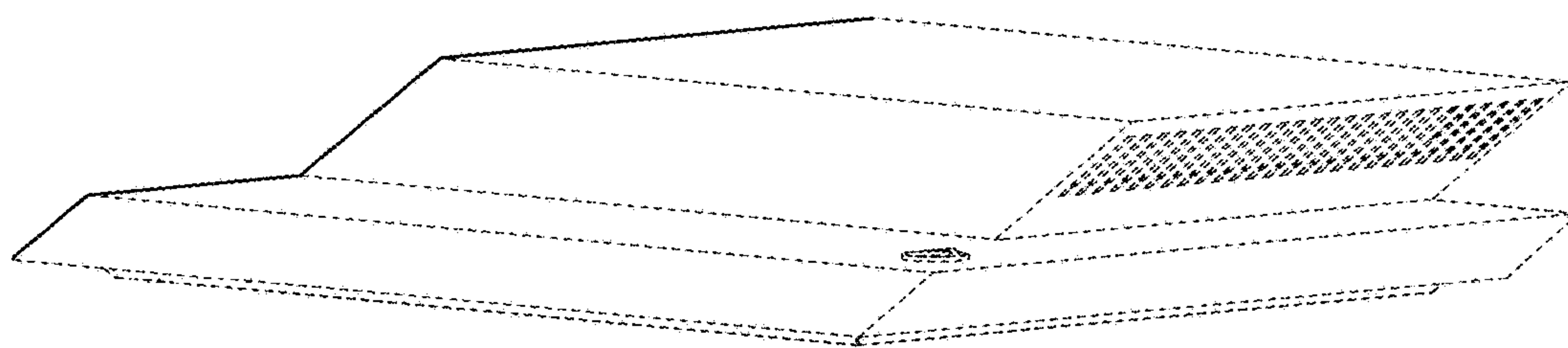
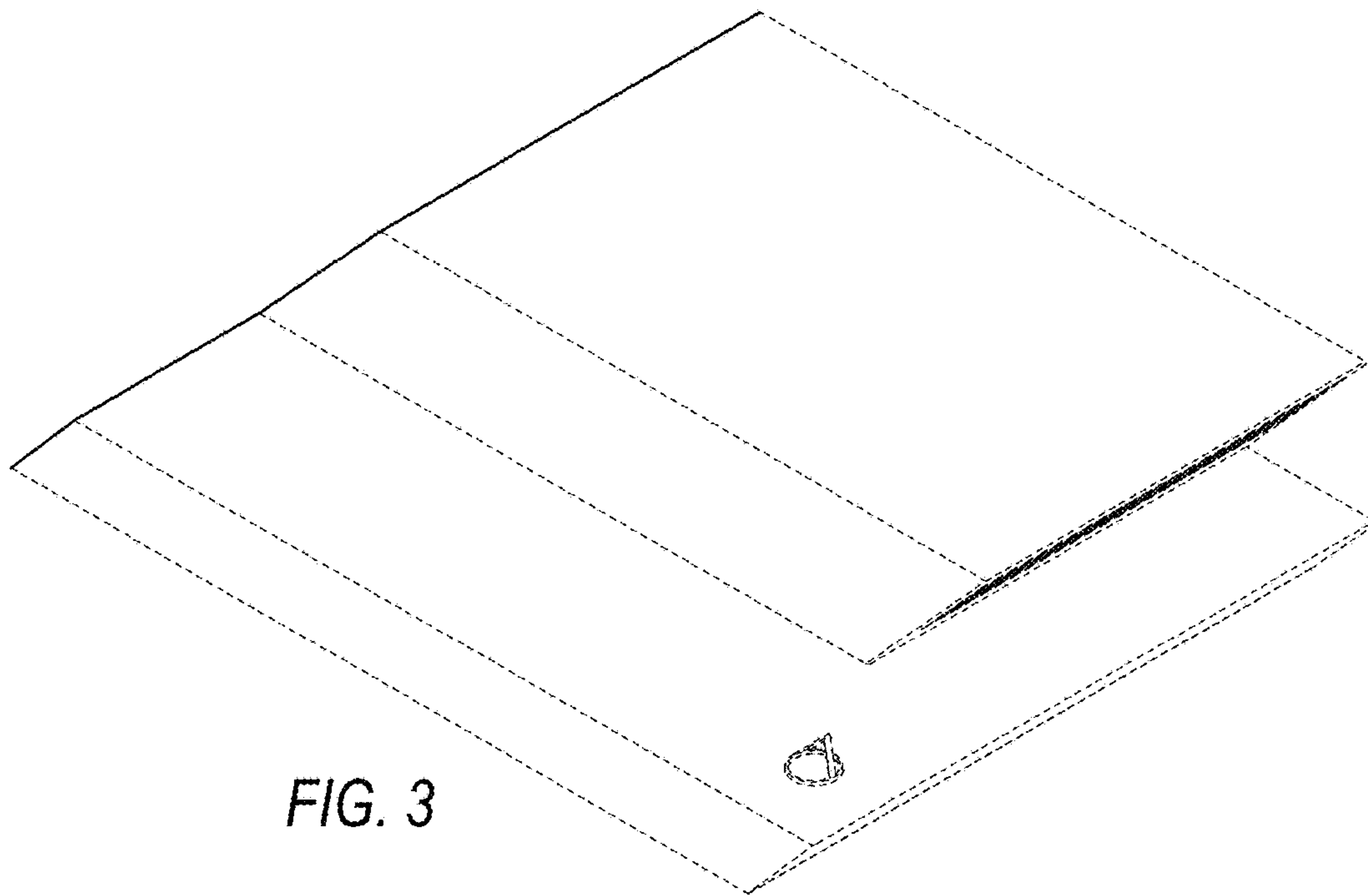


FIG. 4

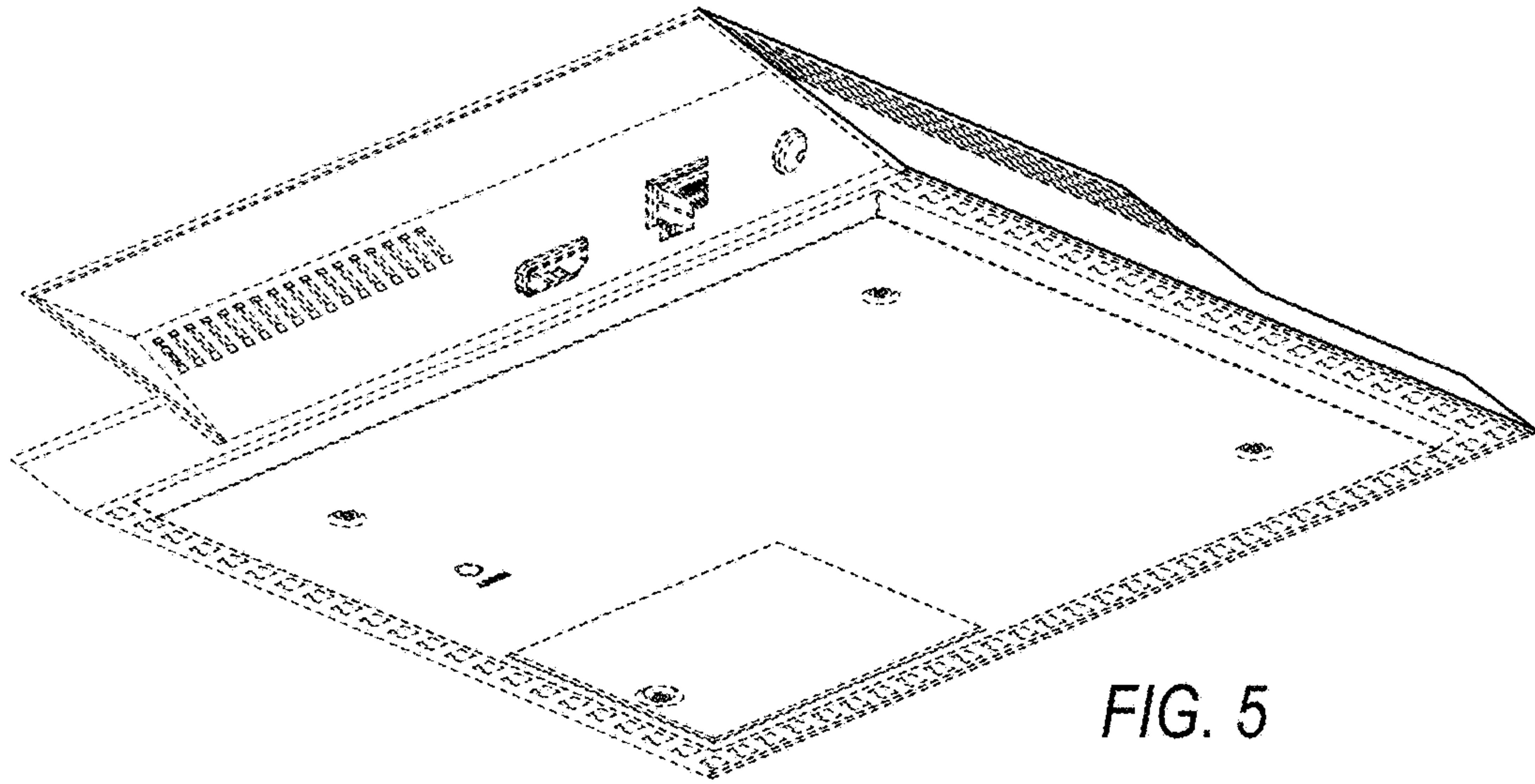


FIG. 5

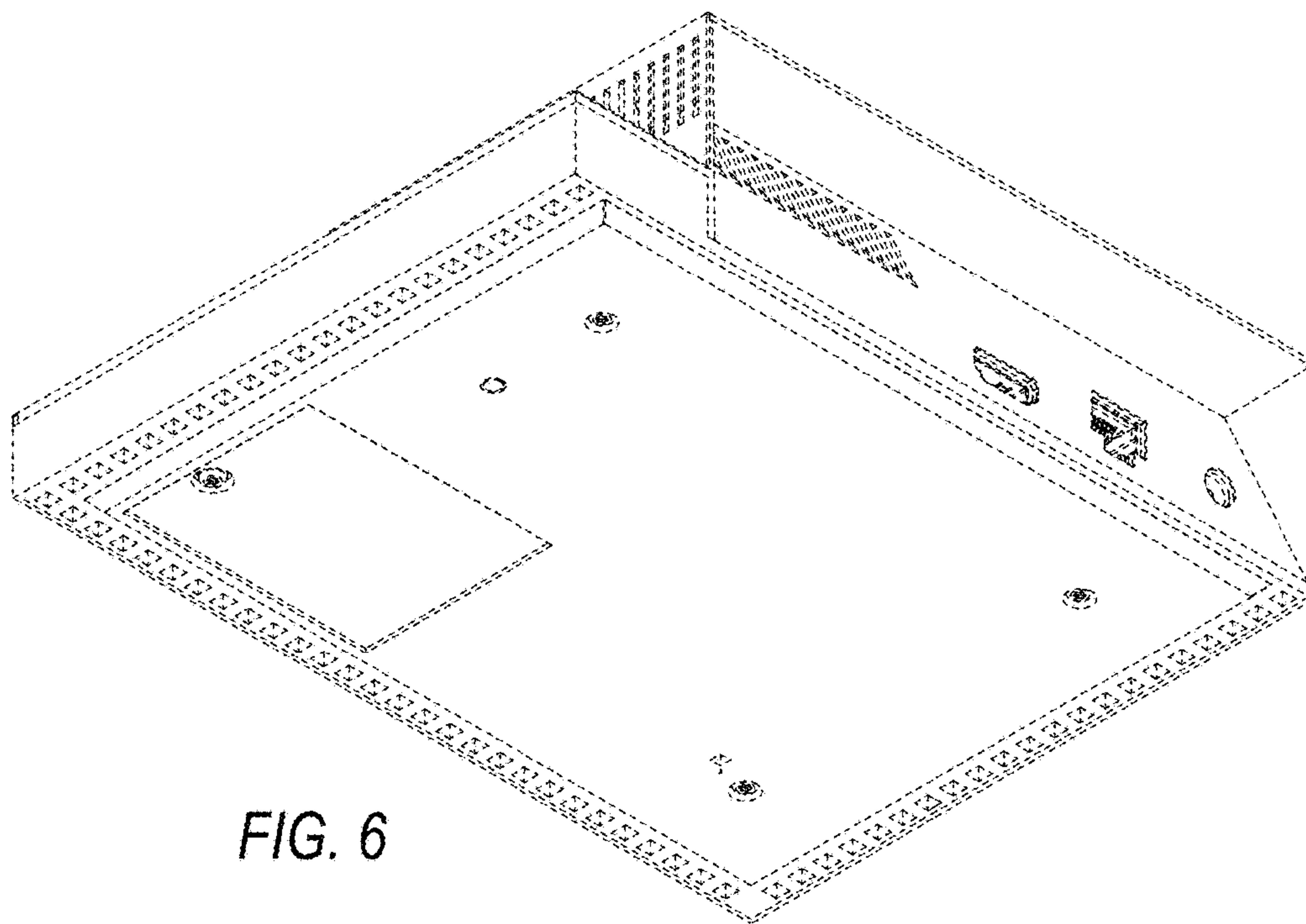


FIG. 6

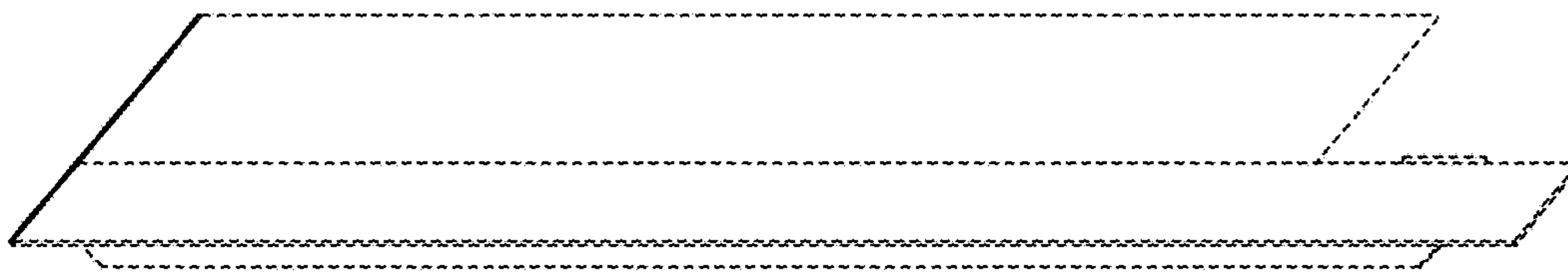


FIG. 7

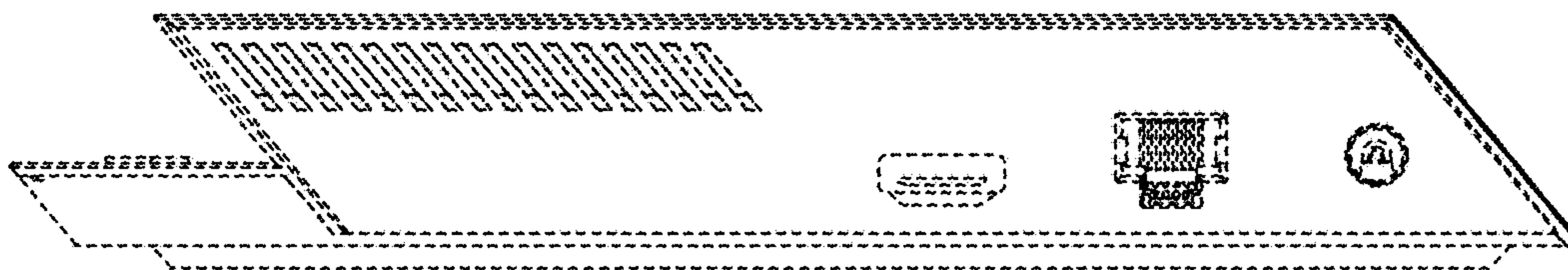


FIG. 8

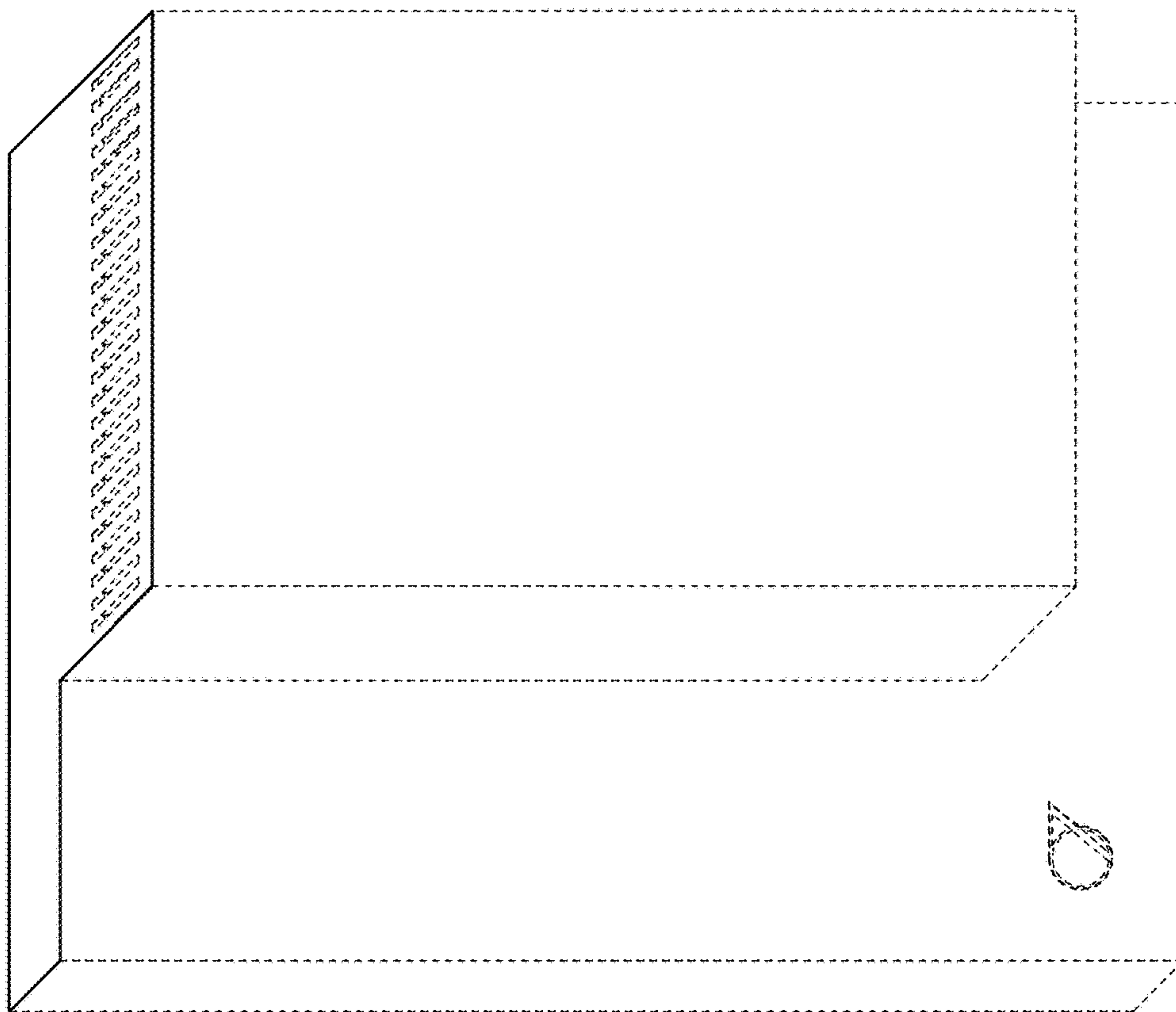


FIG. 9

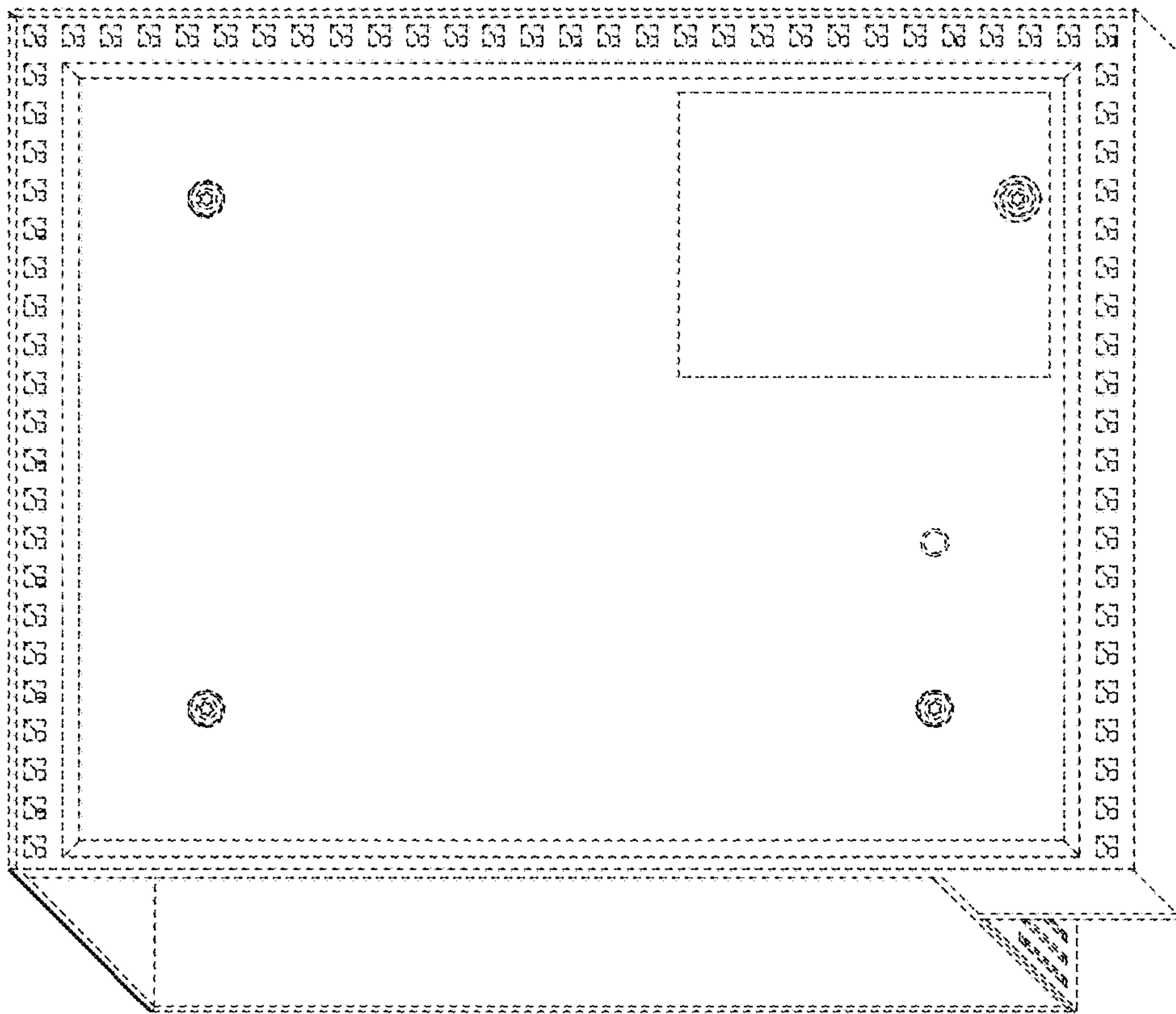


FIG. 10

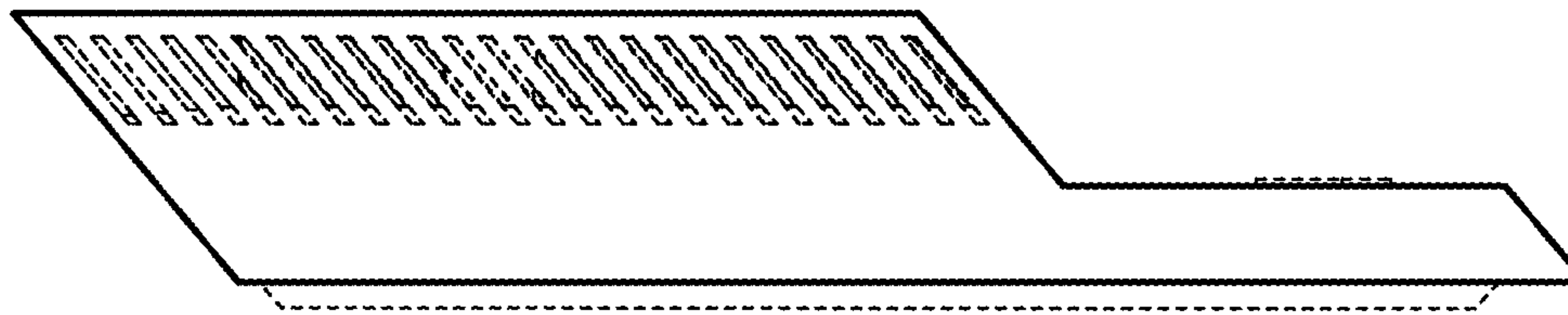


FIG. 11

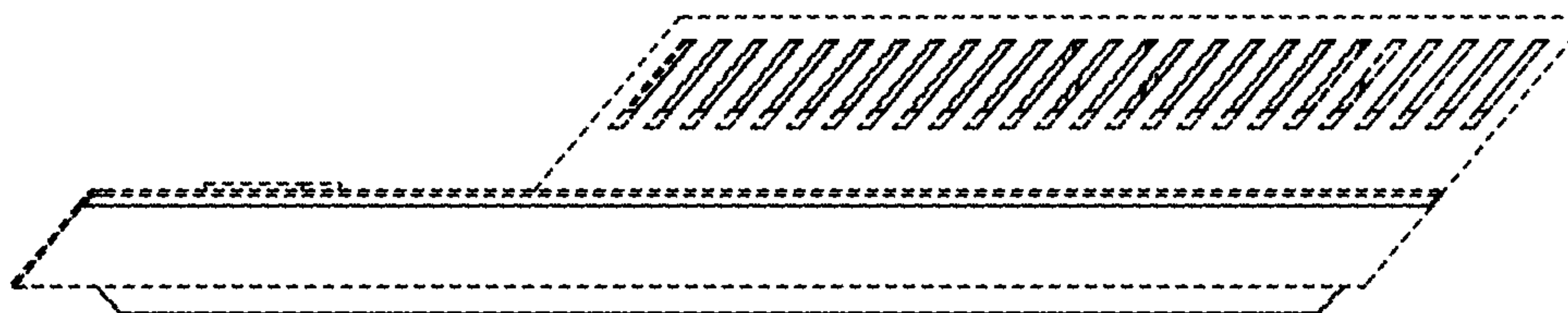


FIG. 12