



US00D780705S

(12) **United States Design Patent**
Waterfall et al.

(10) **Patent No.:** **US D780,705 S**

(45) **Date of Patent:** **** Mar. 7, 2017**

(54) **ELECTRONICS BOX**

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(**) Term: **15 Years**

(21) Appl. No.: **29/531,177**

(22) Filed: **Jun. 23, 2015**

(51) **LOC (10) Cl.** **14-03**

(52) **U.S. Cl.**
USPC **D14/125**

(58) **Field of Classification Search**
USPC D14/125, 357-358, 496, 188, 242, 432;
D13/184; 348/10, 460, 706, 731;
340/825.03; 455/6.1, 6.2; 312/223.1, 7.2
CPC H04N 5/50; H04N 5/64; H05K 5/02;
H05K 5/03; G06F 1/16
See application file for complete search history.

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Primary Examiner — Randall Gholson

(57) **CLAIM**

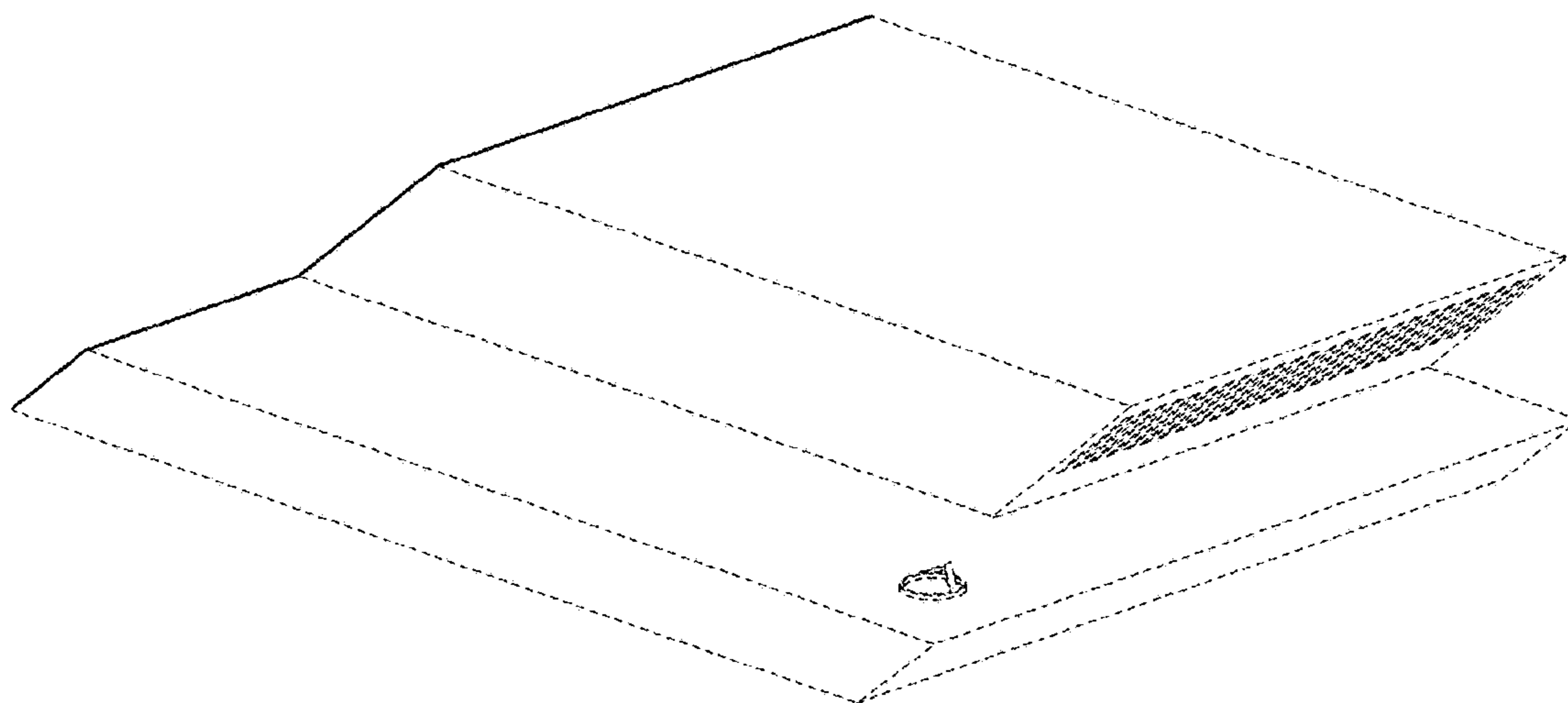
The ornamental design for an electronics box, as shown and described.

DESCRIPTION

FIG. 1 is a top isometric view of an exemplary representation of our new design;
FIG. 2 is another top isometric view of the exemplary representation thereof;
FIG. 3 is another top isometric view of the exemplary representation thereof;
FIG. 4 is another top isometric view of the exemplary representation thereof;
FIG. 5 is a bottom isometric view of the exemplary representation thereof;
FIG. 6 is another bottom isometric view of the exemplary representation thereof;
FIG. 7 is a front view of the exemplary representation thereof;
FIG. 8 is a back view of the exemplary representation thereof;
FIG. 9 is a top view of the exemplary representation thereof;
FIG. 10 is a bottom view of the exemplary representation thereof;
FIG. 11 is a first side view of the exemplary representation thereof; and,
FIG. 12 is a second side view of the exemplary representation thereof.

The broken lines depict portions of the electronics box that form no part of the claimed design.

1 Claim, 7 Drawing Sheets



(56)

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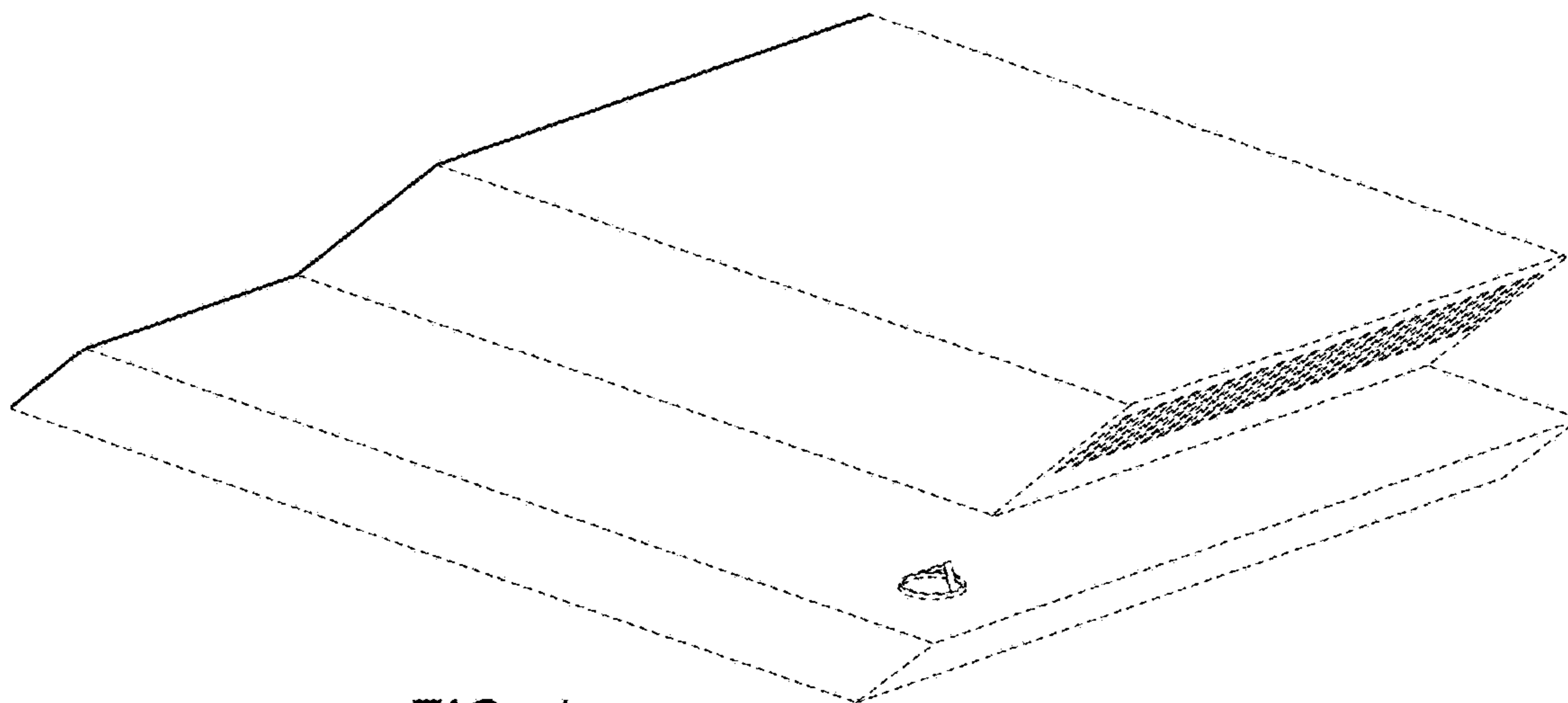


FIG. 1

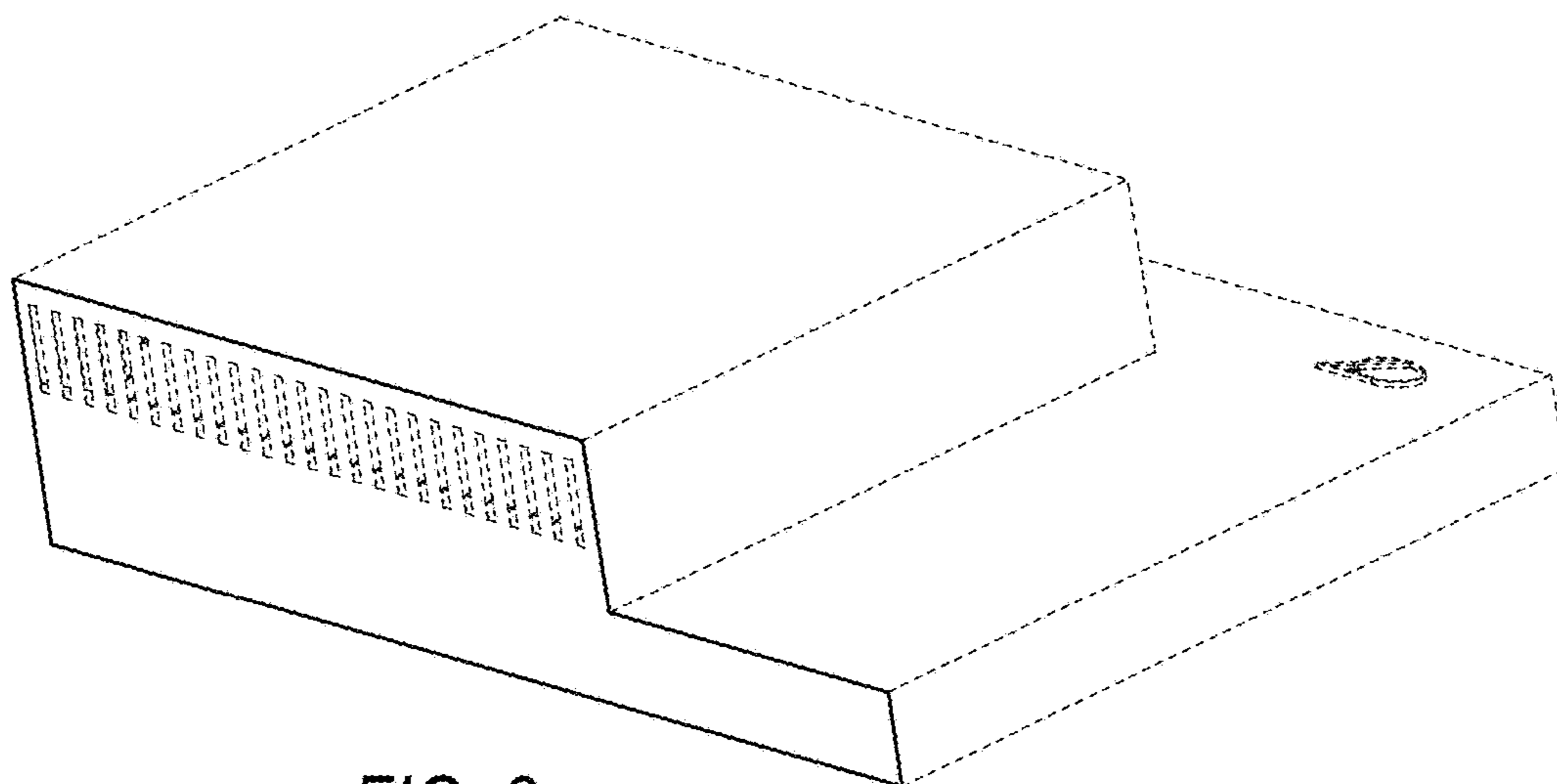


FIG. 2

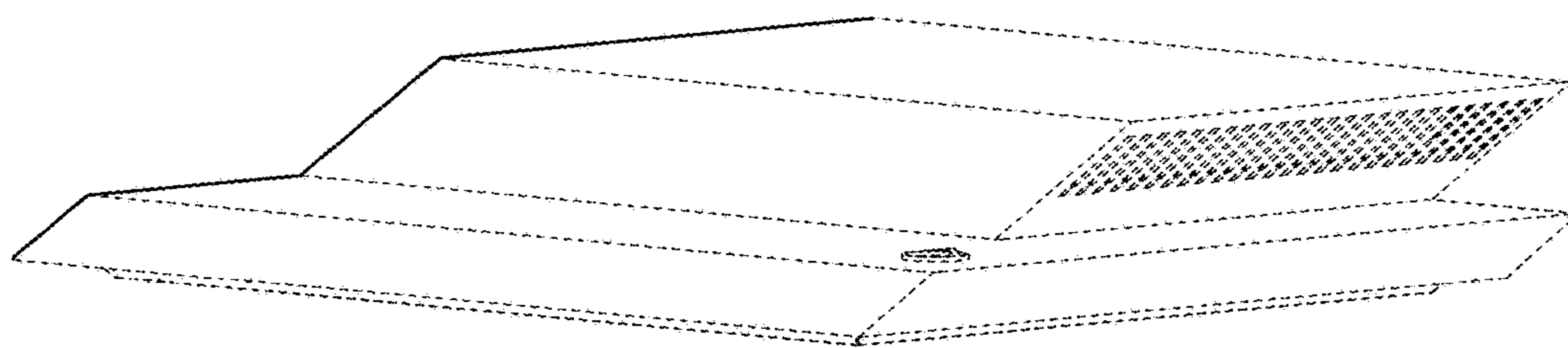
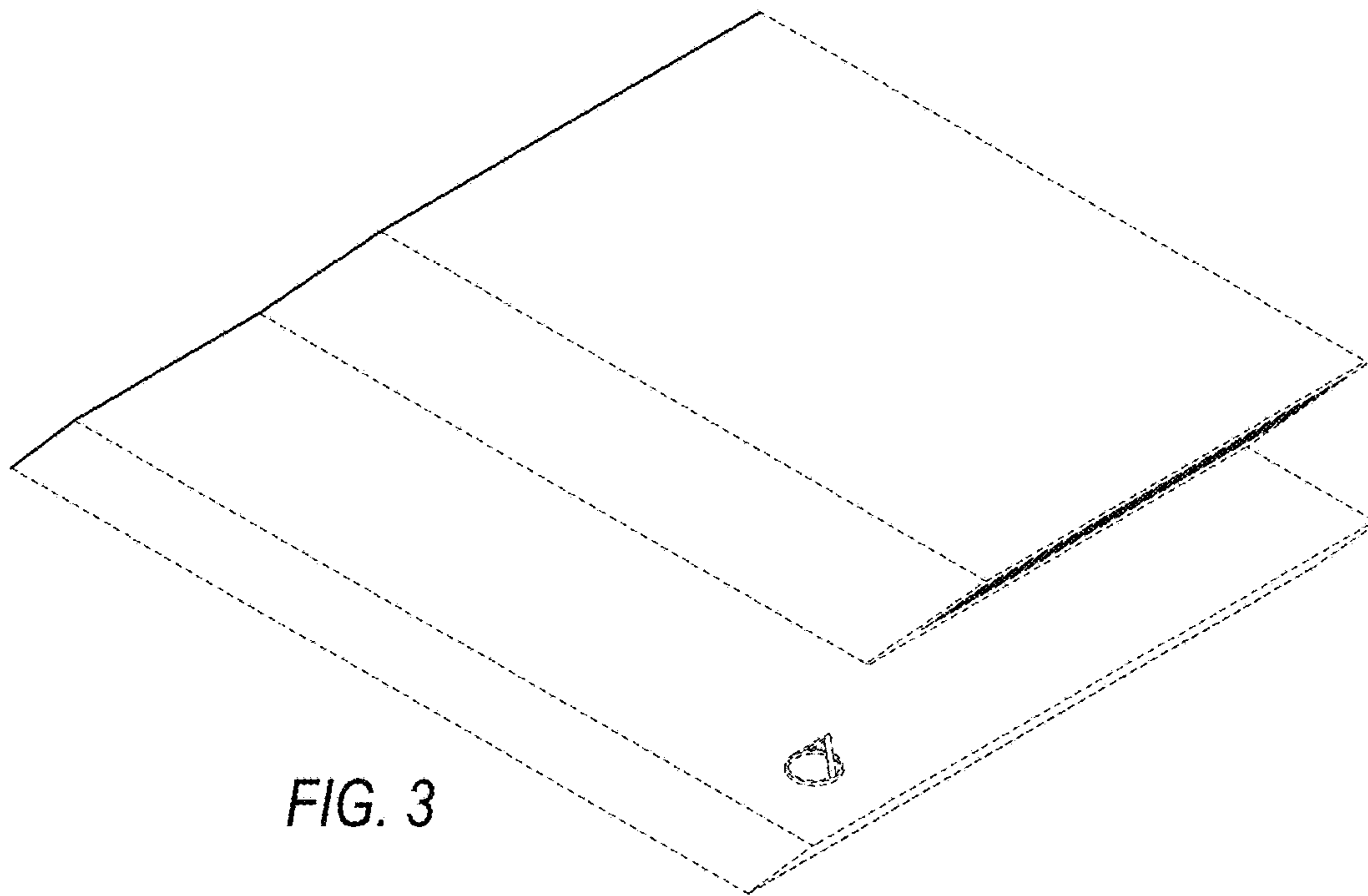


FIG. 4

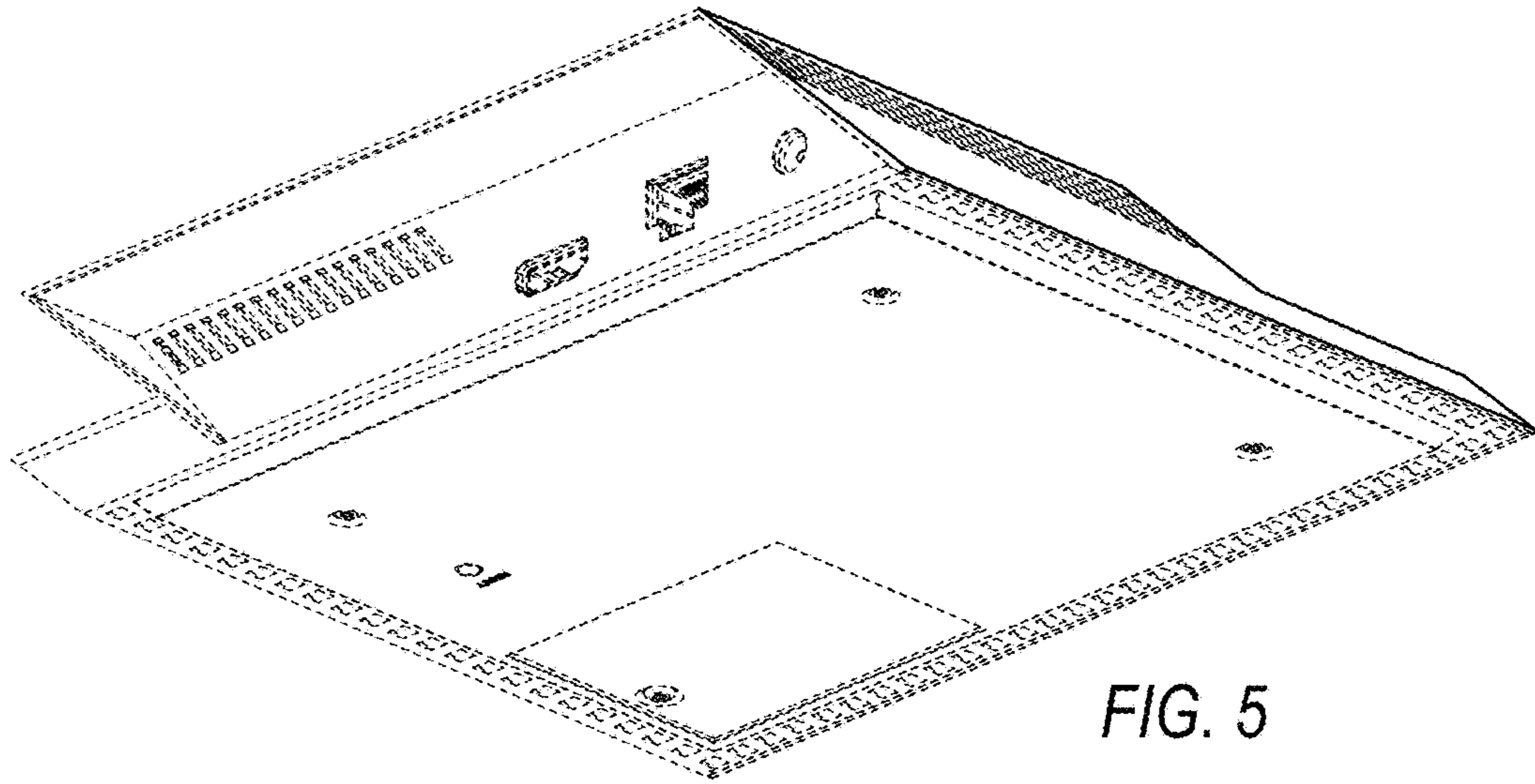


FIG. 5

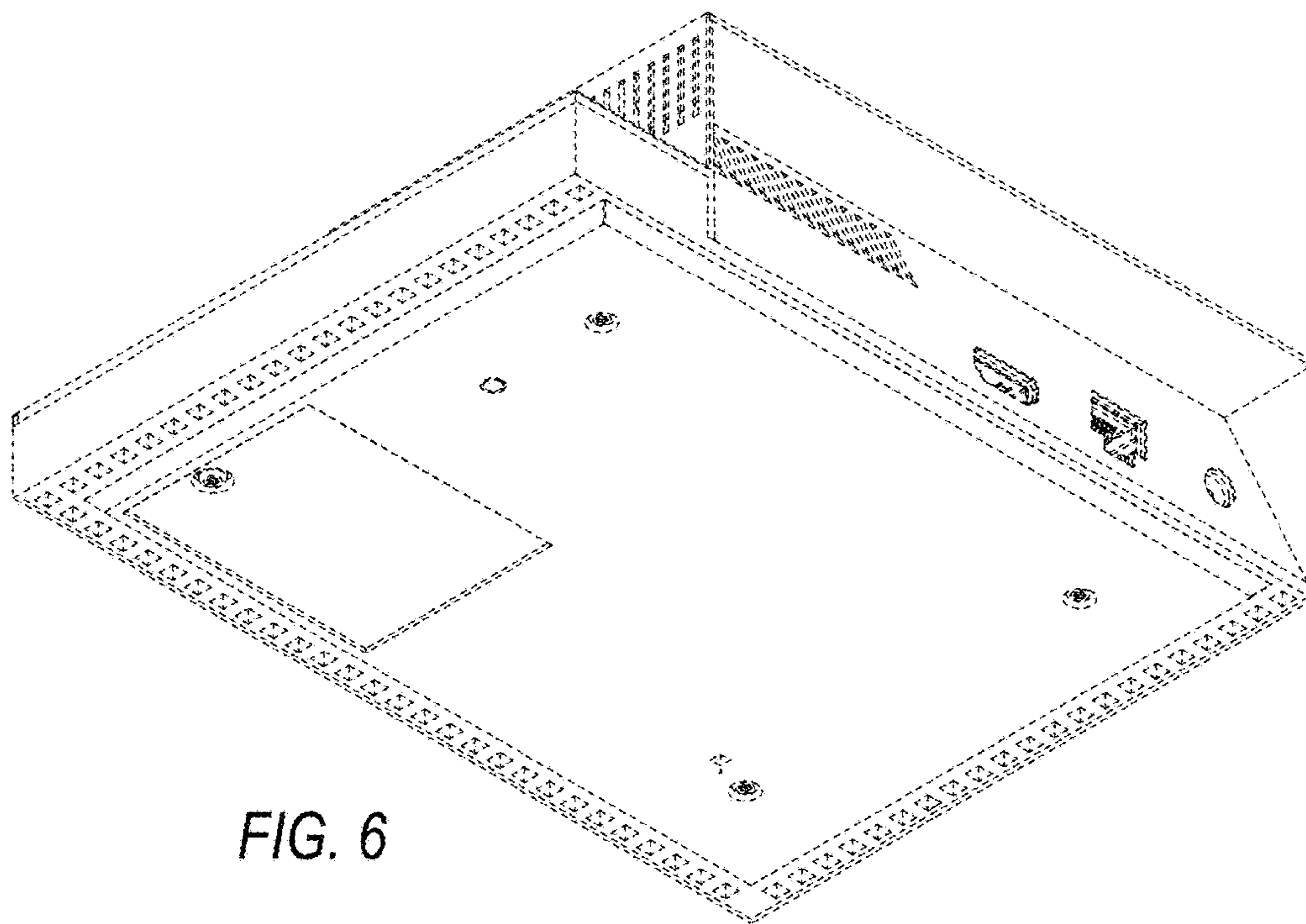


FIG. 6

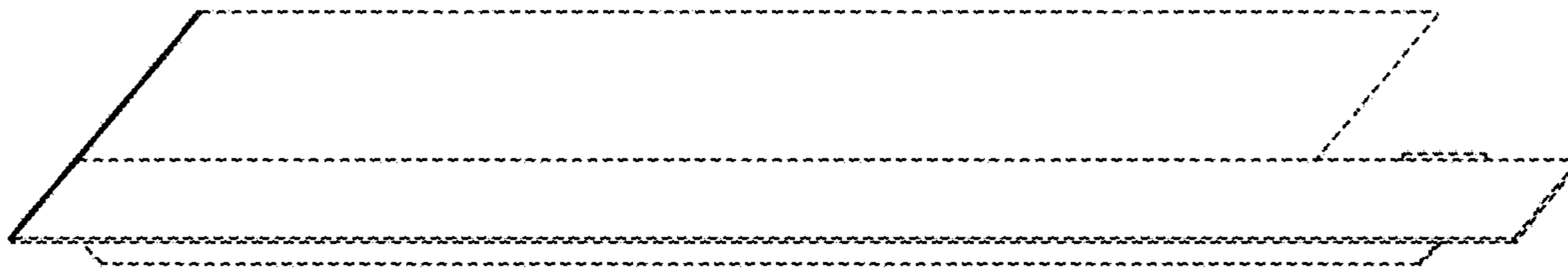


FIG. 7

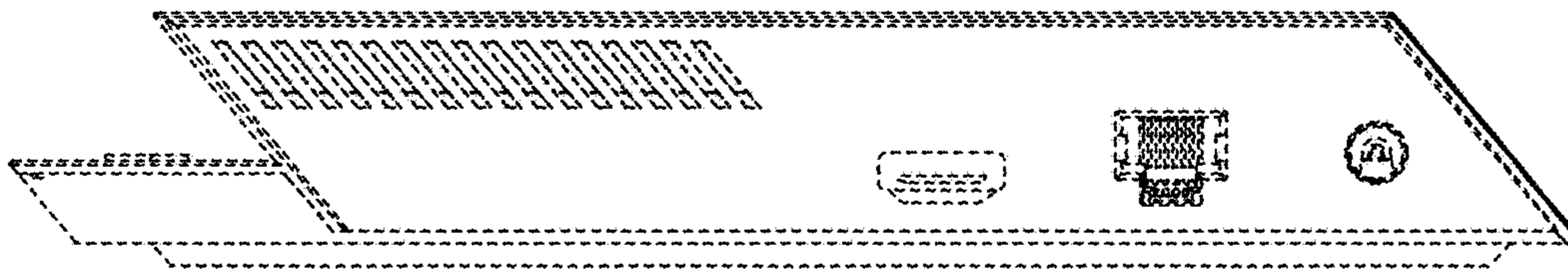


FIG. 8

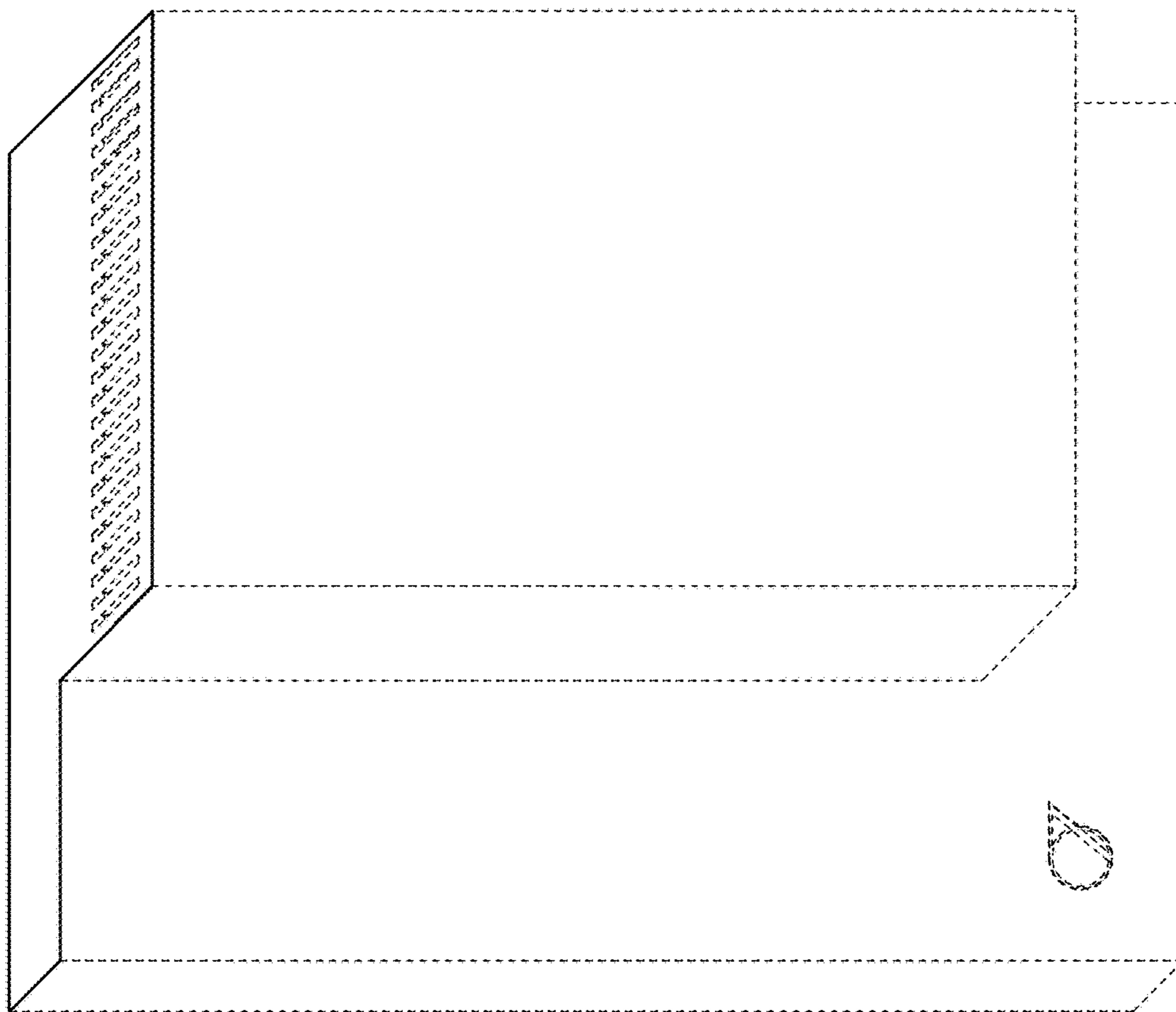


FIG. 9

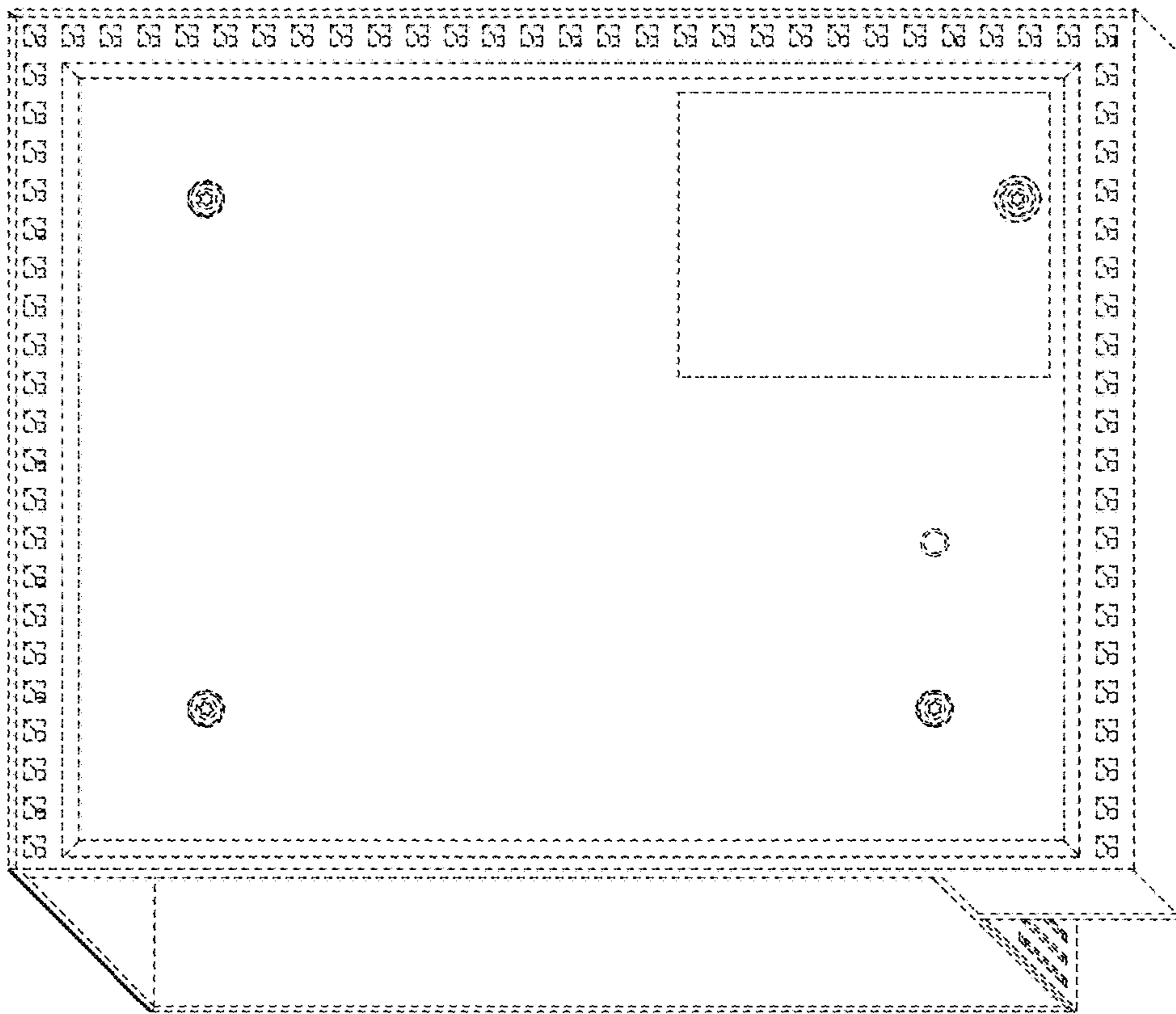


FIG. 10

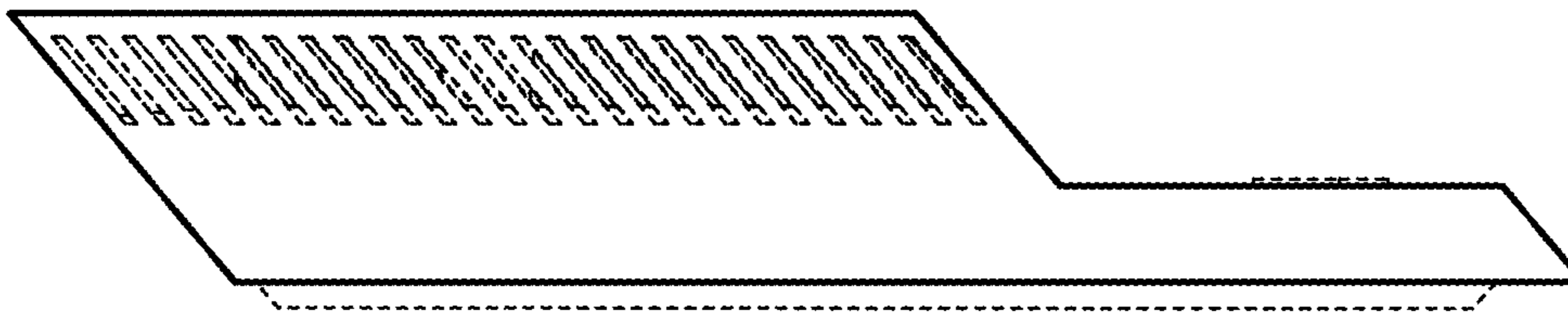


FIG. 11

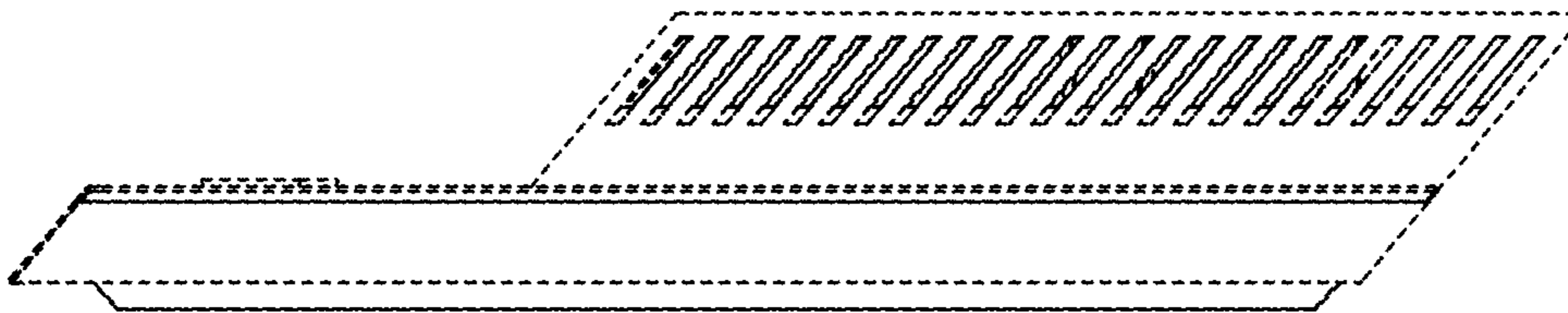


FIG. 12