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Matsumoto et al.

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(54) **SUBSTRATE FOR AN ELECTRONIC CIRCUIT**

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(**) Term: **15 Years**

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(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182, 123, 133, 110, 184, 199; 257/177, 666, 684, 689, 775; 361/600, 361/601, 820; 29/825, 829, 830, 831, 361/832; 174/68.1, 250, 253, 254, 260, 174/261, 268; 216/13; 428/901; D5/4, 61
CPC H01L 25/072; H01L 2224/48245; H01L 23/28; H01L 23/29; H01L 23/298; H01L 23/31; H01L 23/3107; H01L 23/3121; H01L 23/3128; H01L 2924/14; C09K 19/00; C09K 19/02; G06F 1/183; G06F 1/184; G06F 1/187; G11B 33/12; G11B 33/123; G11B 33/124; G11B 33/125;G11B 33/127; G11B 33/128; H05K 1/00; H05K 1/11; H05K 1/111; H05K 1/112; H05K 3/0058; H05K 3/0061; H05K 3/0064; H05K 3/0067
See application file for complete search history.

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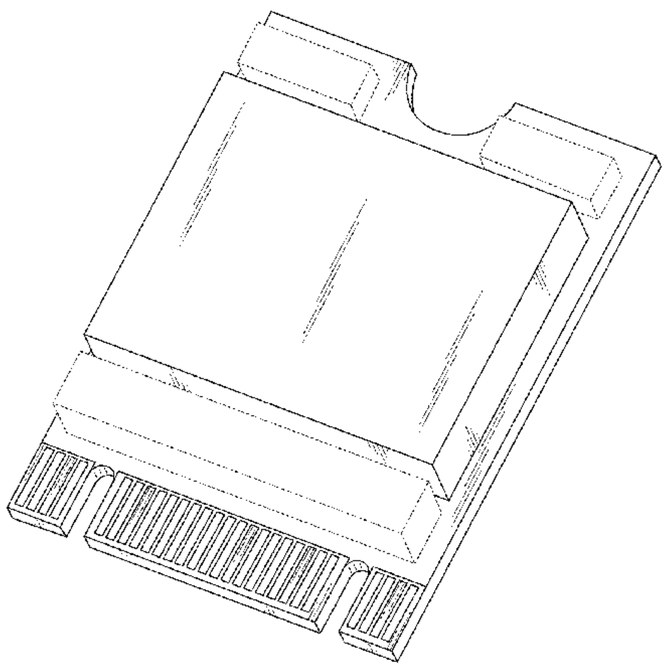
(57) **CLAIM**

The ornamental design for a substrate for an electronic circuit, as shown and described.

DESCRIPTION

FIG. **1** is a perspective view of a substrate for an electronic circuit showing our new design;
FIG. **2** is a rear perspective view thereof;
FIG. **3** is a front elevational view thereof;
FIG. **4** is a rear elevational view thereof;
FIG. **5** is a right side elevational view, a left side elevational view being a mirror image thereof;
FIG. **6** is a top plan view thereof; and,
FIG. **7** is a bottom plan view thereof.
The broken lines shown in the drawings represent portions of the substrate for an electronic circuit that form no part of the claimed design.

1 Claim, 5 Drawing Sheets



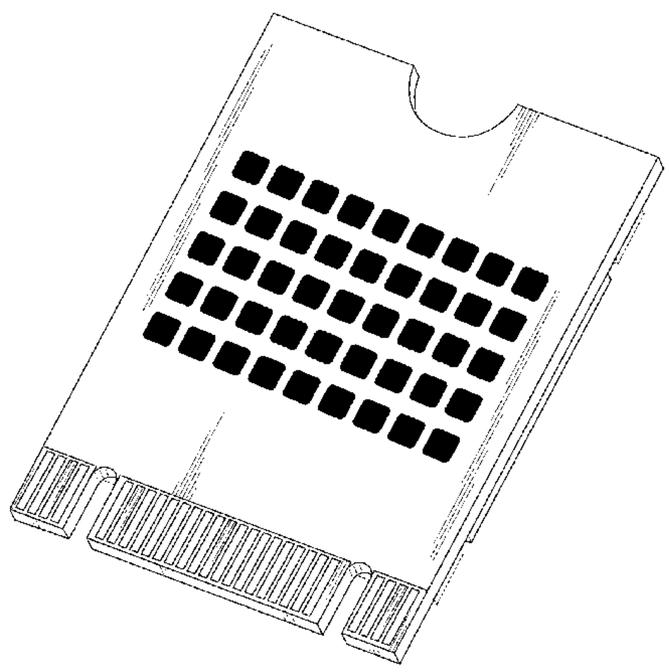


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Fig. 1

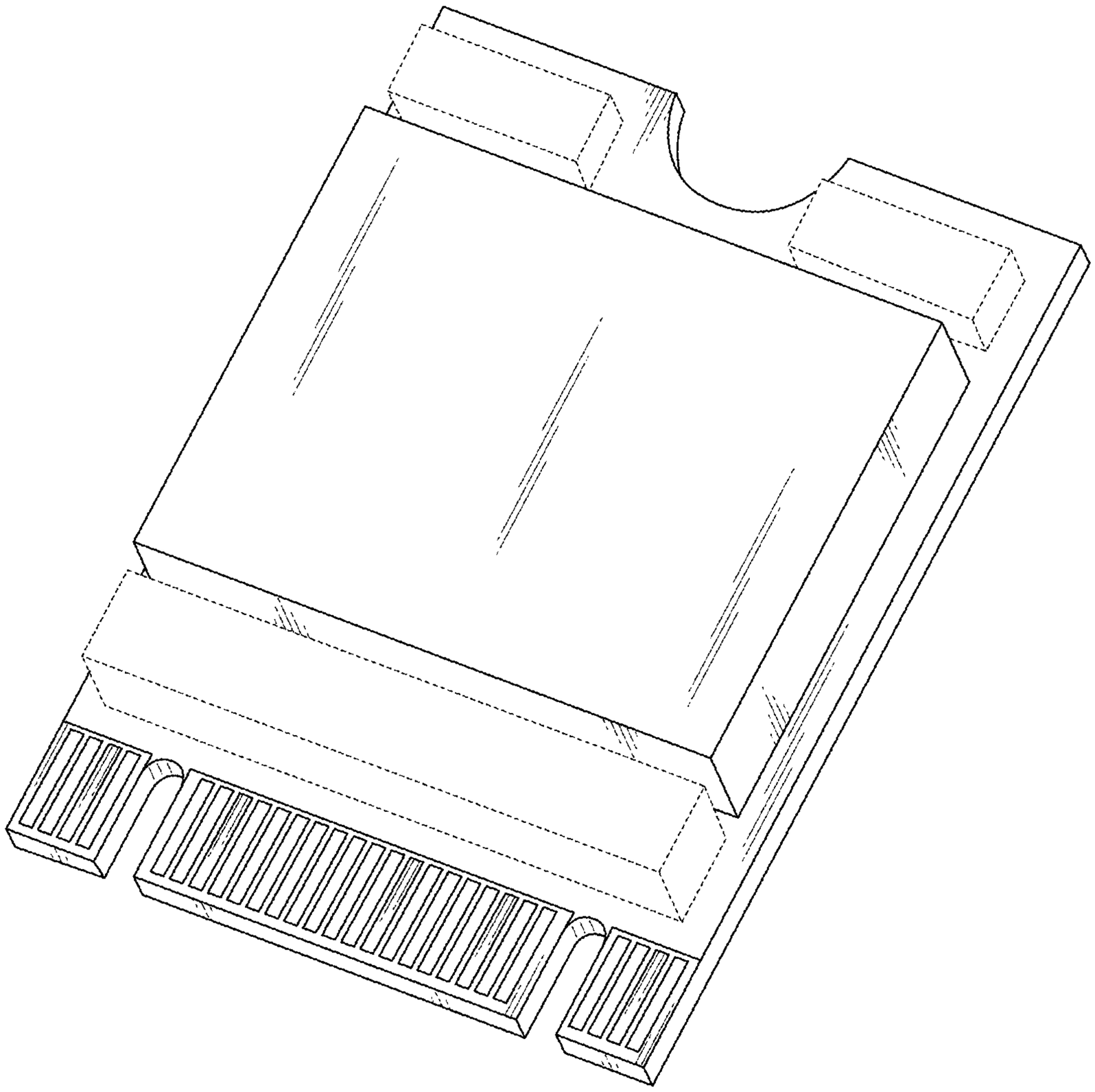

Fig. 2

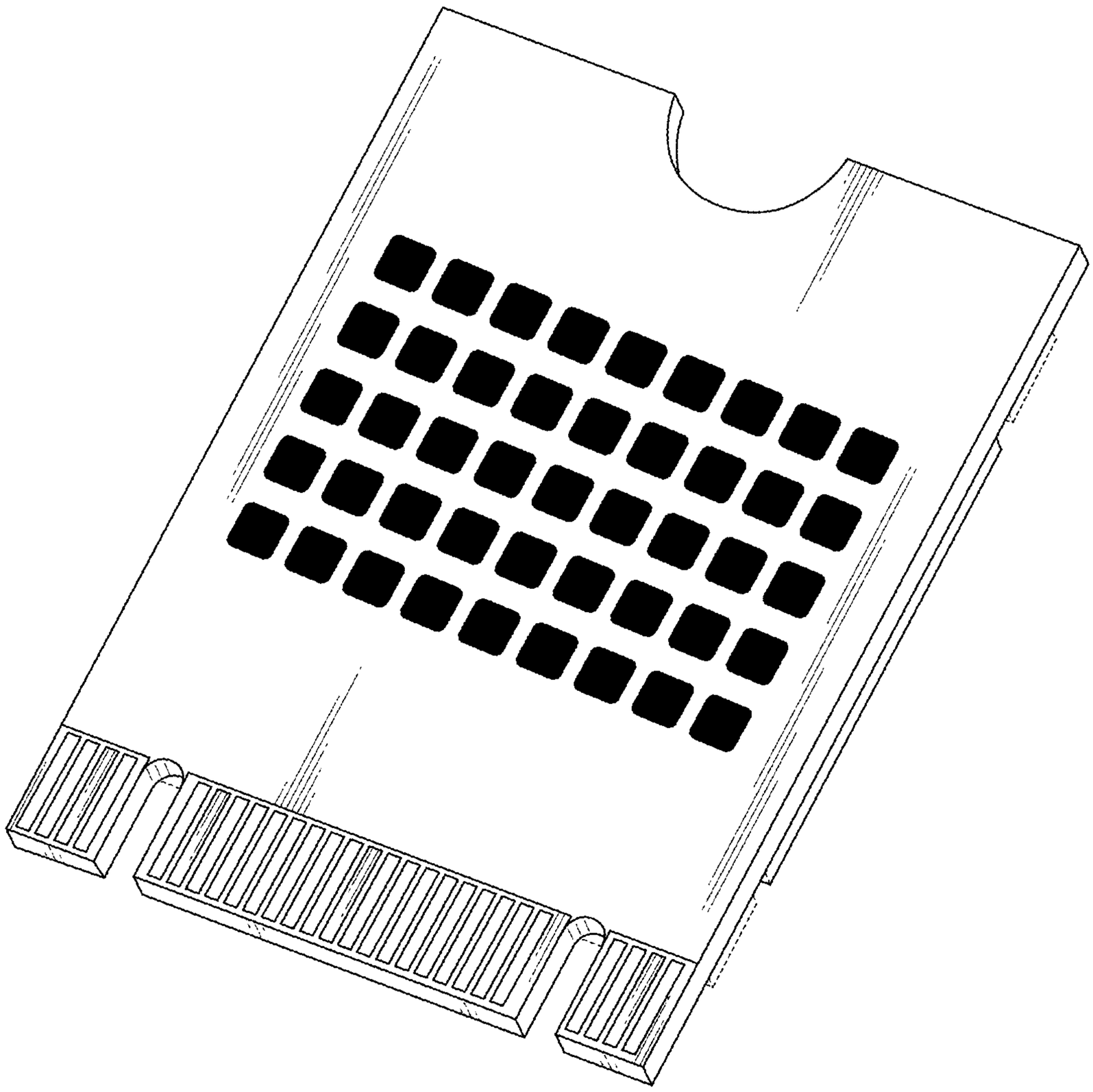

Fig. 3

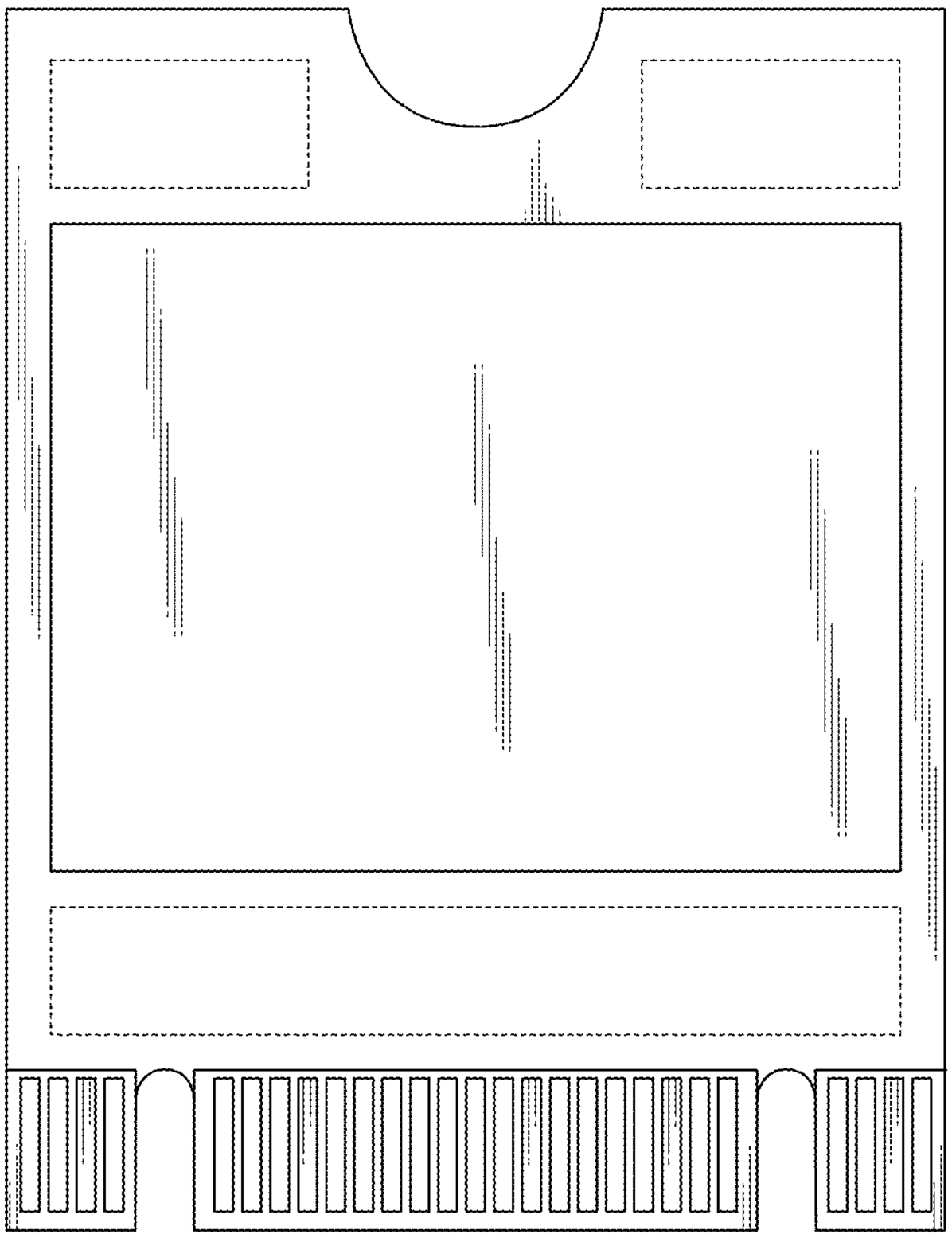

Fig. 4

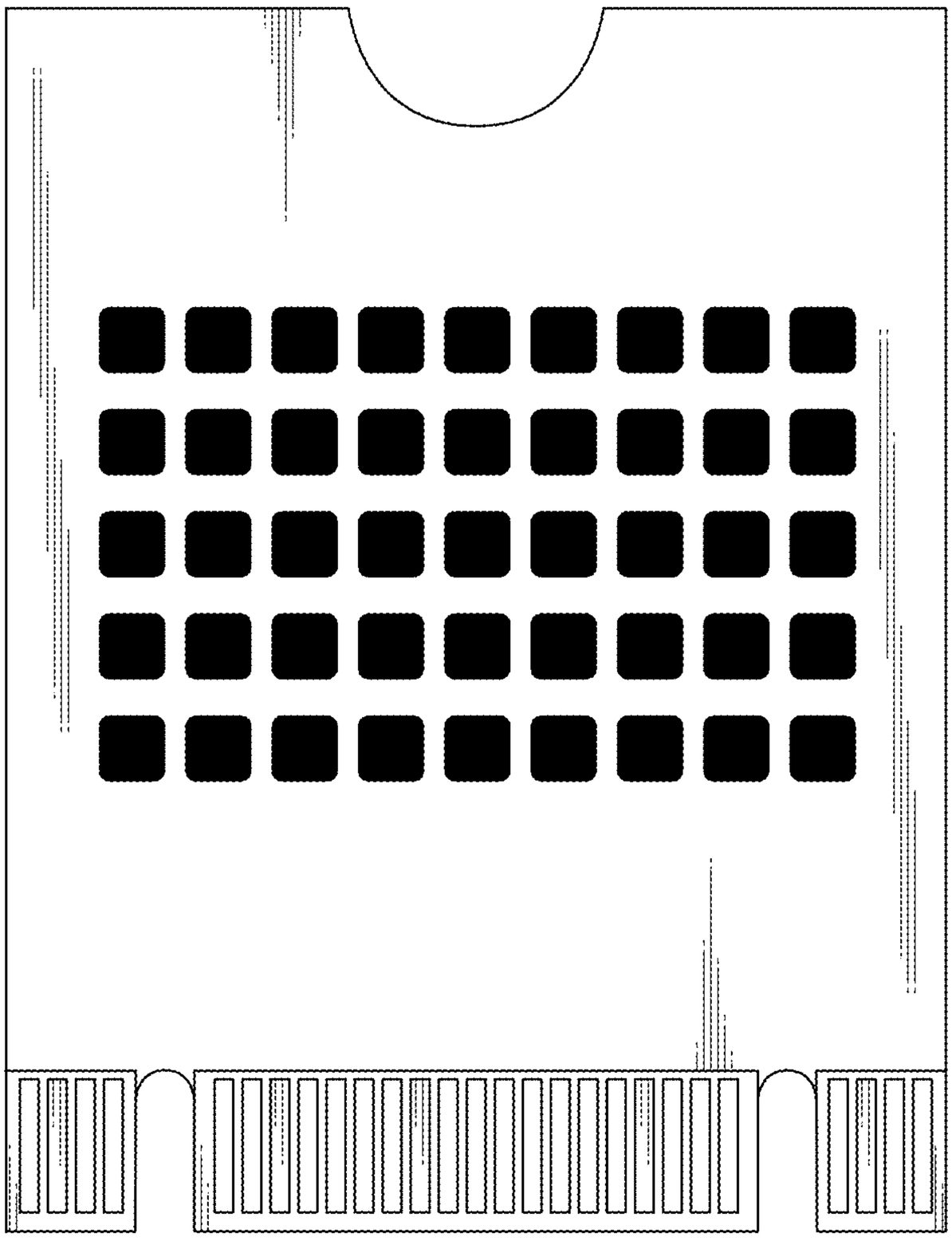

Fig. 5

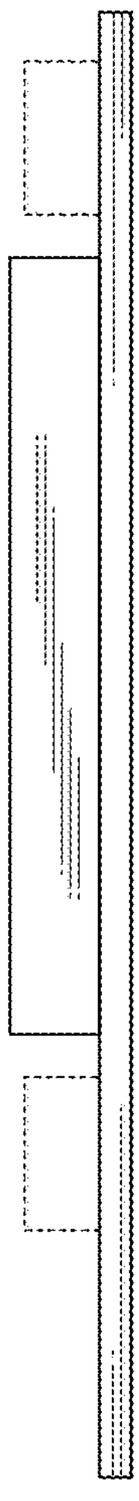

Fig. 6

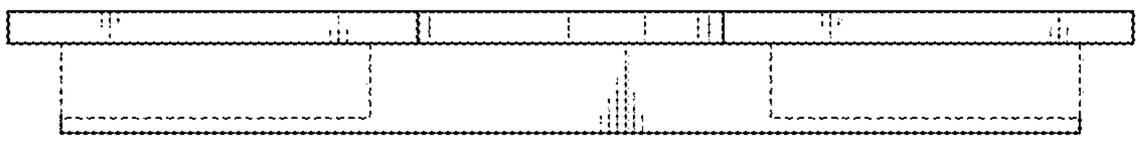

Fig. 7