US00D778851S

(12) United States Design Patent

Matsumoto et al.

(10) Patent No.: US D778,851 S
(45) Date of Patent: ** Feb. 14, 2017

(54) **SUBSTRATE FOR AN ELECTRONIC CIRCUIT**

(71) Applicant: **Kabushiki Kaisha Toshiba**, Minato-ku, Tokyo (JP)

(72) Inventors: **Manabu Matsumoto**, Yokohama (JP); **Isao Ozawa**, Chigasaki (JP)

(73) Assignee: **Kabushiki Kaisha Toshiba**, Minato-ku, Tokyo (JP)

(**) Term: **15 Years**

(21) Appl. No.: **29/564,507**

(22) Filed: **May 13, 2016**

Related U.S. Application Data

(62) Division of application No. 29/500,896, filed on Aug. 29, 2014, now Pat. No. Des. 764,424.

(30) **Foreign Application Priority Data**

May 15, 2014 (JP) 2014-010418
May 15, 2014 (JP) 2014-010419
May 15, 2014 (JP) 2014-010420
May 15, 2014 (JP) 2014-010421

(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182, 123, 133, 110, 184, 199; 257/177, 666, 684, 689, 775; 361/600, 361/601, 820; 29/825, 829, 830, 831, 29/832; 174/68.1, 250, 253, 254, 260, 174/261, 268; 216/13; 428/901; D5/4, 61
CPC H01L 25/072; H01L 2224/48245; H01L 23/28; H01L 23/29; H01L 23/298; H01L 23/31; H01L 23/3107; H01L 23/3121; H01L 23/3128; H01L 2924/14; C09K 19/00; C09K 19/02; G06F 1/183; G06F 1/184; G06F 1/187; G11B 33/12; G11B 33/123; G11B 33/124; G11B 33/125;G11B 33/127; G11B 33/128; H05K 1/00; H05K 1/11; H05K 1/111; H05K 1/112; H05K 3/0058; H05K 3/0061; H05K 3/0064; H05K 3/0067
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

D68,316 S 9/1925 Lader
5,858,481 A 1/1999 Fukushima et al.
6,410,355 B1 * 6/2002 Wallace H01L 22/14 257/107

(Continued)

FOREIGN PATENT DOCUMENTS

CN 488834 5/2002
JP 1104233 3/2001

(Continued)

Primary Examiner — Elizabeth J Oswecki
(74) *Attorney, Agent, or Firm* — Banner & Witcoff, Ltd.

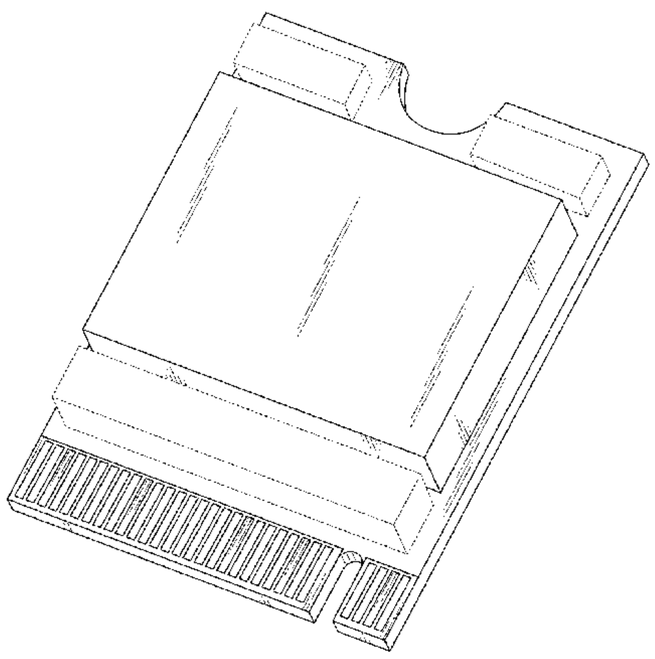
(57) **CLAIM**

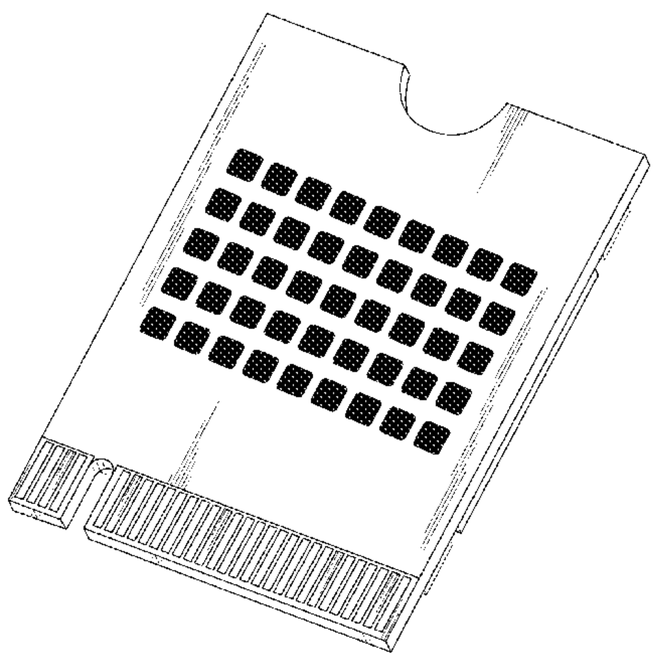
The ornamental design for a substrate for an electronic circuit, as shown and described.

DESCRIPTION

FIG. **1** is a perspective view of a substrate for an electronic circuit showing our new design;
FIG. **2** is a rear perspective view thereof;
FIG. **3** is a front elevational view thereof;
FIG. **4** is a rear elevational view thereof;
FIG. **5** is a right side elevational view, a left side elevational view being a mirror image thereof;
FIG. **6** is a top plan view thereof; and,
FIG. **7** is a bottom plan view thereof.
The broken lines shown in the drawings represent portions of the substrate for an electronic circuit that form no part of the claimed design.

1 Claim, 5 Drawing Sheets





(56) **References Cited**

U.S. PATENT DOCUMENTS

D459,706	S	7/2002	Ebihara et al.	
D471,524	S	3/2003	Ebihara et al.	
D526,972	S	8/2006	Egawa et al.	
D531,139	S	10/2006	Egawa et al.	
7,306,161	B2 *	12/2007	Takiar	G06K 13/0825 235/441
7,307,848	B2 *	12/2007	Takiar	G06K 19/077 361/736
D608,741	S	1/2010	Miyashita	
7,864,540	B2 *	1/2011	Takiar	G06K 19/04 361/736
D633,672	S	3/2011	McKnight	
D633,673	S	3/2011	McKnight	
D637,193	S	5/2011	Andre et al.	
D670,917	S	11/2012	Blackford	
D673,922	S	1/2013	Moriai et al.	
D674,759	S	1/2013	Chang et al.	
D686,175	S	7/2013	Gurary et al.	
D686,582	S	7/2013	Krishnan et al.	
D690,671	S	10/2013	Gurary et al.	
D699,201	S	2/2014	Petsch	
D702,445	S	4/2014	Boyle	
D704,155	S	5/2014	Chang et al.	
D716,743	S *	11/2014	Hu	D13/182
D727,861	S *	4/2015	Tang	D13/182
D730,304	S	5/2015	Matsumoto et al.	
D753,073	S *	4/2016	Sponring	D13/182
D757,666	S *	5/2016	Yokoo	D13/182
D761,745	S *	7/2016	Shinkai	D13/182
D764,424	S *	8/2016	Matsumoto	D13/182
D768,115	S *	10/2016	Kazanchian	D13/182
2003/0094628	A1	5/2003	Yeh et al.	
2006/0168721	A1	8/2006	McGuire et al.	
2008/0123318	A1	5/2008	Lam	
2010/0326710	A1	12/2010	Zhang	
2011/0051351	A1	3/2011	Harashima	

FOREIGN PATENT DOCUMENTS

JP	1287854	12/2006
JP	1426168	10/2011
JP	1479369	9/2013
JP	1479370	9/2013
KR	30-0470075	11/2007

* cited by examiner

Fig. 1

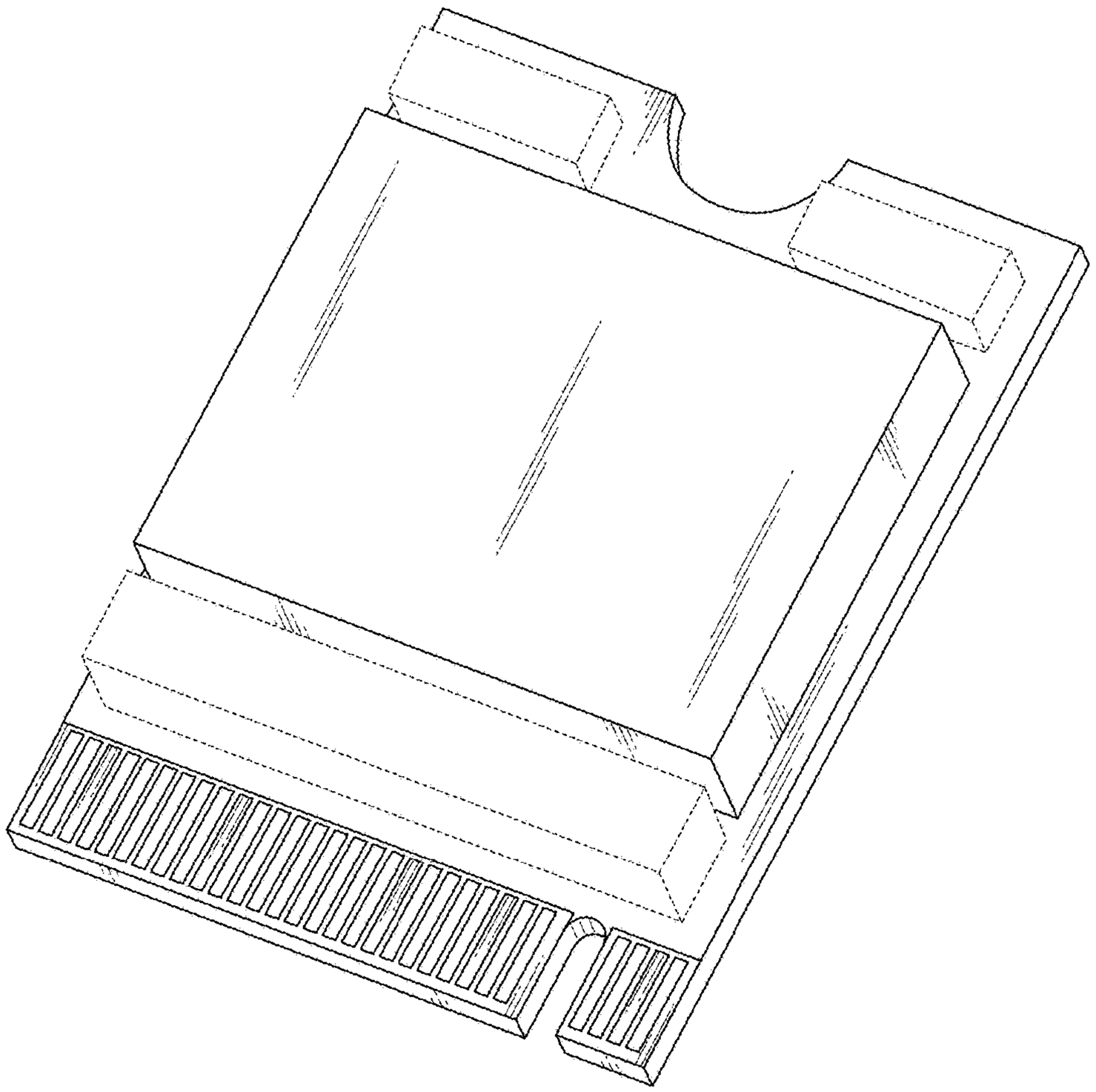


Fig. 2

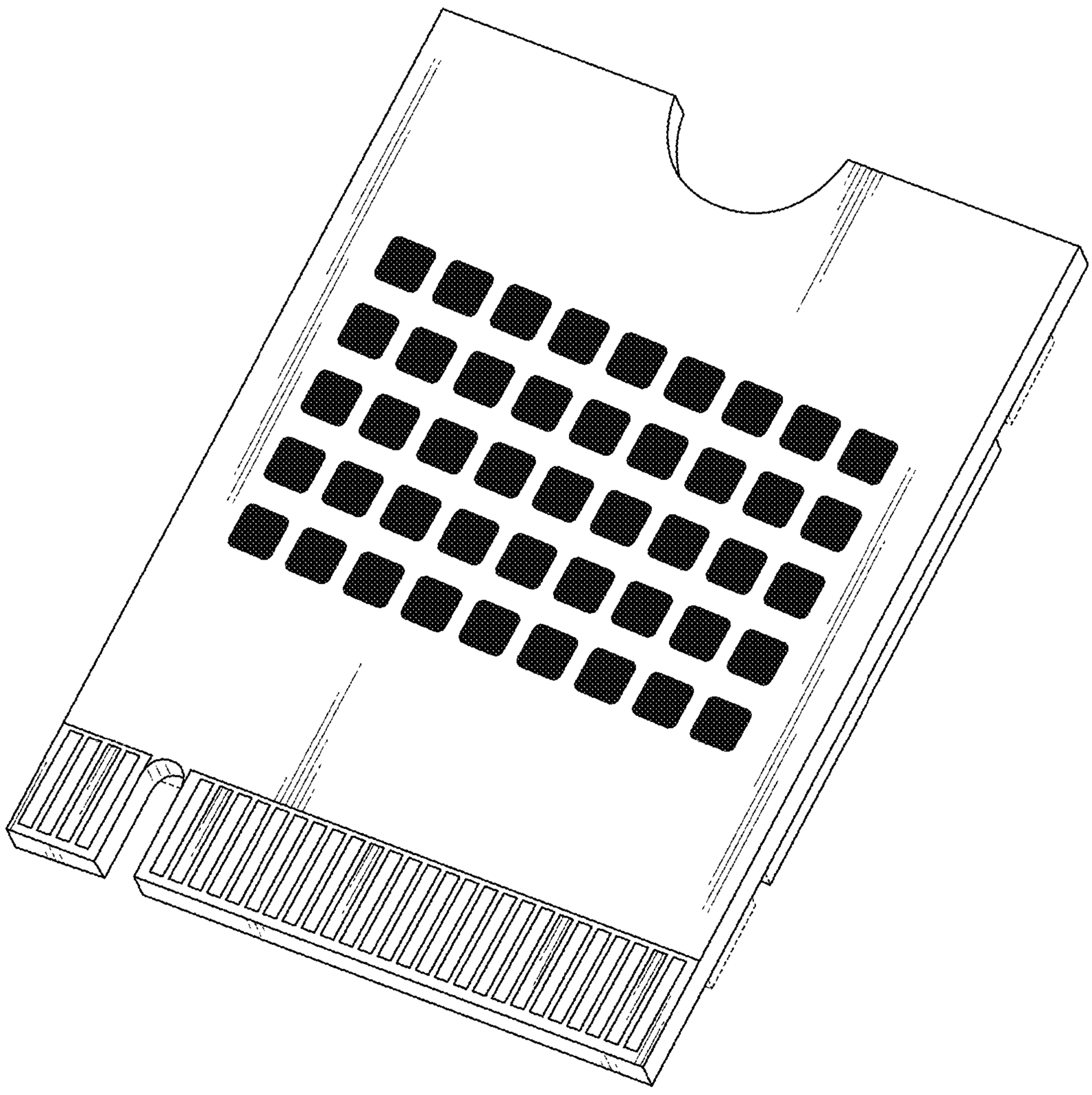


Fig. 3

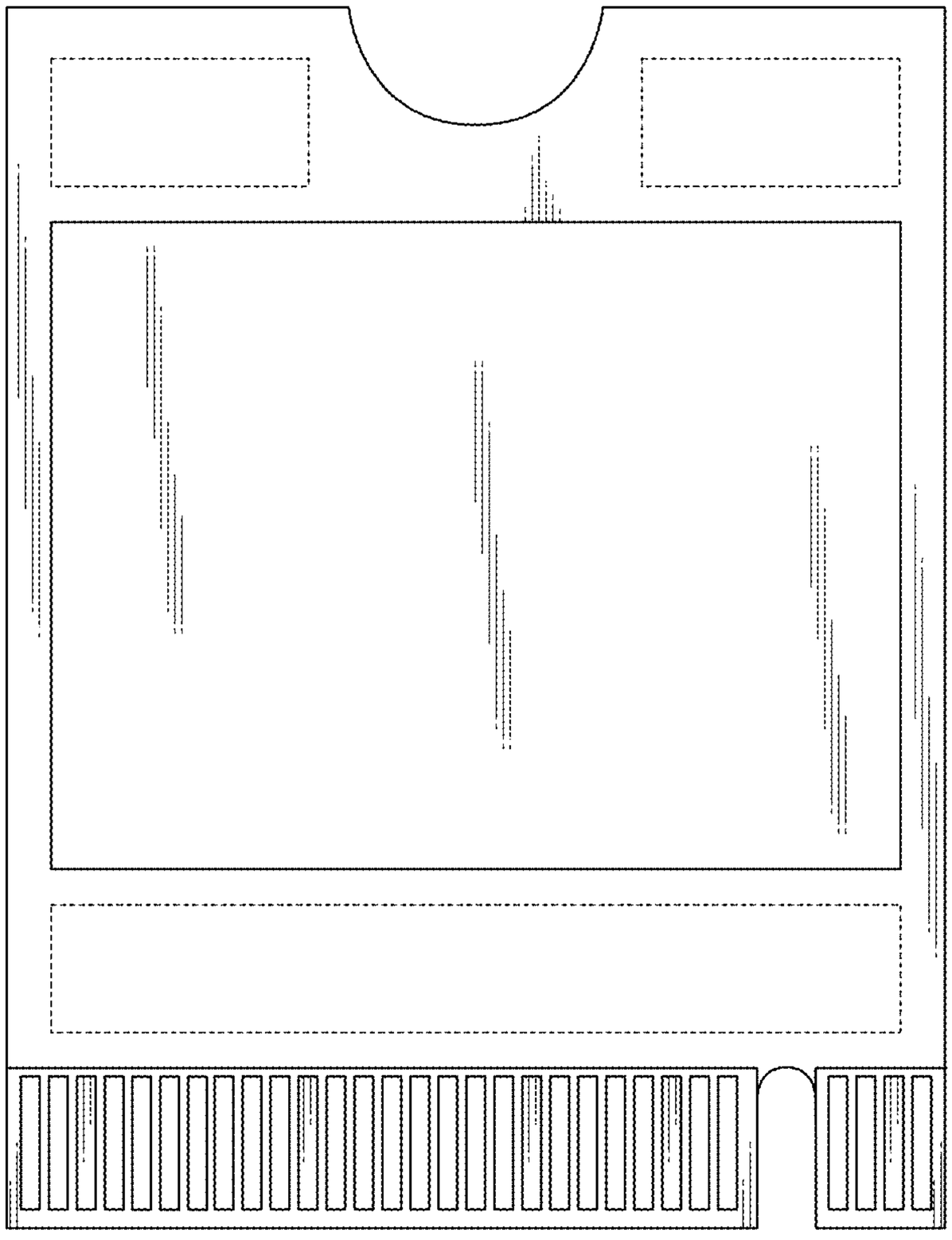


Fig. 4

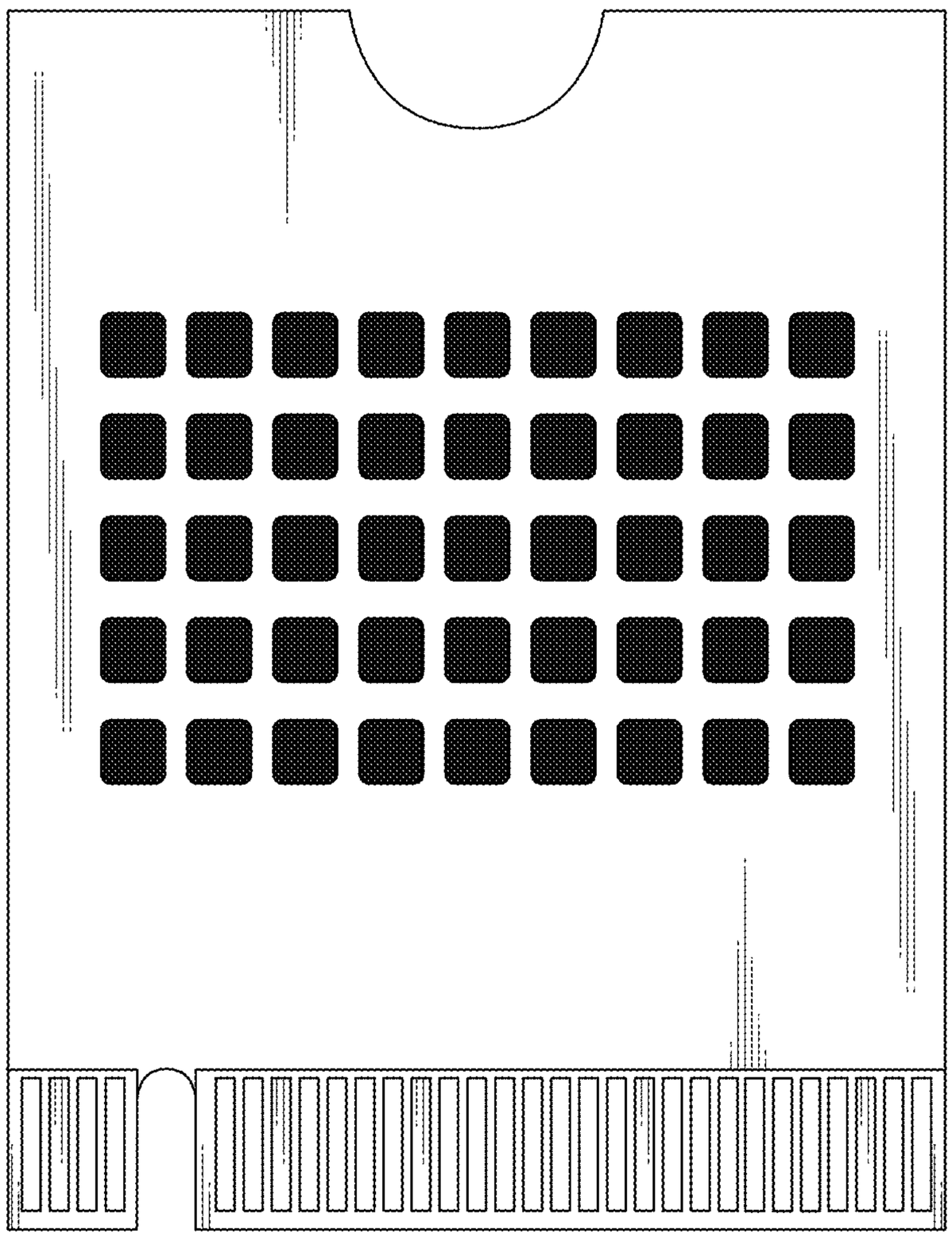


Fig. 5

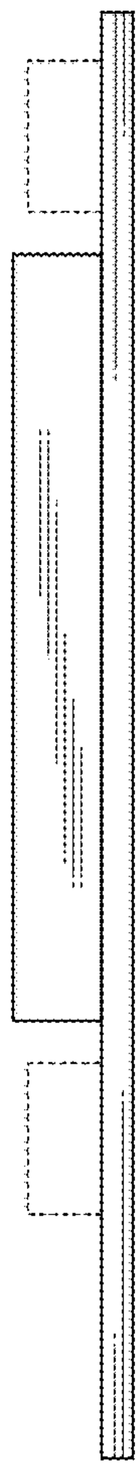


Fig. 6

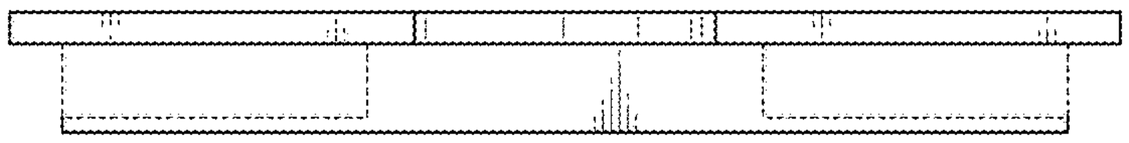


Fig. 7