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(12) **United States Design Patent**
Soyano et al.

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(45) **Date of Patent:** **** Dec. 20, 2016**

(54) **SEMICONDUCTOR MODULE**

6/4262;G02B 6/428; G02B 6/4281; H05K
1/14; H05K 1/141; H05K 1/142; H05K
1/144; H05K

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(Continued)

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(56) **References Cited**

U.S. PATENT DOCUMENTS

D357,672 S * 4/1995 Terasawa D13/182
D396,450 S * 7/1998 Nishiura D13/182

(Continued)

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(**) Term: **15 Years**

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(21) Appl. No.: **29/528,214**

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(57) **CLAIM**

The ornamental design for a semiconductor module, as
shown and described.

(30) **Foreign Application Priority Data**

Nov. 28, 2014 (JP) D2014-026634
Nov. 28, 2014 (JP) D2014-026635
Nov. 28, 2014 (JP) D2014-026636

DESCRIPTION

(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**

USPC D13/182
CPC H01L 21/00; H01L 21/02433; H01L
2224/42; H01L 2224/43; H01L 2021/00;
H01L 2021/02; H01L 2021/04; H01L
21/4814; H01L 21/4846; H01L 21/4871;
H01L 21/67144; H01L 23/12; H01L
23/13; H01L 23/14; H01L 23/147; H01L
2924/171; H01L 2924/1711; H01L
2924/17151; H01L 2924/181; H01L
2924/1811; H01L 2924/1815; H01L
2924/1905; H01L 29/04; H01L
2224/08054; H01L 23/58; H05B 41/14;
H02B 6/4201; G02B 6/4256; G02B
6/4257; G02B 6/4261; G02B

FIG. 1 is a front view of a semiconductor module showing
our new design;

FIG. 2 is a rear view thereof;

FIG. 3 is a left side view thereof;

FIG. 4 is a right side view thereof;

FIG. 5 is a top view thereof;

FIG. 6 is a bottom view thereof;

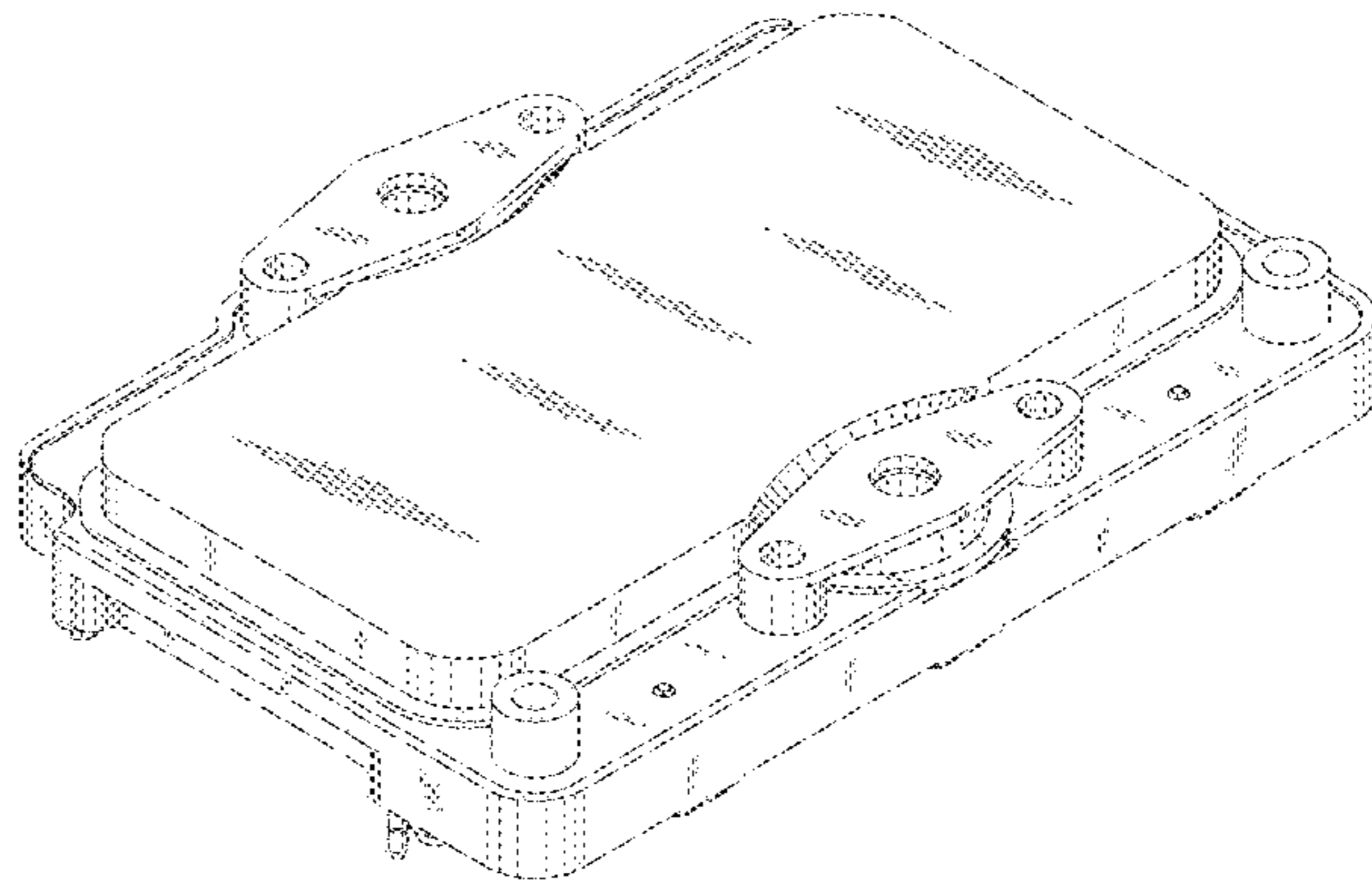
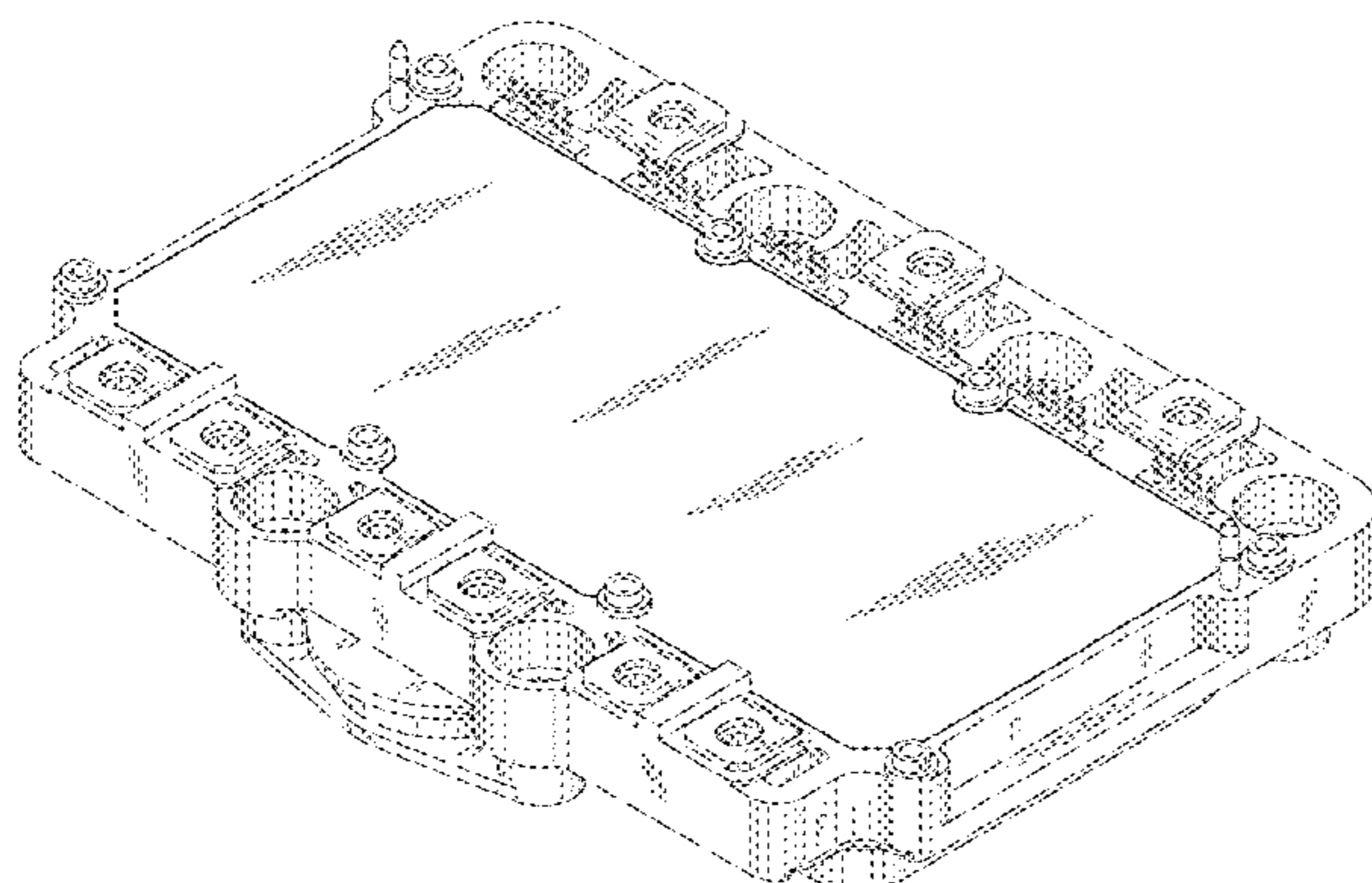
FIG. 7 is a front, right, and bottom perspective view thereof;
and,

FIG. 8 is a rear, left, and top perspective view thereof.

The ornamental design of the present disclosure is a semi-
conductor module on which power semiconductor elements
and the like may be mounted. Rhombic plate members
having rounded corners are centered along the long sides of
the rear view, such that the longer diagonal line of each
rhombic plate member extends along a long side.

The broken lines shown in the drawing views of FIGS. 1-8
form no part of the claimed design.

1 Claim, 8 Drawing Sheets



(58) **Field of Classification Search**

CPC 1/18;H05K 1/181; H05K 1/182; H05K
 1/026; H05K 1/0228; H05K
 1/0245; H05K 1/0236; H05K 1/0263
 See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

D441,726	S *	5/2001	Sofue	D13/182
6,521,983	B1 *	2/2003	Yoshimatsu	H01L 25/072 257/678
D587,662	S *	3/2009	Soutome	D13/182
D589,012	S *	3/2009	Soyano	D13/182
D606,951	S *	12/2009	Soyano	D13/182
D653,633	S *	2/2012	Soyano	D13/182
D653,634	S *	2/2012	Soyano	D13/182
D686,174	S *	7/2013	Soyano	D13/182
D689,446	S *	9/2013	Soyano	D13/180
D704,670	S	5/2014	Chen et al.	
D704,671	S	5/2014	Chen et al.	
D705,184	S	5/2014	Takahashi et al.	
D706,232	S	6/2014	Nakamura	
D710,317	S	8/2014	Chen et al.	
D710,318	S	8/2014	Chen et al.	
D710,319	S	8/2014	Chen et al.	
D712,853	S	9/2014	Nakamura	
D721,048	S	1/2015	Nakamura	
D721,340	S	1/2015	Nakamura	
D724,554	S	3/2015	Motohashi et al.	
D748,595	S *	2/2016	Bertalan	D13/182
2001/0038143	A1 *	11/2001	Sonobe	H01L 24/49 257/690
2010/0149774	A1 *	6/2010	Matsumoto	H01L 23/055 361/783

* cited by examiner

FIG. 1

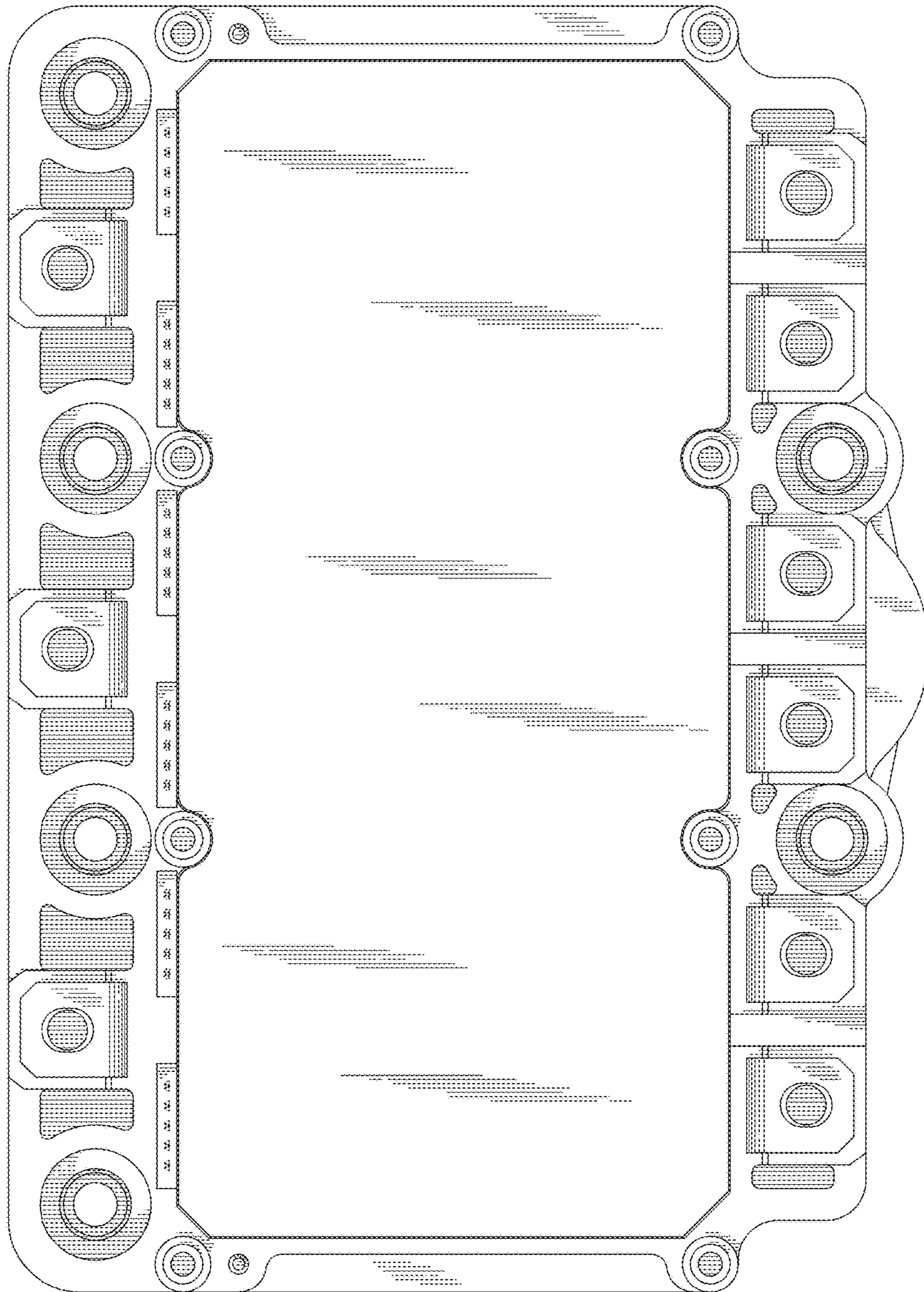


FIG. 2

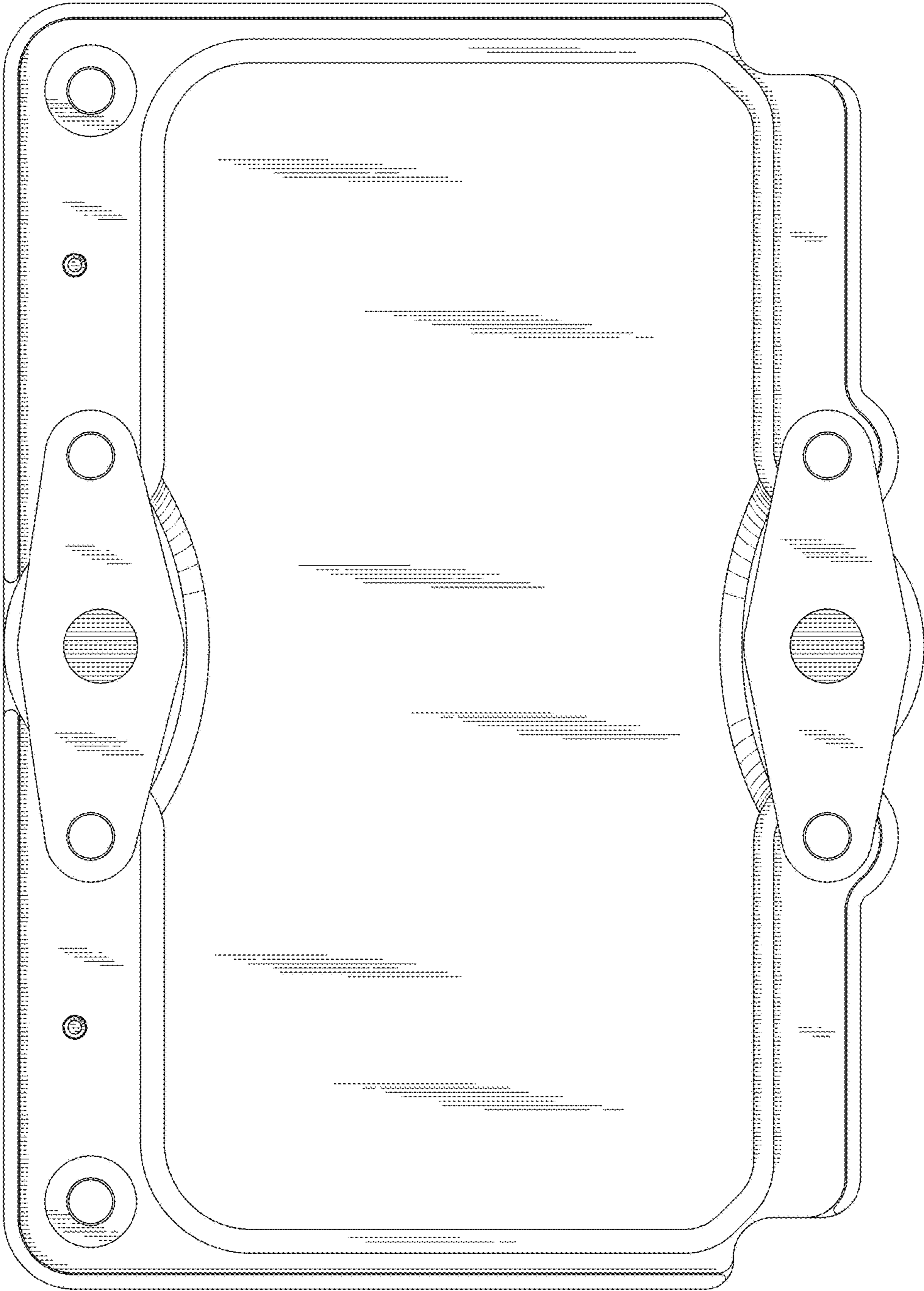


FIG. 3

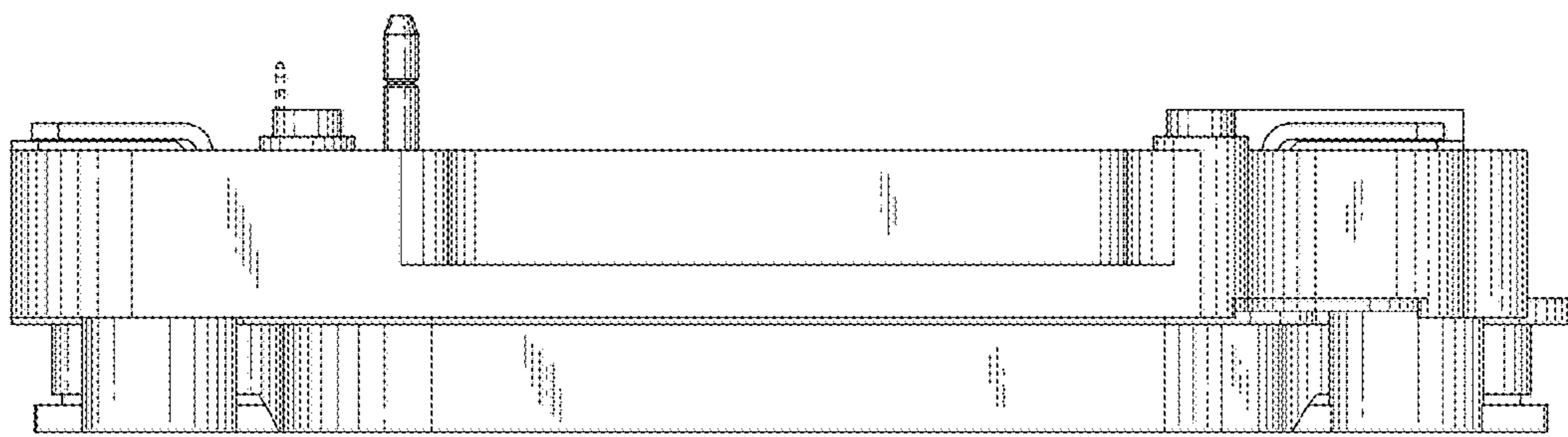


FIG. 4

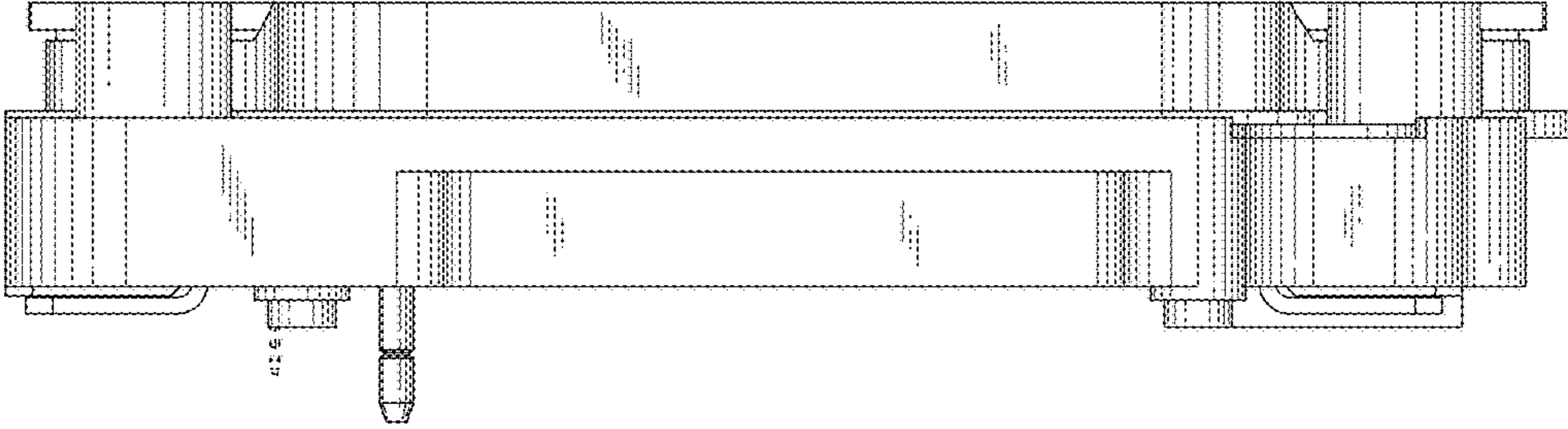


FIG. 5

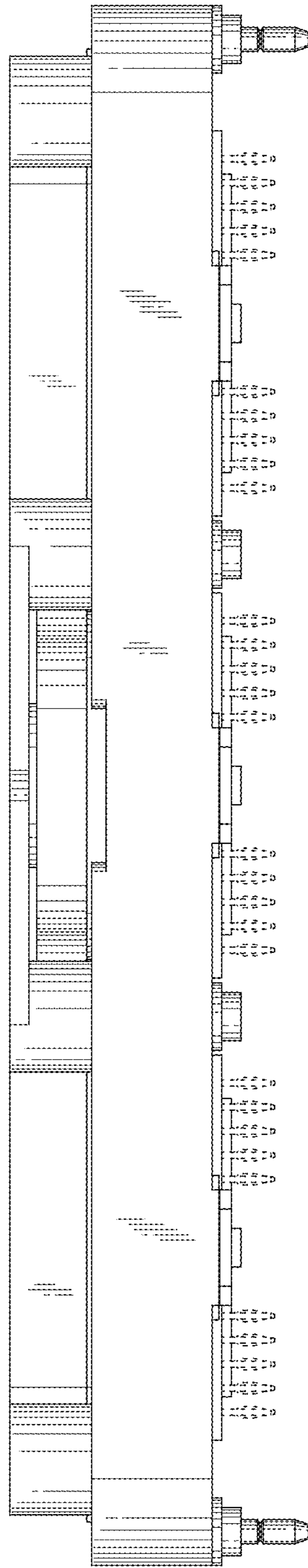
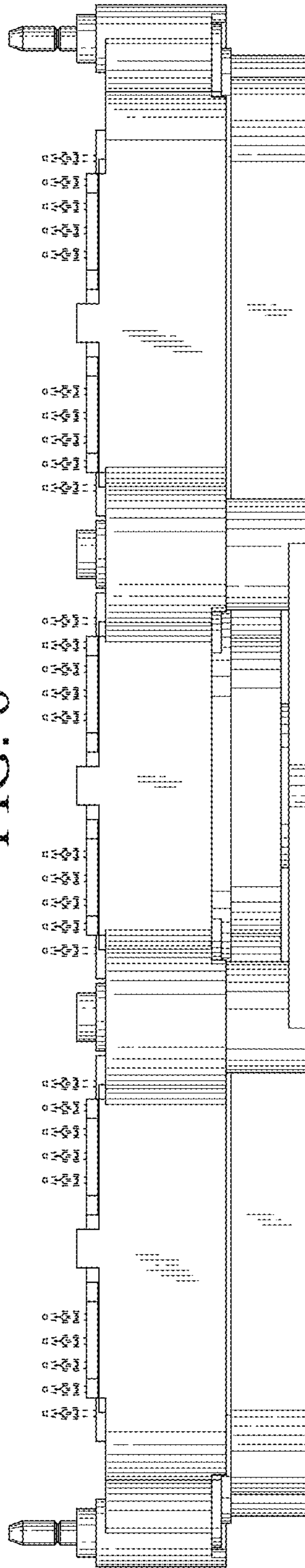
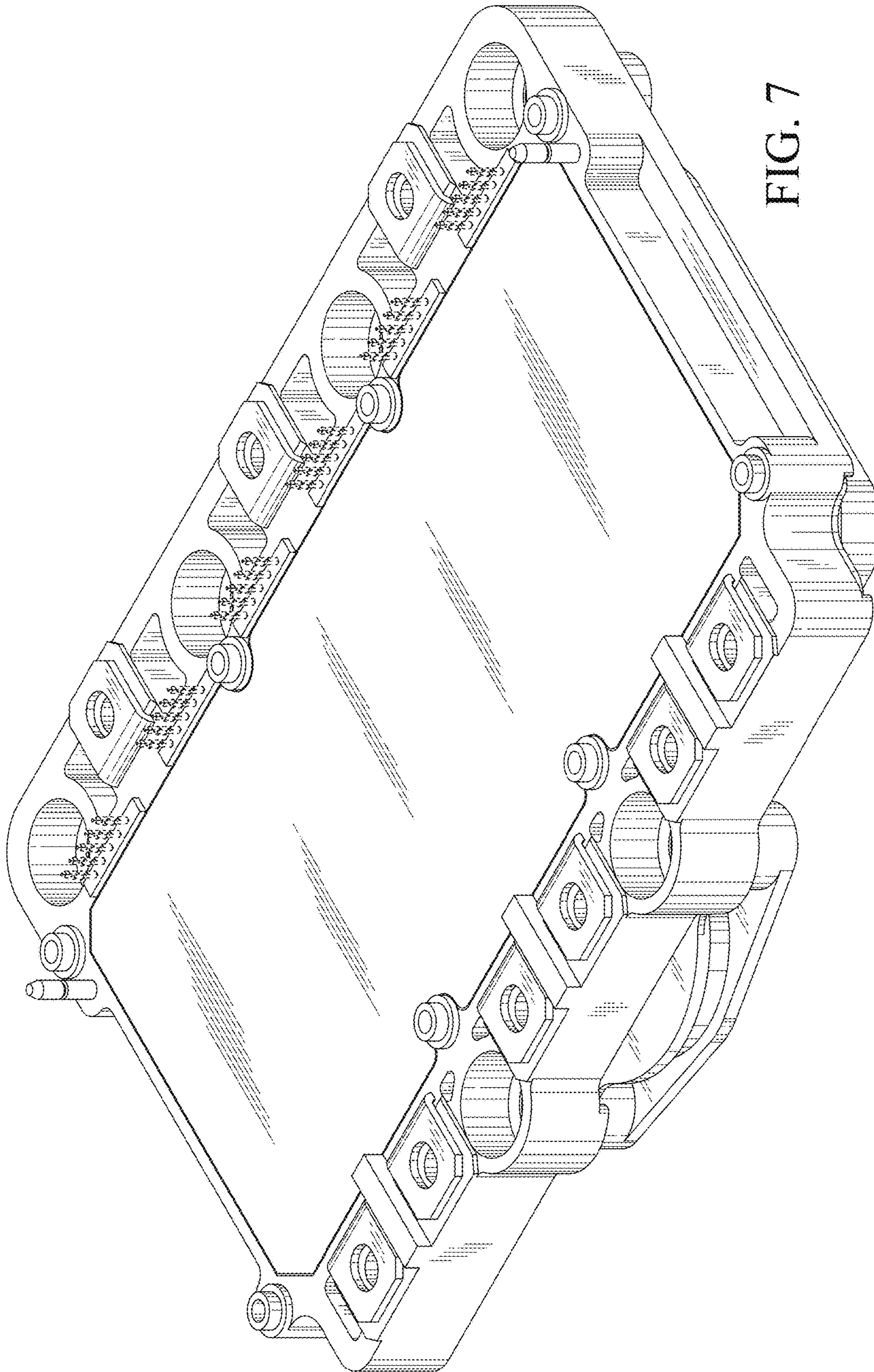


FIG. 6





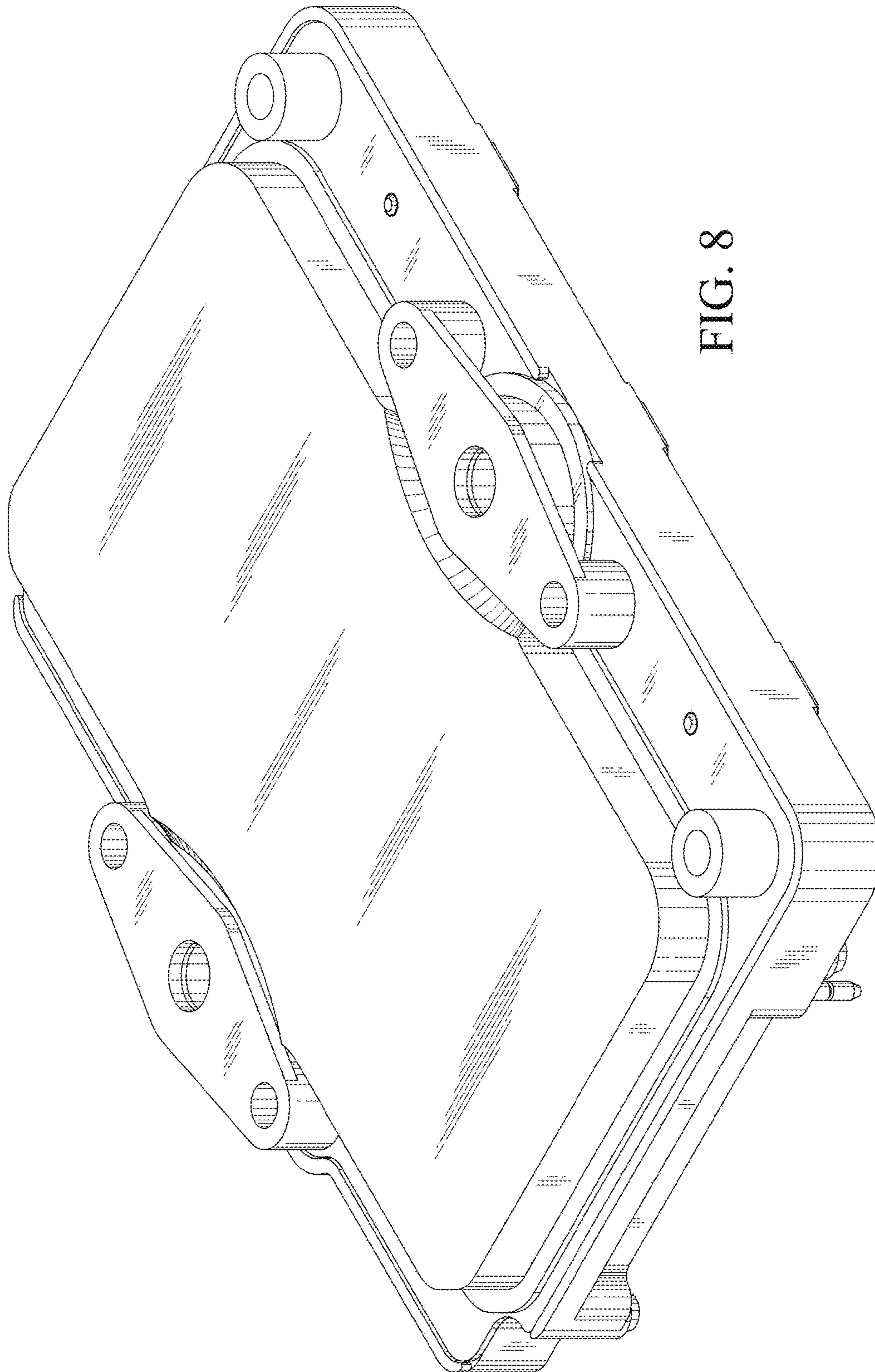


FIG. 8