



US00D772184S

(12) **United States Design Patent**
Soyano et al.

(10) **Patent No.:** **US D772,184 S**

(45) **Date of Patent:** **** Nov. 22, 2016**

(54) **SEMICONDUCTOR MODULE**

(71) Applicant: **Fuji Electric Co., Ltd.**, Kawasaki-shi, Kanagawa (JP)

(72) Inventors: **Shin Soyano**, Tokyo (JP); **Yoshikazu Takamiya**, Tokyo (JP); **Toru Yamada**, Tokyo (JP); **Ryo Maruyama**, Tokyo (JP)

(73) Assignee: **Fuji Electric Co., Ltd.**, Kawasaki-shi, Kanagawa (JP)

(**) Term: **15 Years**

(21) Appl. No.: **29/531,129**

(22) Filed: **Jun. 23, 2015**

(30) **Foreign Application Priority Data**

Dec. 24, 2014 (JP) D2014-028804
Dec. 24, 2014 (JP) D2014-028805
Dec. 24, 2014 (JP) D2014-028806

(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182
CPC H01L 21/00; H01L 21/02433; H01L 2224/42; H01L 2224/43; H01L 2021/00; H01L 2021/02; H01L 2021/04; H01L 21/4814; H01L 21/4846; H01L 21/4871; H01L 21/67144; H01L 23/12; H01L 23/13; H01L 23/14; H01L 23/147; H01L 2924/171; H01L 2924/1711; H01L 2924/17151; H01L 2924/181; H01L 2924/1811; H01L 2924/1815; H01L 2924/1905; H01L 29/04; H01L 2224/08054; H01L 23/58; H05B 41/14; H02B 6/4201; G02B 6/4281; G02B 6/4256; G02B 6/4257; G02B 6/4261; G02B 6/4262; G02B 6/428; H05K 1/14; H05K 1/141; H05K 1/142; H05K 1/144; H05K 1/18; H05K 1/181; H05K 1/182; H05K 1/026;

H05K 1/0228; H05K 1/0245; H05K 1/0236;
H05K 1/0263

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

D357,672 S * 4/1995 Terasawa D13/182
D396,450 S * 7/1998 Nishiura D13/182

(Continued)

OTHER PUBLICATIONS

U.S. Appl. No. 29/528,214, filed May 27, 2015.

Primary Examiner — Elizabeth J Oswecki

(74) *Attorney, Agent, or Firm* — Young Basile Hanlon & MacFarlane, P.C.

(57) **CLAIM**

The ornamental design for a semiconductor module, as shown and described.

DESCRIPTION

FIG. 1 is a front view of a semiconductor module showing our new design;
FIG. 2 is a rear view thereof;
FIG. 3 is a left side view thereof;
FIG. 4 is a right side view thereof;
FIG. 5 is a top view thereof;
FIG. 6 is a bottom view thereof;
FIG. 7 is a front, right, and bottom perspective view thereof;
FIG. 8 is a rear, left, and top perspective view thereof; and,
FIG. 9 is a cross-sectional view taken along line 9-9 of FIG. 1.

The ornamental design of the present disclosure is a semiconductor module on which power semiconductor elements and the like may be mounted. Plate shaped terminals are provided on the left side and right side. A plurality of post shaped pins extend from a rear surface. The cross-sections of the post shaped pins are rhombic. A hole penetrates from a front surface to the rear surface at each of four corners of the semiconductor module.

The broken lines shown in the drawing views of FIGS. 1-8 form no part of the claimed design.

1 Claim, 9 Drawing Sheets

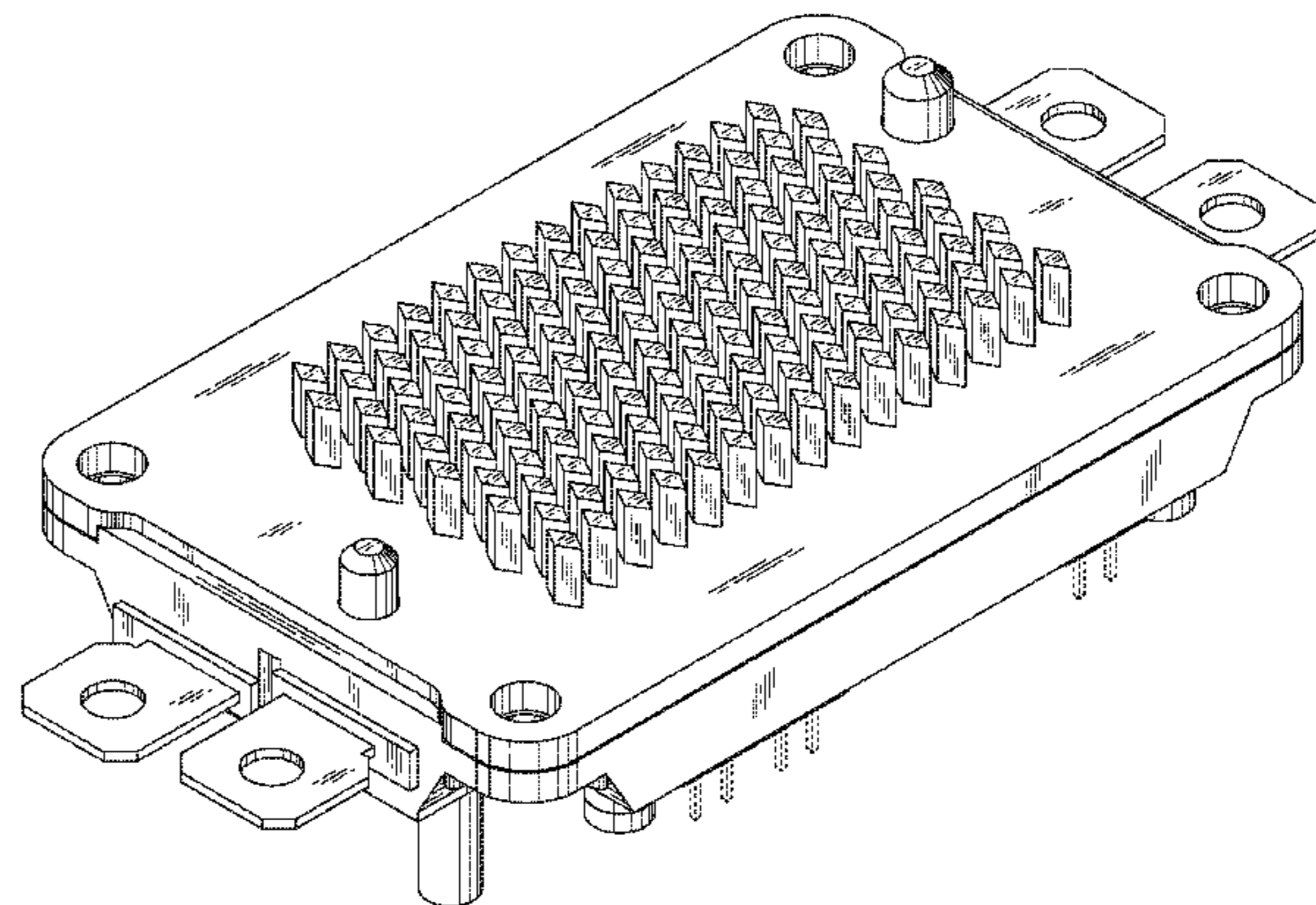
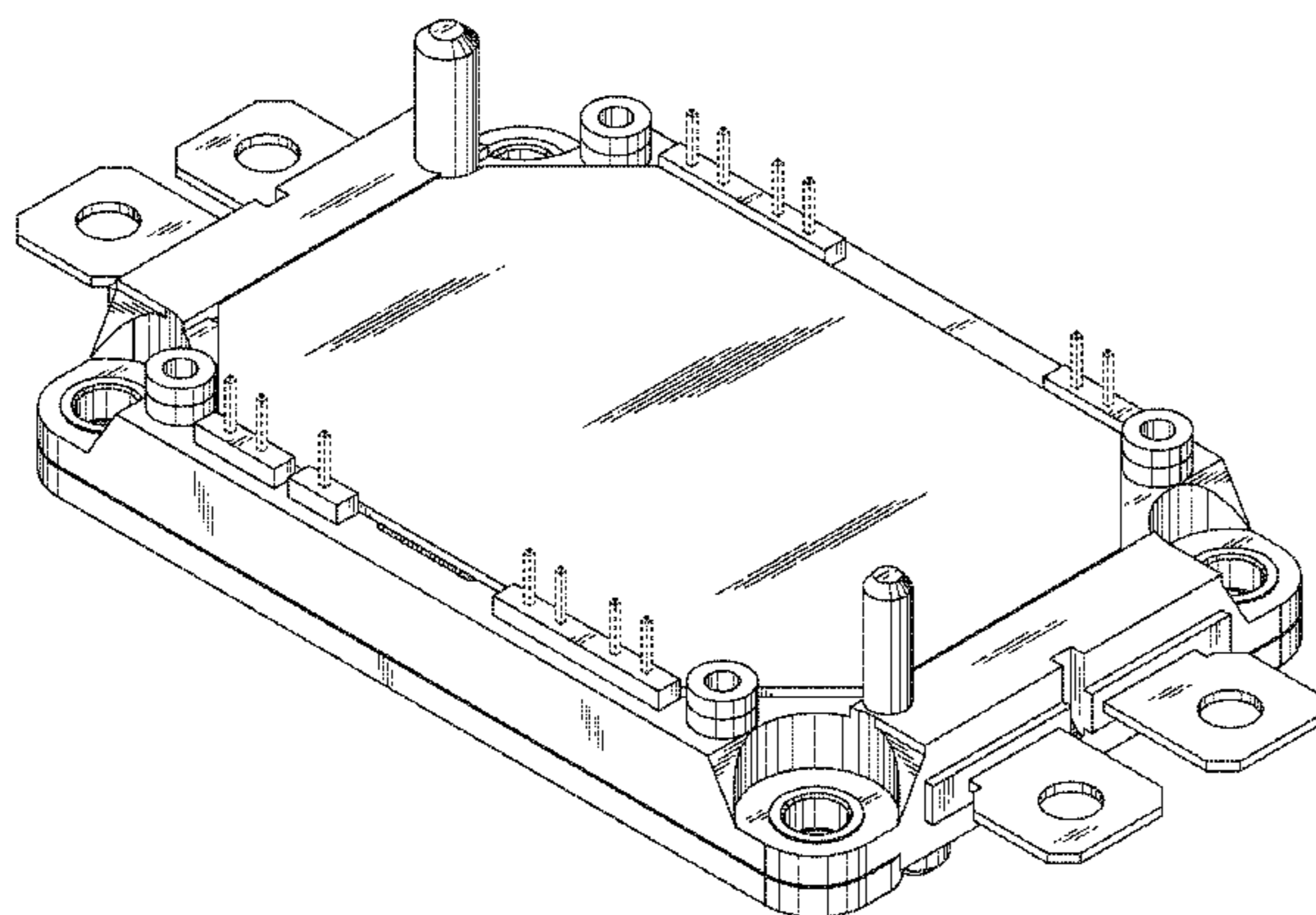


FIG. 1

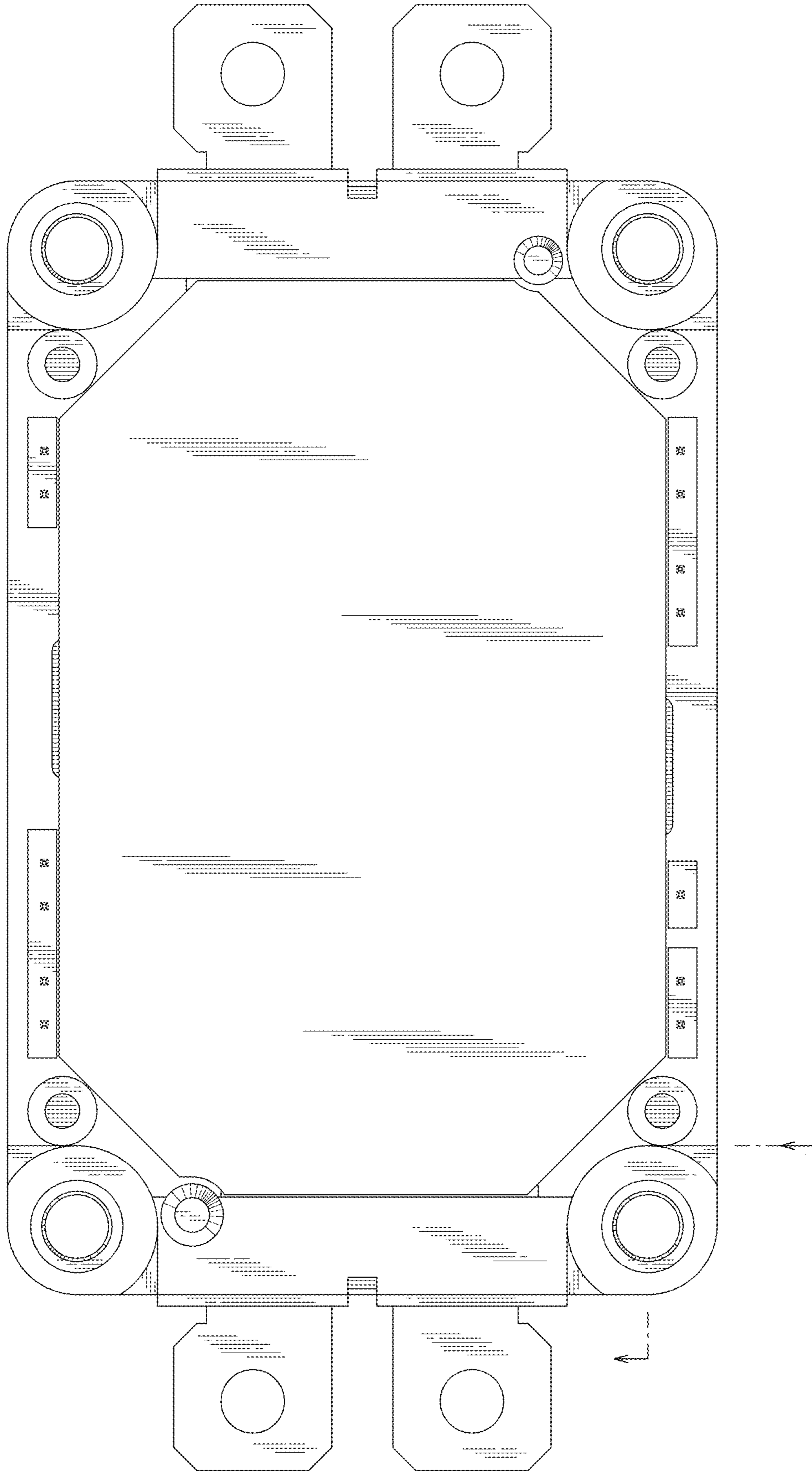


FIG. 2

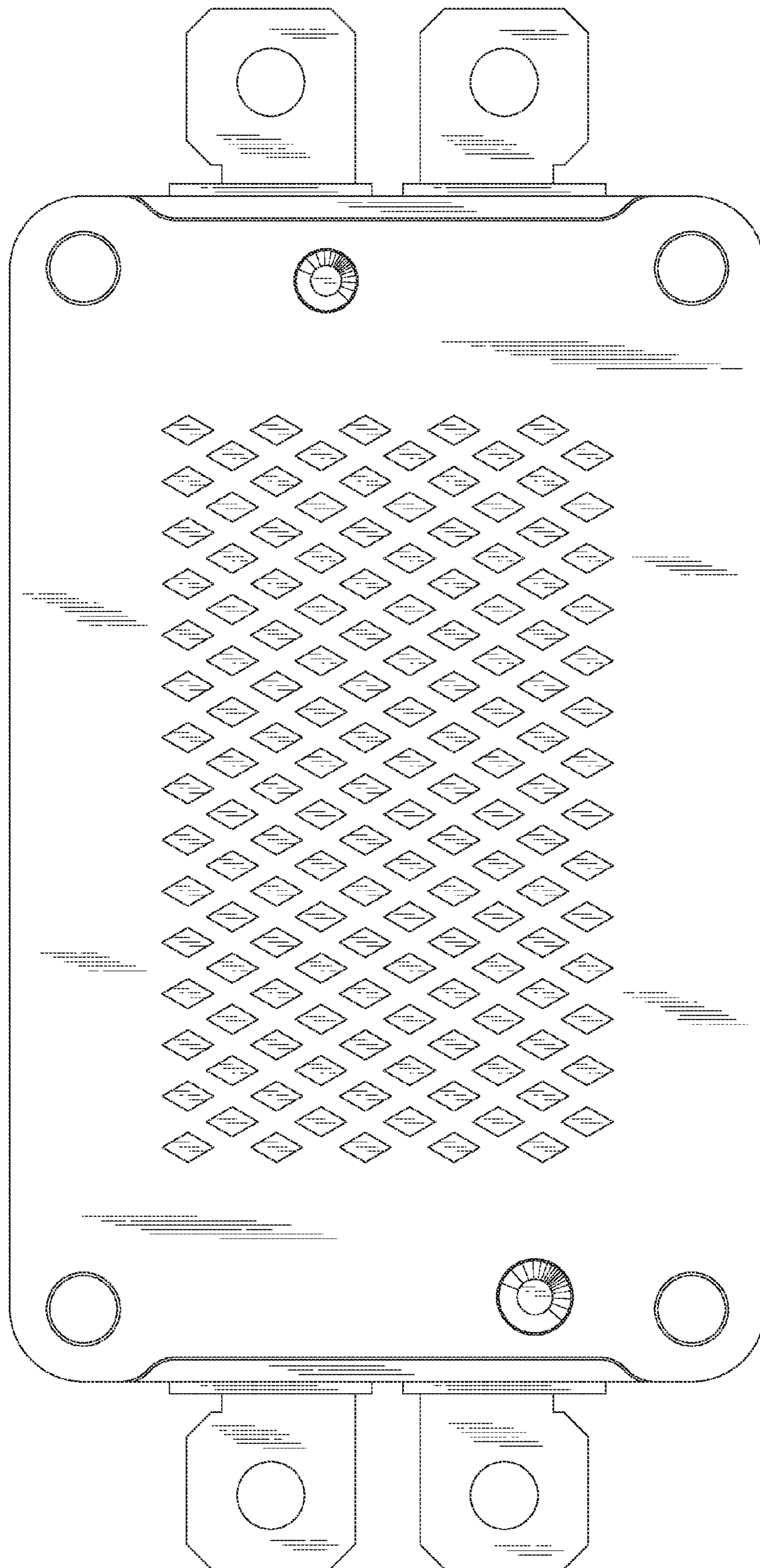


FIG. 3

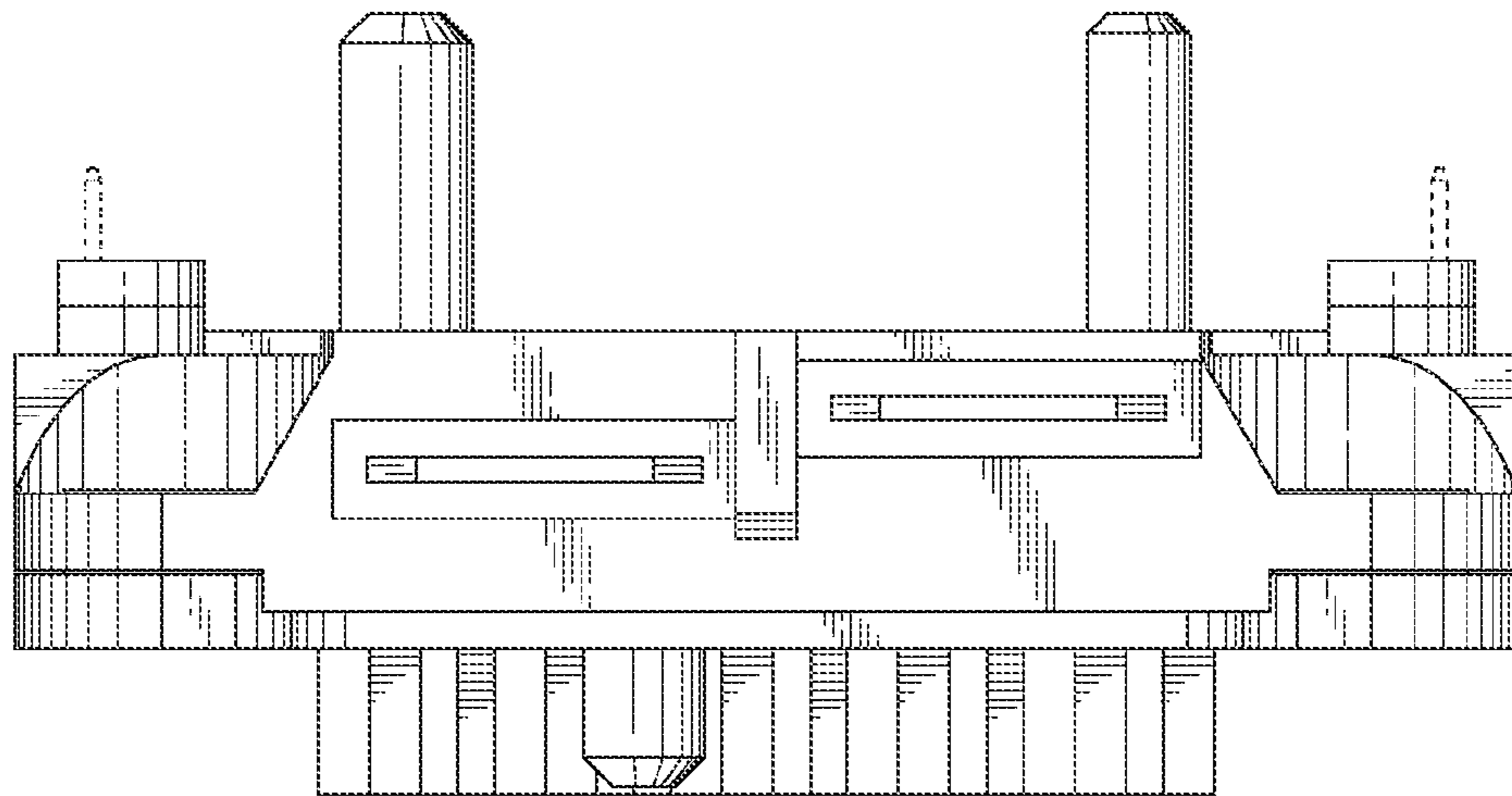


FIG. 4

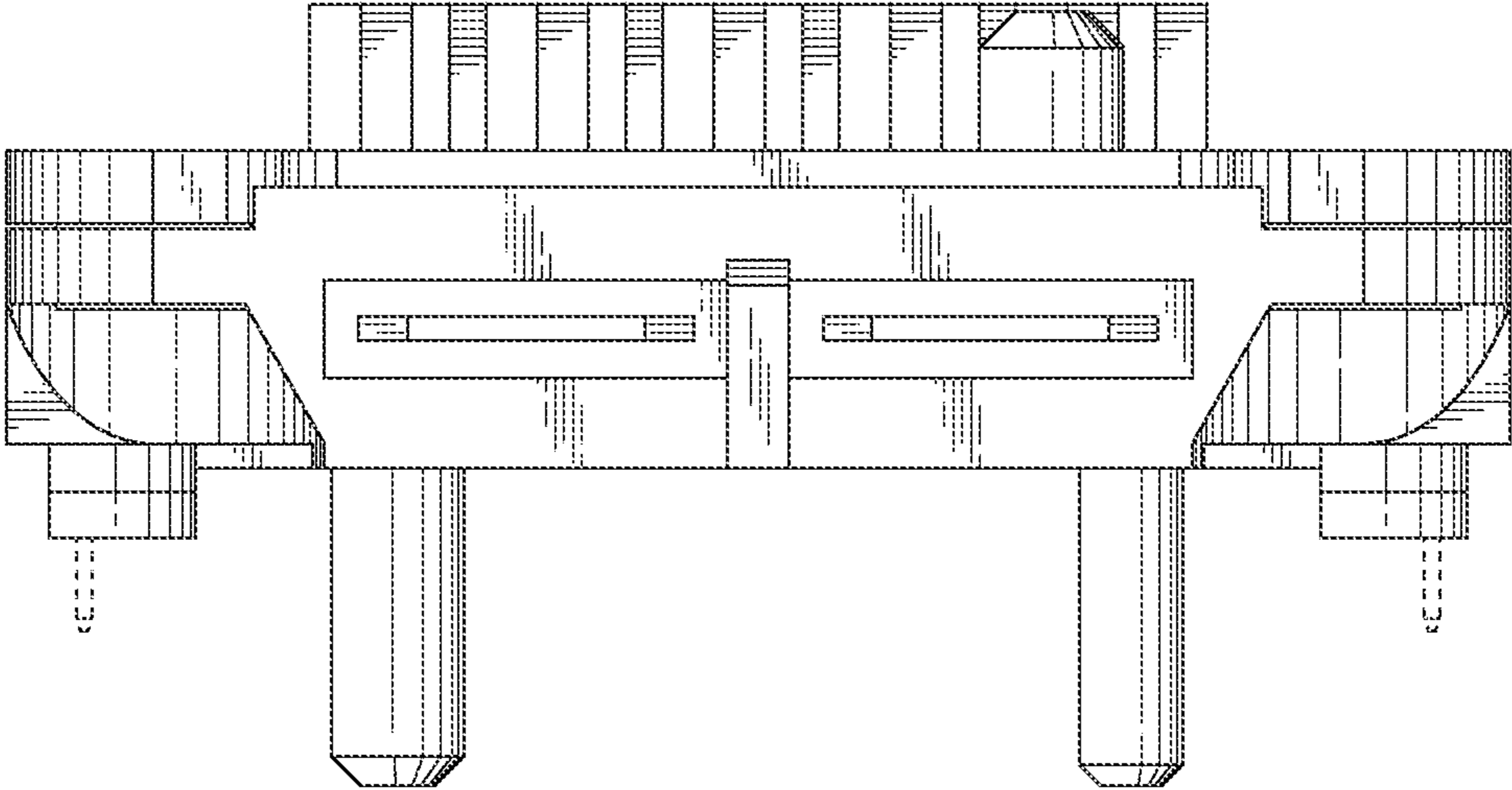


FIG. 5

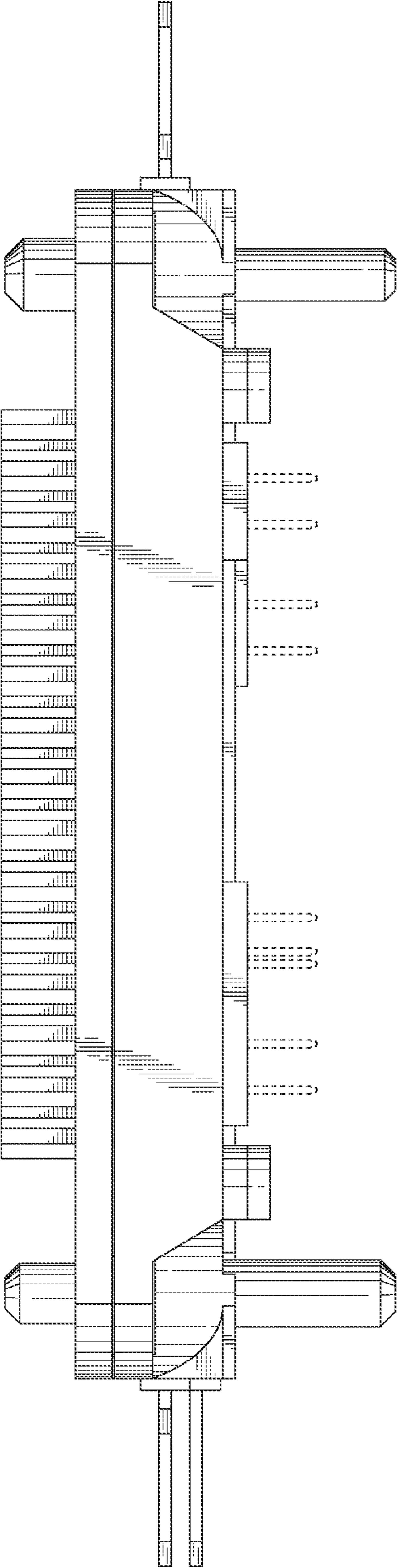


FIG. 6

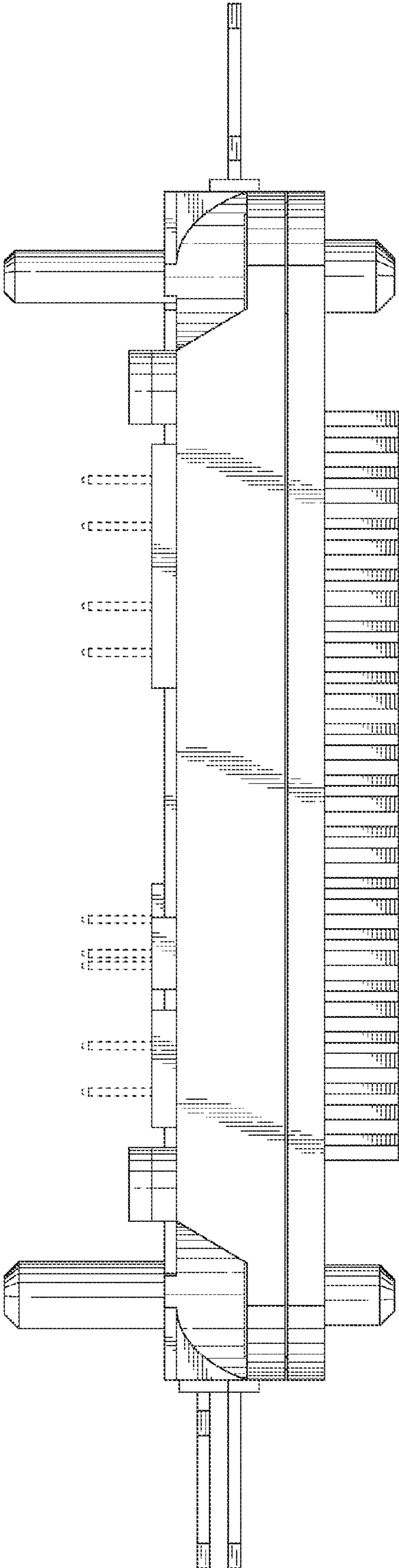
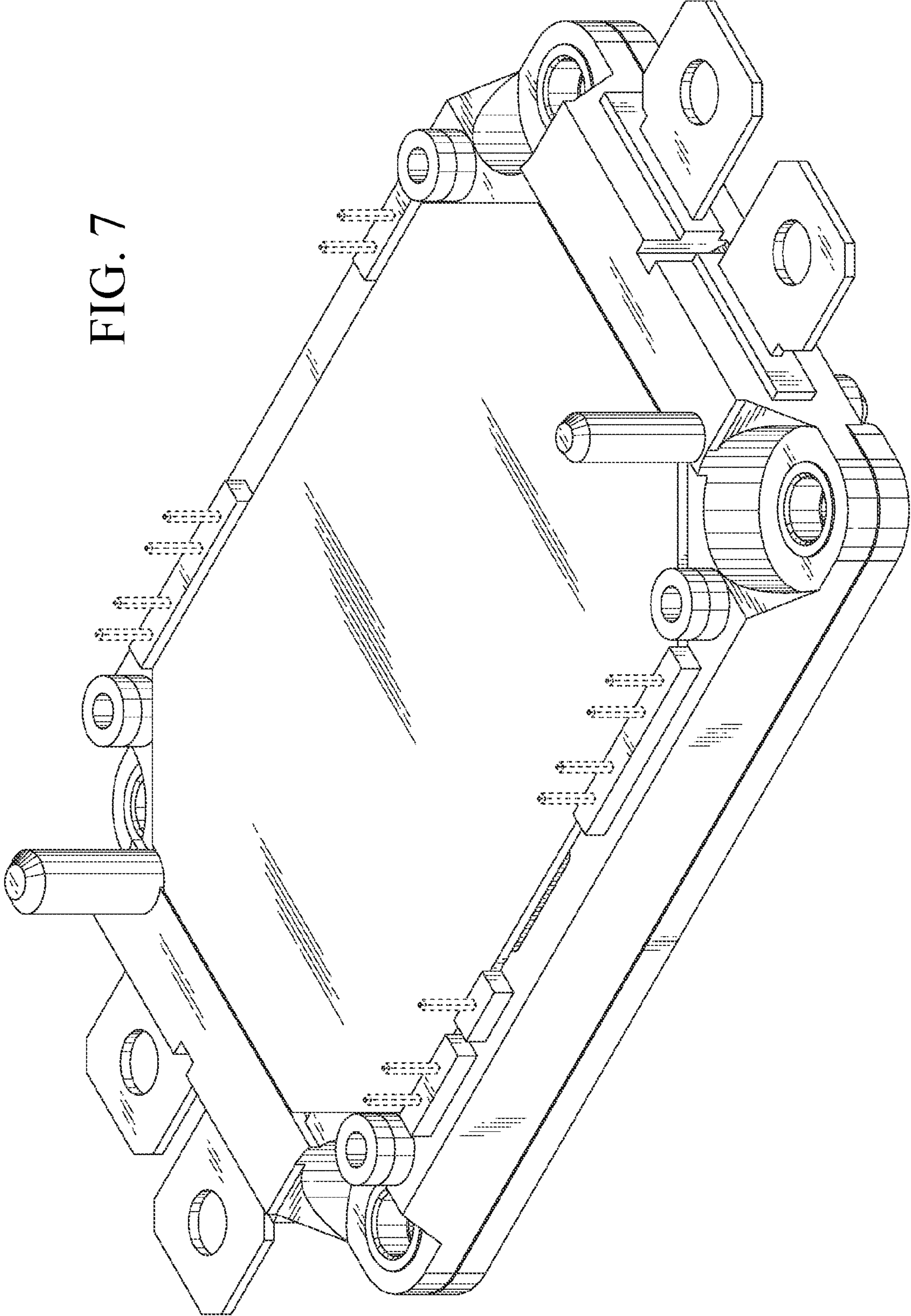


FIG. 7



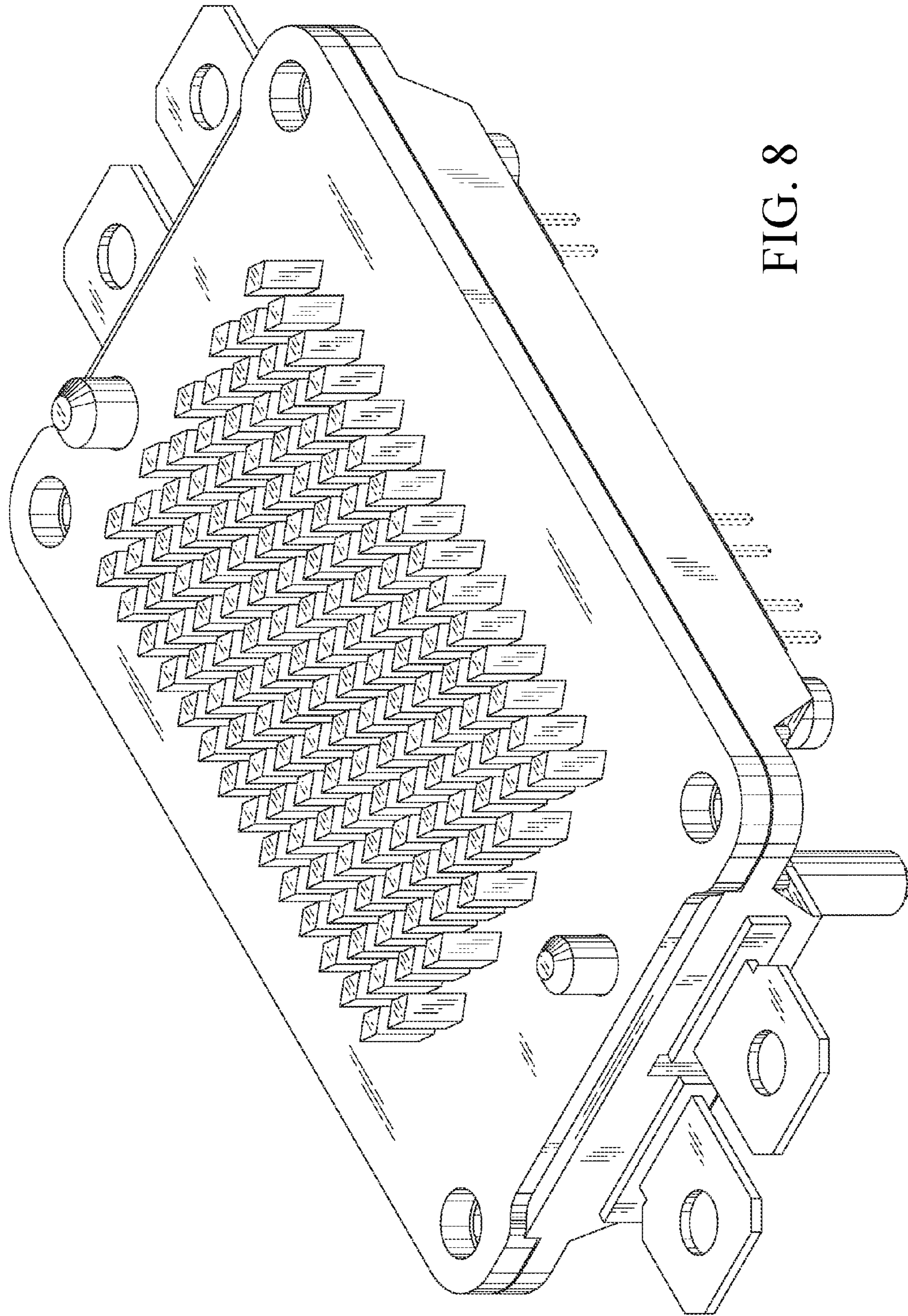


FIG. 8

FIG. 9

