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(12) **United States Design Patent**
Nakano et al.

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- (54) **INTEGRATED CIRCUIT TAG**
- (71) Applicant: **NOK CORPORATION**, Tokyo (JP)
- (72) Inventors: **Tomoko Nakano**, Kanagawa (JP);
Naohiro Fujisawa, Kanagawa (JP);
Keiichi Miyajima, Kanagawa (JP)
- (73) Assignee: **NOK Corporation**, Tokyo (JP)
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- (30) **Foreign Application Priority Data**

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(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

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D11/222; D20/22, 28

CPC .. H01L 21/6831; G06K 19/06; G06K 19/07;
G06K 19/07749; G06K 19/07745; G06K
19/07747; G06K 19/04; G06K 19/041;
G06K 19/044; G06K 19/07758; B65D
2203/10; G08B 13/2402; G08B 13/2405;
G08B 13/2428; G08B 13/2431; G08B
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G08B 13/2442; G08B 13/2445

See application file for complete search history.

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Primary Examiner — Elizabeth J Oswecki

(74) *Attorney, Agent, or Firm* — Michael Best &
Friedrich LLP

(57) **CLAIM**

The ornamental design for an integrated circuit tag, as shown and described.

DESCRIPTION

FIG. 1 is a perspective view of an integrated circuit tag showing our new design;

FIG. 2 is a front elevational view thereof;

FIG. 3 is a right side elevational view thereof;

FIG. 4 is a left side elevational view thereof;

FIG. 5 is a top plan view thereof; and

FIG. 6 is a bottom plan view thereof.

FIG. 7 is a reference front elevational view thereof;

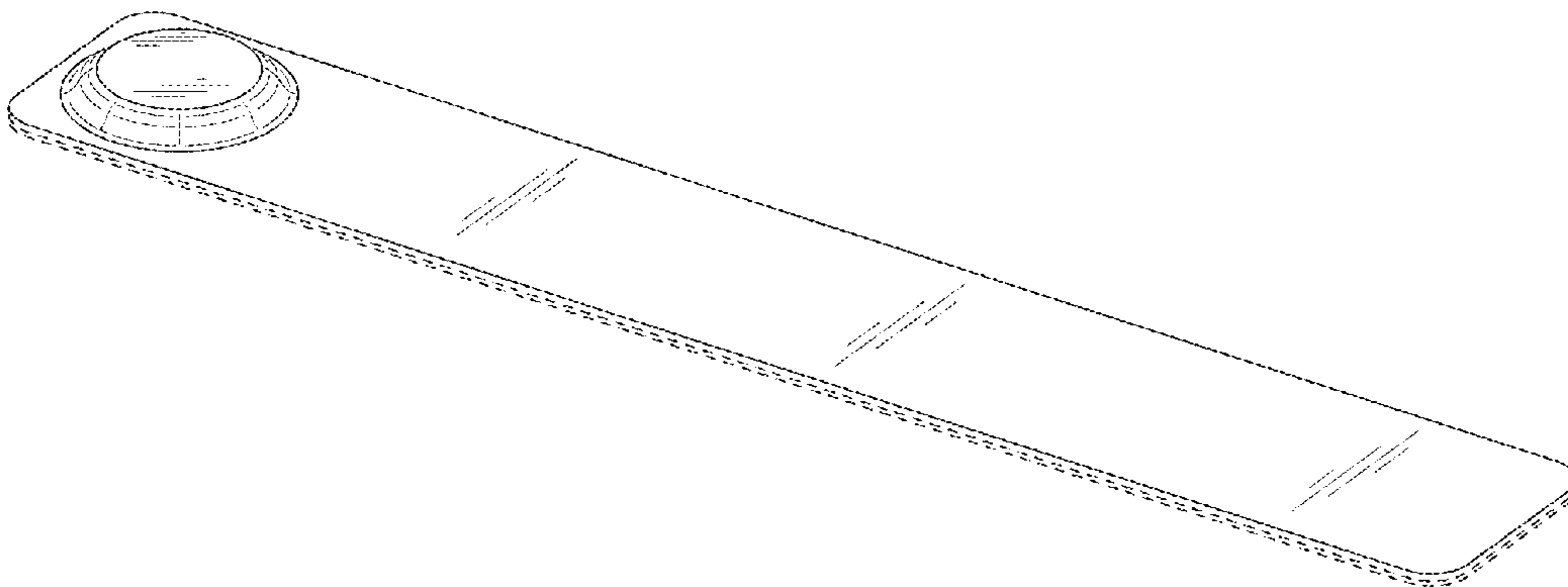
FIG. 8 is a reference rear elevational view thereof;

FIG. 9 is a cross sectional view thereof cut along the line 9-9 of FIG. 7; and,

FIG. 10 is a reference rear elevational view thereof showing the translucent portion in gray.

The broken lines shown in the drawings represent portions of the integrated circuit tag that form no part of the claimed design.

1 Claim, 5 Drawing Sheets



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FIG.1

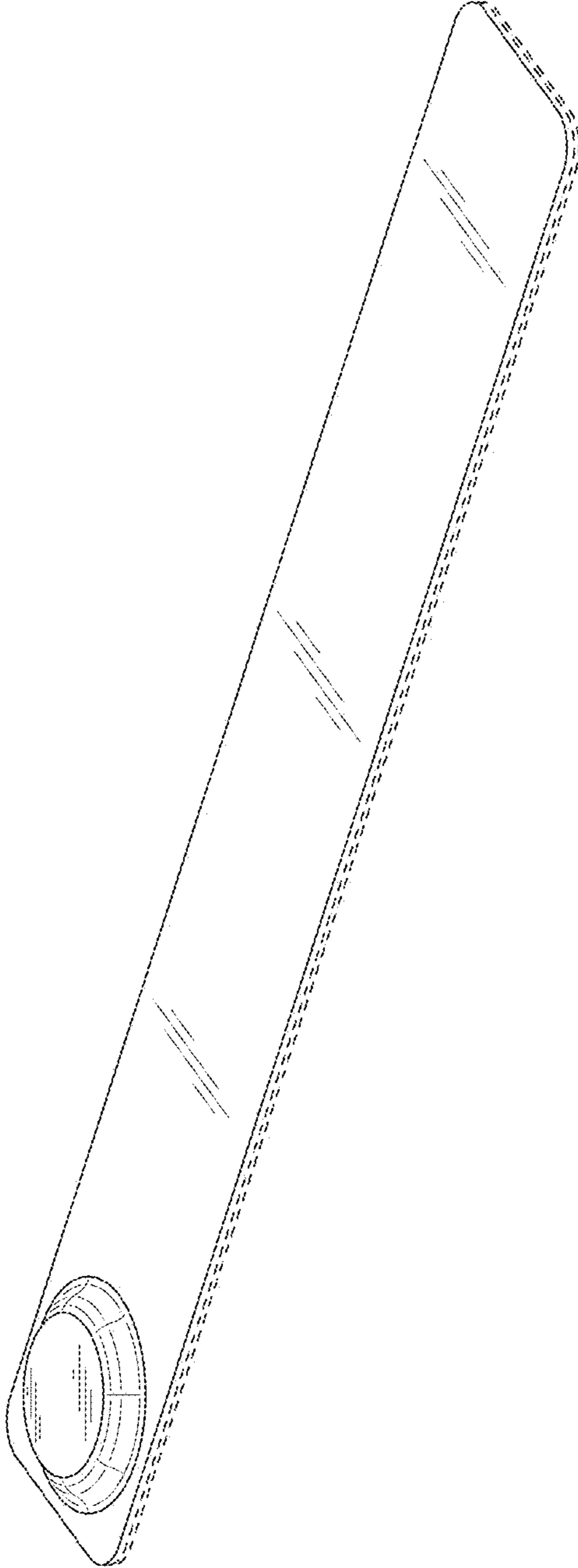


FIG.2

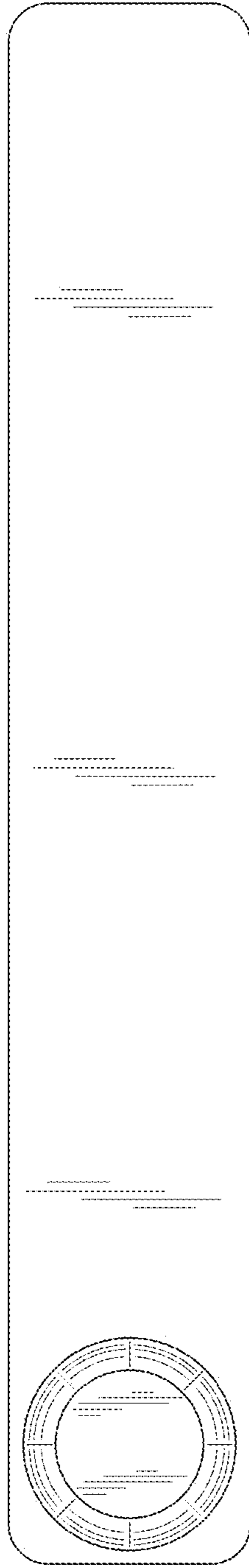


FIG.3

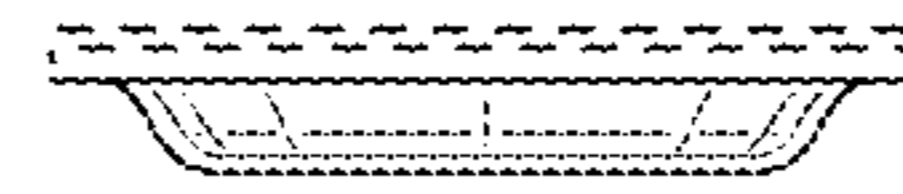


FIG.4

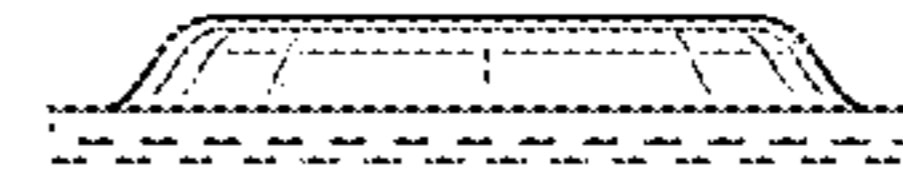


FIG.5



FIG.6

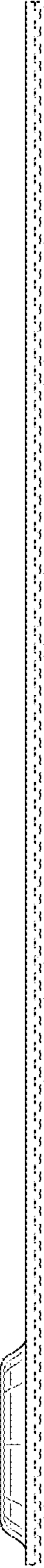


FIG.7

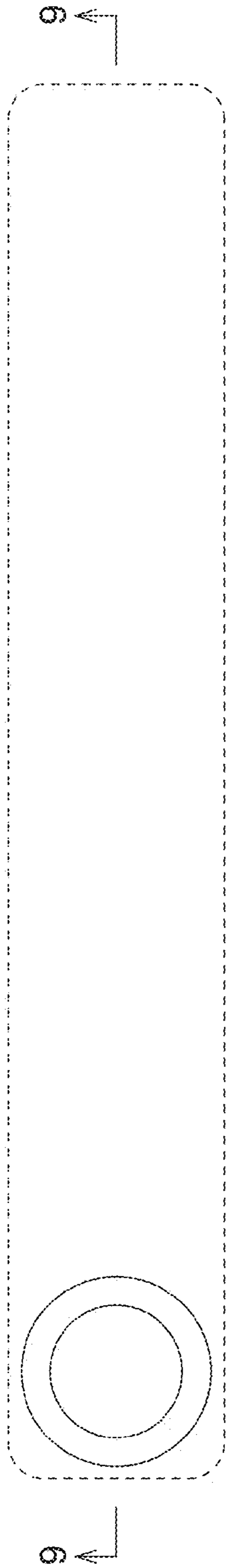


FIG.8

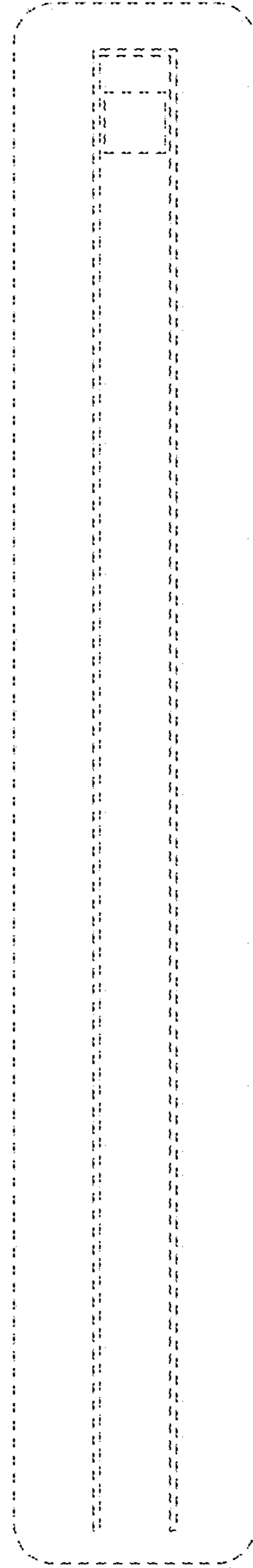


FIG.9



FIG.10

