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Fukushima et al.

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(54) **ELASTIC MEMBRANE FOR SEMICONDUCTOR WAFER POLISHING APPARATUS**

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(**) Term: **14 Years**

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Related U.S. Application Data

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Nov. 11, 2013 (JP) 2013-026349

(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182; 451/66, 288, 289
CPC B24B 37/30; B24B 41/061; B24B 49/16
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,659,850 B2 * 12/2003 Korovin B24B 37/30 451/286
7,357,699 B2 * 4/2008 Togawa B24B 37/30 451/288

(Continued)

FOREIGN PATENT DOCUMENTS

CN 301348233 S 9/2010
CN 301445758 S 1/2011

(Continued)

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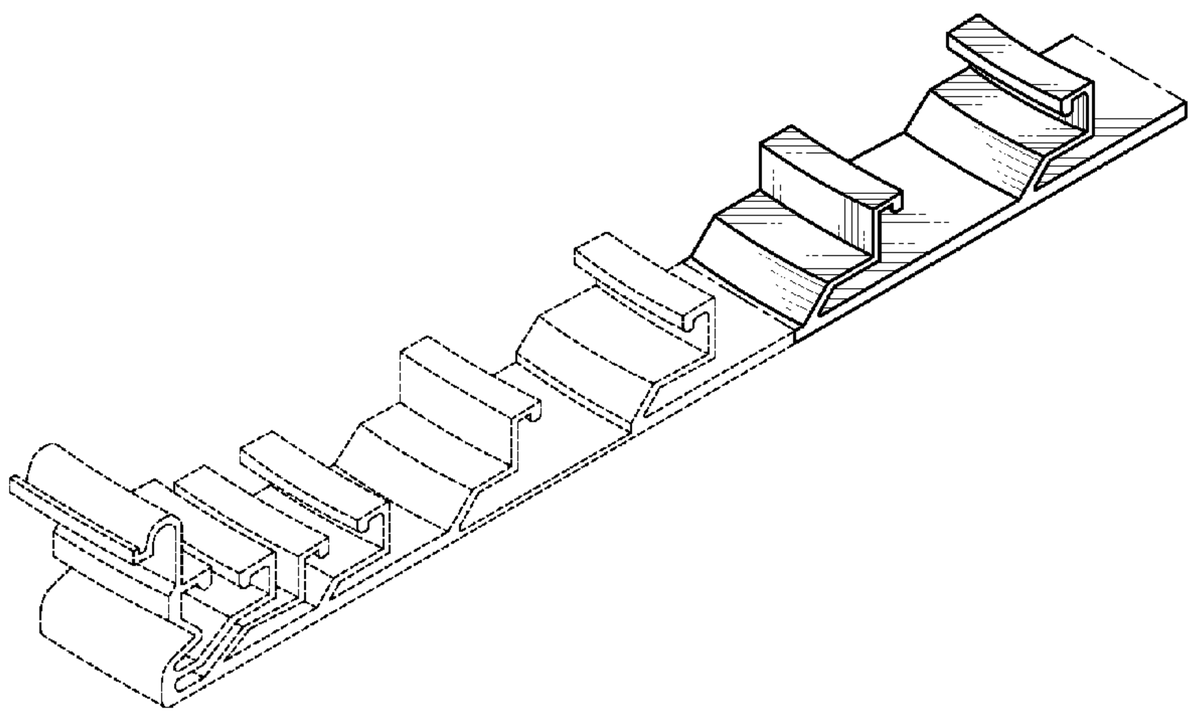
(57) **CLAIM**

The ornamental design for an elastic membrane for semiconductor wafer polishing apparatus, as shown and described.

DESCRIPTION

FIG. **1** is a bottom plan view of an elastic membrane for semiconductor wafer polishing apparatus showing our new design;
FIG. **2** is a top plan view thereof;
FIG. **3** is a front elevation view thereof;
FIG. **4** is an enlarged perspective view of a portion taken along section **4** in FIG. **2**;
FIG. **5** is a cross sectional view taken along line **5-5** in FIG. **2**; and,
FIG. **6** is an enlarged portion view taken along line **6-6** in FIG. **5**.
The broken lines shown in the drawings represent portions of the elastic membrane for semiconductor wafer polishing apparatus that form no part of the claimed design. The dashed-dot-dashed lines represent the boundary lines of the claimed design.
All surfaces not shown form no part of the claimed design.

1 Claim, 2 Drawing Sheets



(56) **References Cited**

U.S. PATENT DOCUMENTS

7,402,098	B2 *	7/2008	Severson	B24B 37/30 451/288
D616,390	S *	5/2010	Sato	D13/182
D633,452	S	3/2011	Namiki et al.	
D634,719	S	3/2011	Yasuda et al.	
D649,126	S *	11/2011	Takahashi	D13/182
D684,551	S *	6/2013	Nguyen	D13/182
8,469,776	B2 *	6/2013	Zuniga	B24B 37/30 428/119
D686,175	S *	7/2013	Gurary	D13/182
D686,582	S *	7/2013	Krishnan	D13/182
D687,790	S *	8/2013	Krishnan	D13/182
D687,791	S *	8/2013	Krishnan	D13/182
D711,330	S	8/2014	Fukushima et al.	
8,859,070	B2 *	10/2014	Yasuda	B32B 3/08 428/201
D729,753	S	5/2015	Fukushima et al.	
2001/0029158	A1 *	10/2001	Sasaki	B24B 37/14 451/66
2004/0175951	A1 *	9/2004	Chen	B24B 37/30 438/692
2008/0070479	A1 *	3/2008	Nabeya	B24B 37/30 451/8
2009/0068934	A1 *	3/2009	Hong	B24B 57/00 451/288
2009/0068935	A1 *	3/2009	Torii	B24B 37/345 451/331
2009/0111362	A1 *	4/2009	Nabeya	B24B 37/32 451/64
2009/0247057	A1 *	10/2009	Kobayashi	B24B 37/16 451/287
2013/0316628	A1 *	11/2013	Jang	B24B 37/30 451/398

FOREIGN PATENT DOCUMENTS

TW	D 138225	S	12/2010
TW	D 139857	S	4/2011
TW	D 146491	S	4/2012

* cited by examiner

FIG. 1

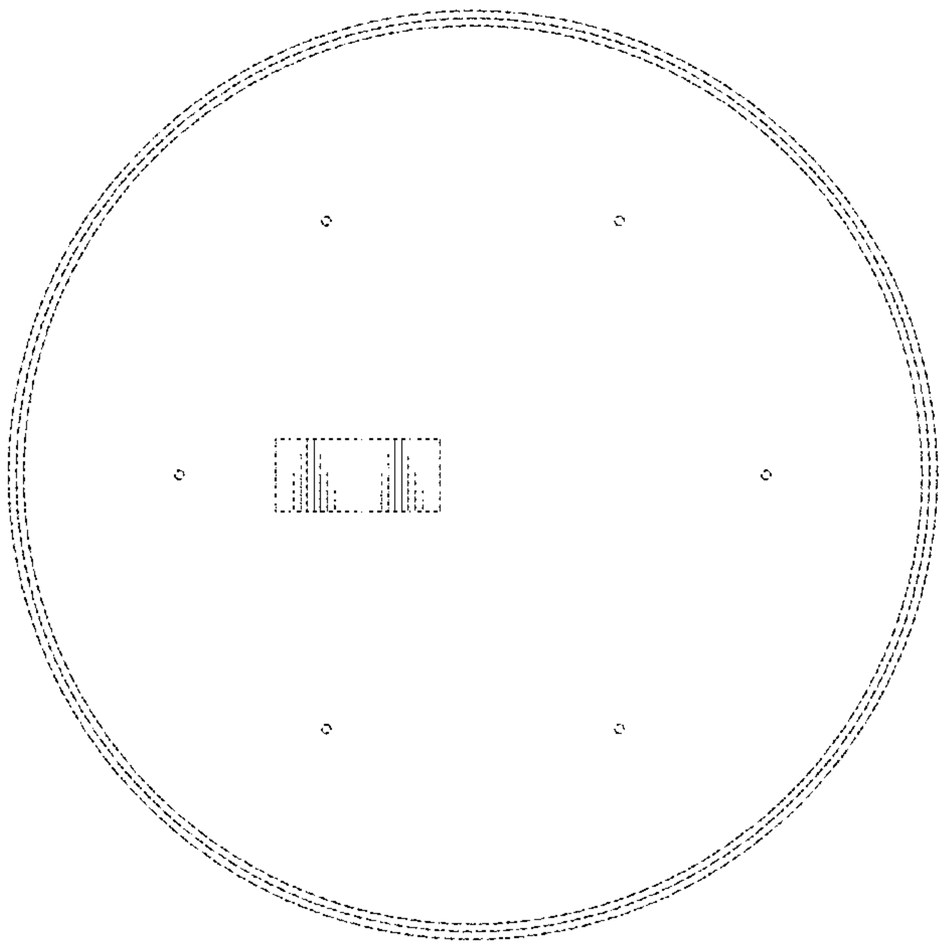


FIG. 2

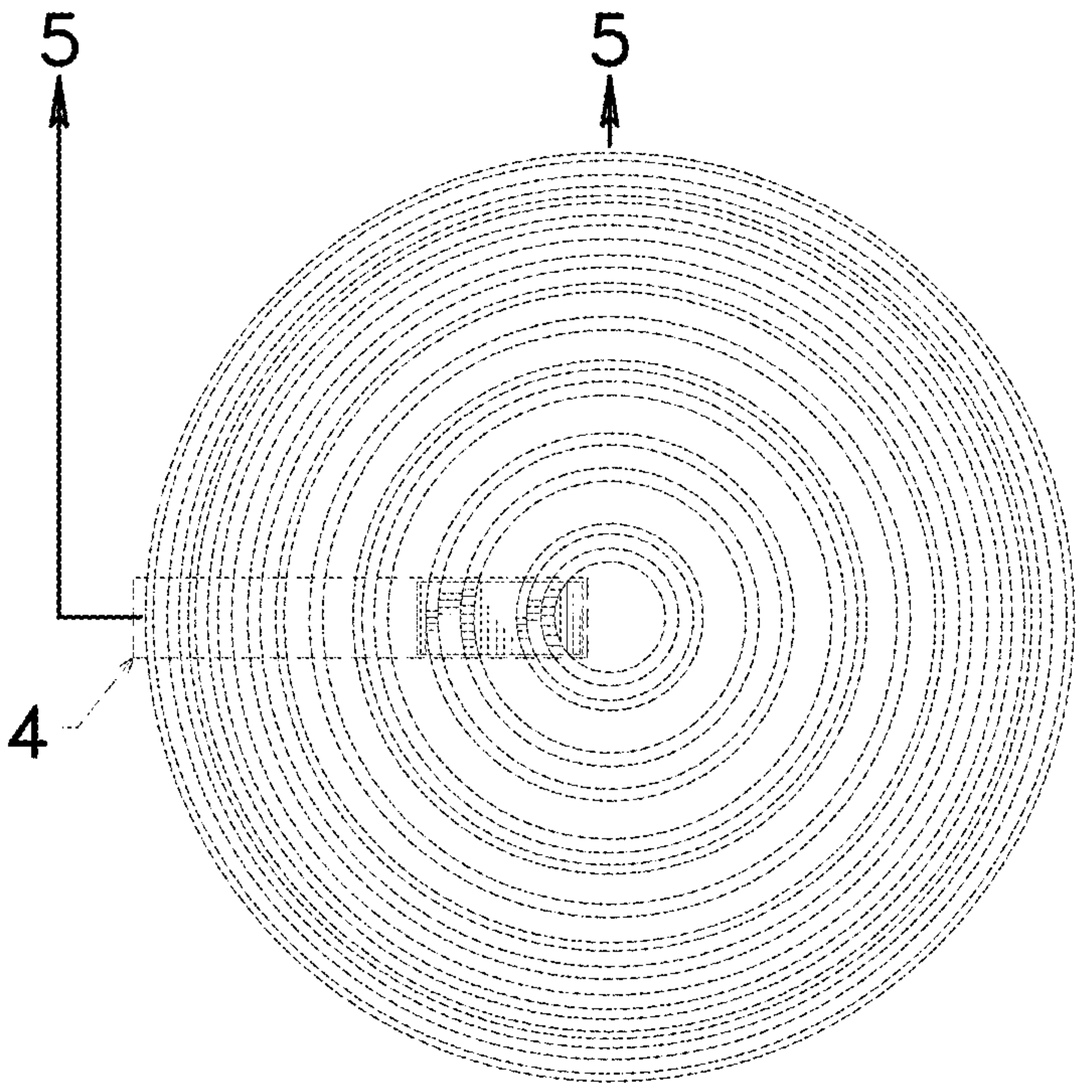


FIG. 3

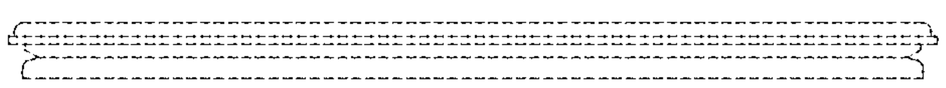


FIG.4

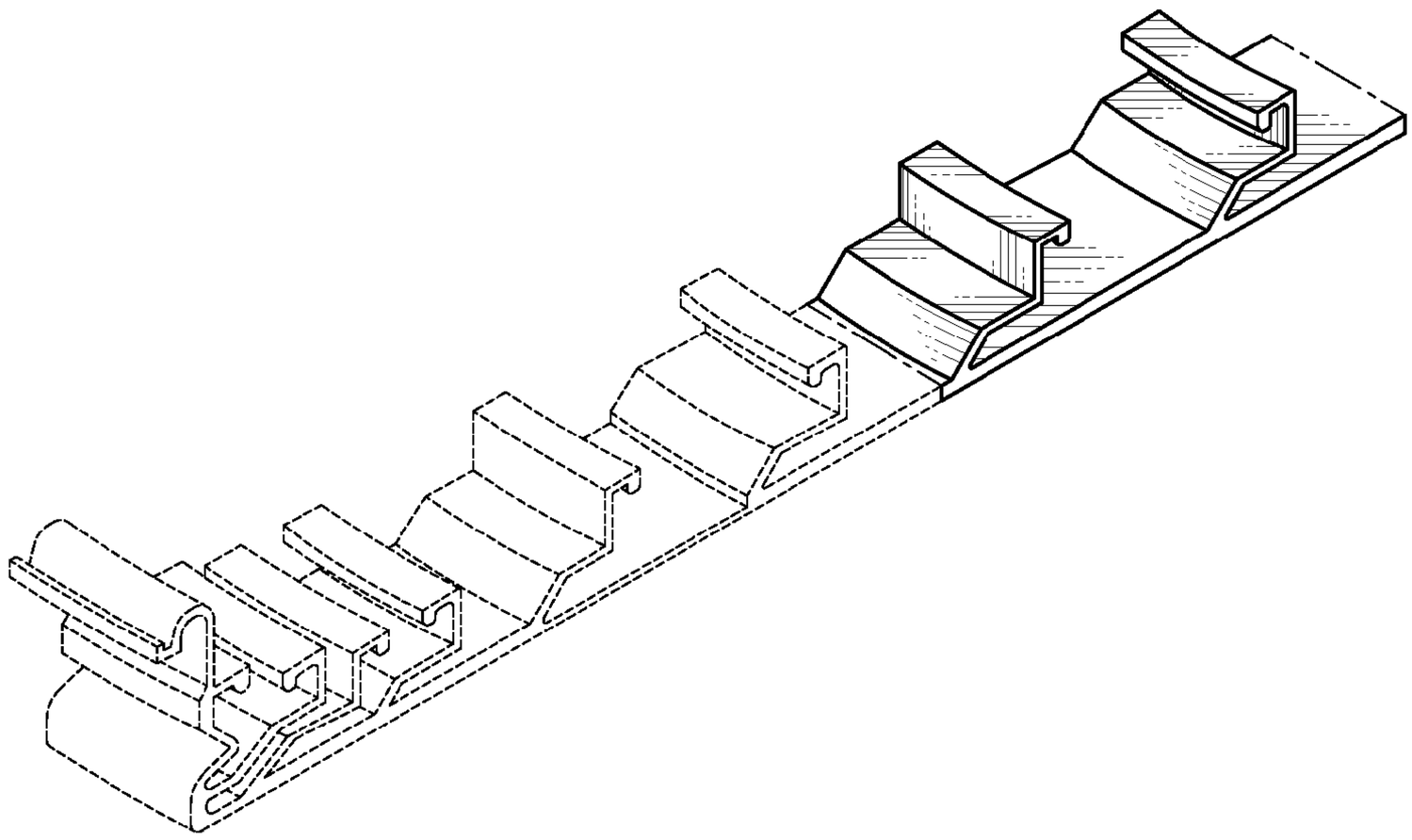


FIG.5

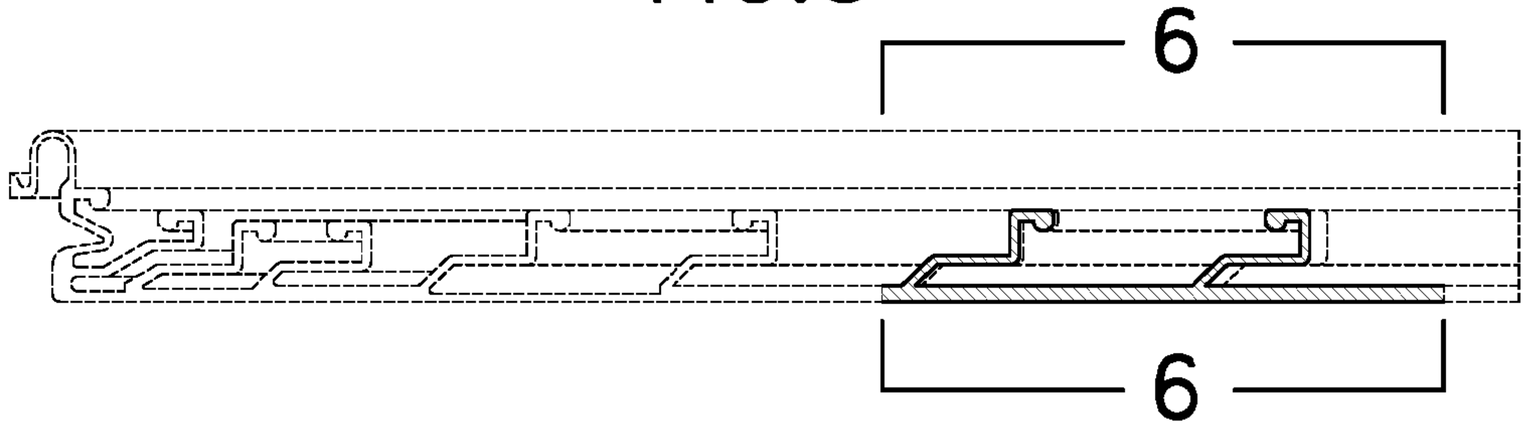


FIG.6