



US00D769200S

(12) **United States Design Patent** (10) **Patent No.:** **US D769,200 S**
Fukushima et al. (45) **Date of Patent:** **** Oct. 18, 2016**

(54) **ELASTIC MEMBRANE FOR SEMICONDUCTOR WAFER POLISHING APPARATUS**
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(73) Assignee: **EBARA CORPORATION**, Tokyo (JP)
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May 15, 2013 (JP) 2013-10678

(51) **LOC (10) Cl.** **13-03**
(52) **U.S. Cl.**
USPC **D13/182**
(58) **Field of Classification Search**
USPC D13/182; 451/66, 288, 289
CPC B24B 37/30; B24B 41/061; B24B 49/16
See application file for complete search history.

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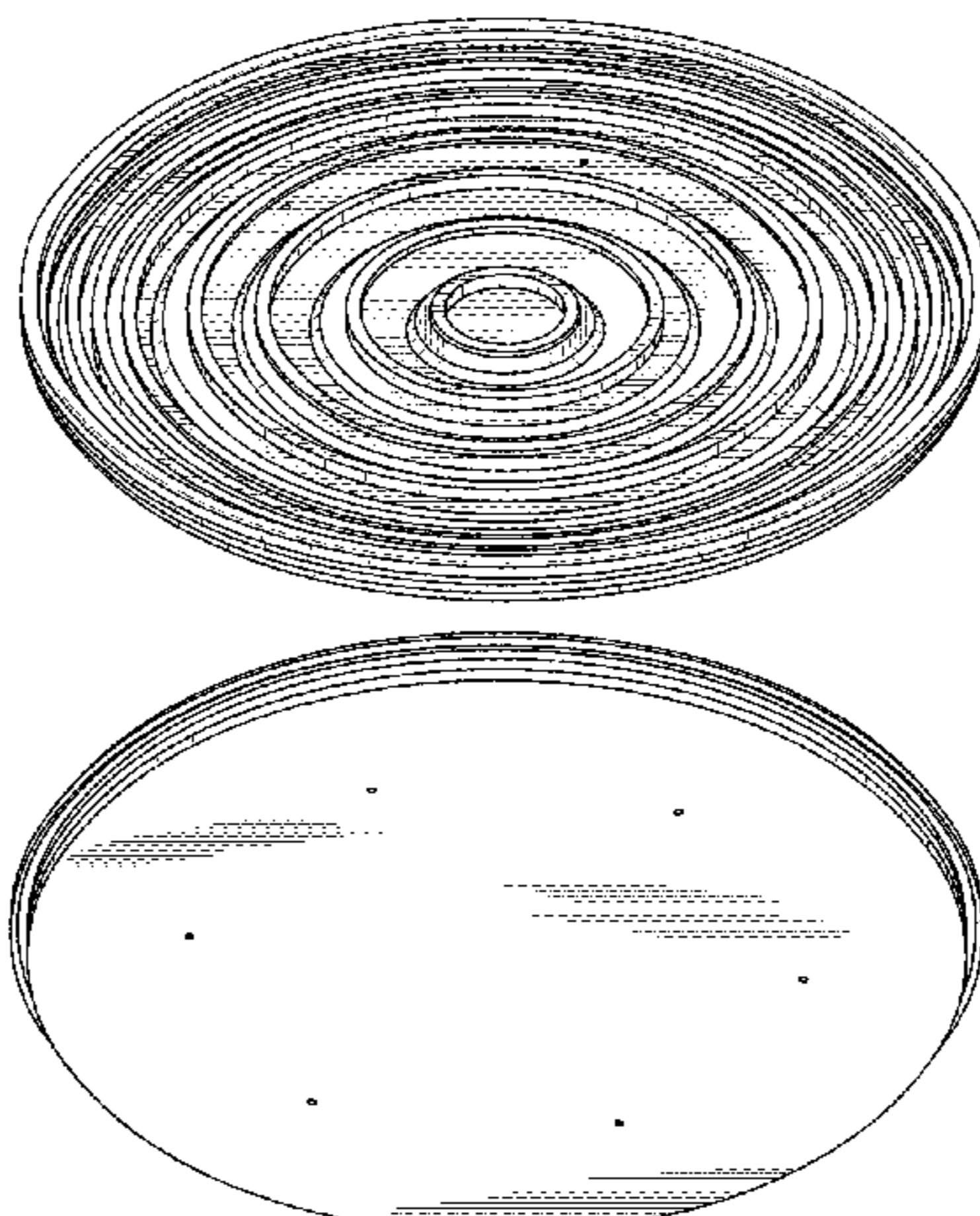
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Primary Examiner — Elizabeth J Oswecki

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(57) **CLAIM**

The ornamental design for an elastic membrane for semiconductor wafer polishing apparatus, as shown and described.



DESCRIPTION

FIG. 1 is a top perspective view a first embodiment of an elastic membrane for semiconductor wafer polishing apparatus showing our new design;
FIG. 2 is a bottom perspective view thereof;
FIG. 3 is a top plan view thereof;
FIG. 4 is a bottom plan view thereof;
FIG. 5 is a side view thereof, with the apparatus being radially symmetrical about a vertical axis;
FIG. 6 is a cross sectional view taken along section line 6-6 in FIG. 3;
FIG. 7 is an enlarged portion view taken along line 7-7 in FIG. 6;
FIG. 8 is a top perspective view a second embodiment of an elastic membrane for semiconductor wafer polishing apparatus showing our new design;
FIG. 9 is a bottom perspective view thereof;
FIG. 10 is a top plan view thereof;
FIG. 11 is a bottom plan view thereof;
FIG. 12 is a side view thereof, with the apparatus being radially symmetrical about a vertical axis;
FIG. 13 is a cross sectional view taken along section line 13-13 in FIG. 10;
FIG. 14 is an enlarged portion view taken along line 14-14 in FIG. 13;

FIG. 15 is a top perspective view a third embodiment of an elastic membrane for semiconductor wafer polishing apparatus showing our new design;
FIG. 16 is a bottom perspective view thereof;
FIG. 17 is a top plan view thereof;
FIG. 18 is a bottom plan view thereof;
FIG. 19 is a side view thereof, the apparatus being radially symmetrical about a vertical axis;
FIG. 20 is a cross sectional view taken along section line 20-20 in FIG. 17;
FIG. 21 is an enlarged portion view taken along line 21-21 in FIG. 20;
FIG. 22 is a top perspective view a fourth embodiment of an elastic membrane for semiconductor wafer polishing apparatus showing our new design;
FIG. 23 is a bottom perspective view thereof;
FIG. 24 is a top plan view thereof;
FIG. 25 is a bottom plan view thereof;
FIG. 26 is a side view thereof, the apparatus being radially symmetrical about a vertical axis;
FIG. 27 is a cross sectional view taken along line 27-27 in FIG. 24; and,
FIG. 28 is an enlarged portion view taken along line 28-28 in FIG. 27.
The broken lines shown in the drawings represent portions of the elastic membrane for semiconductor wafer polishing apparatus that form no part of the claimed design.

1 Claim, 16 Drawing Sheets

FIG. 1

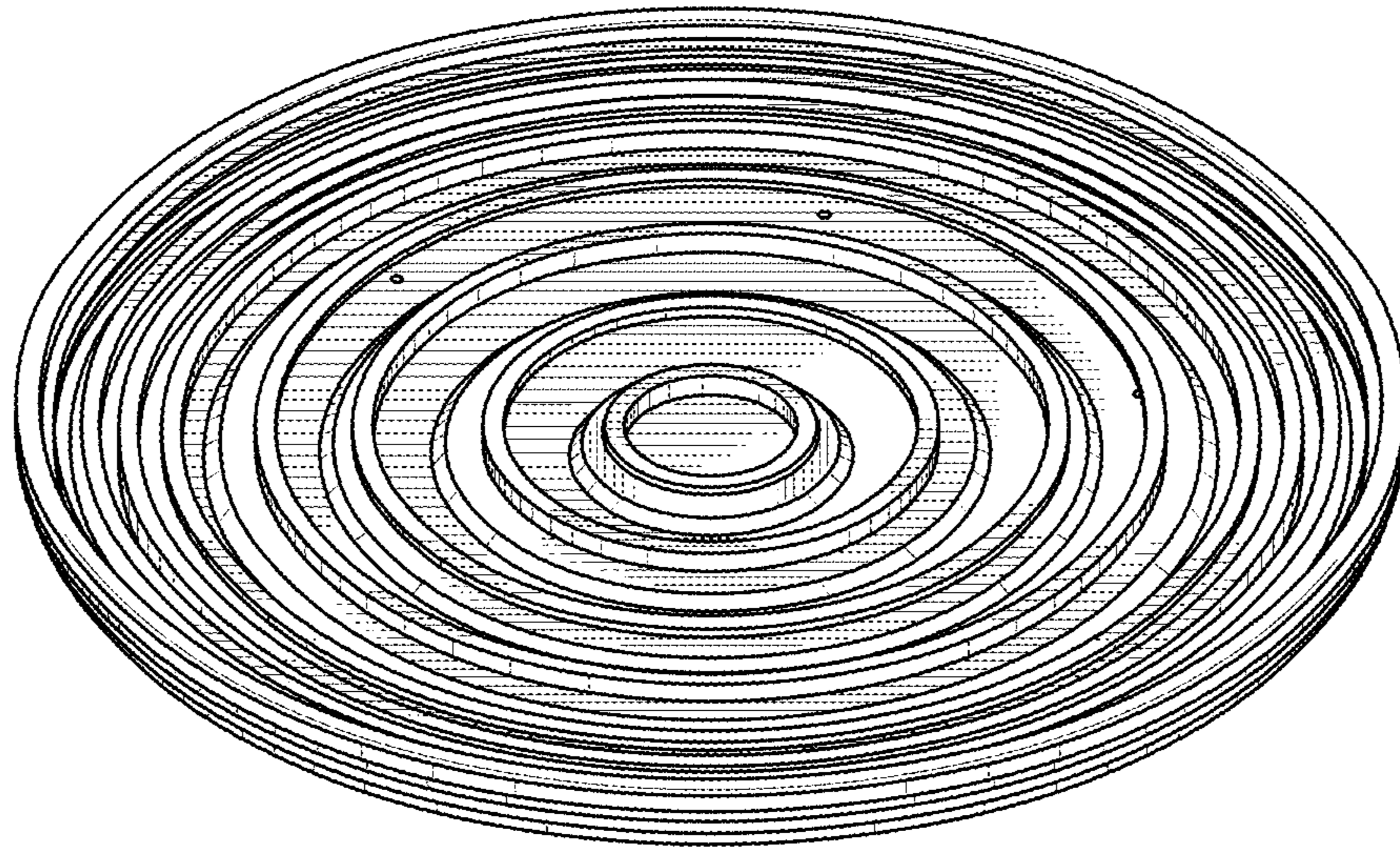


FIG. 2

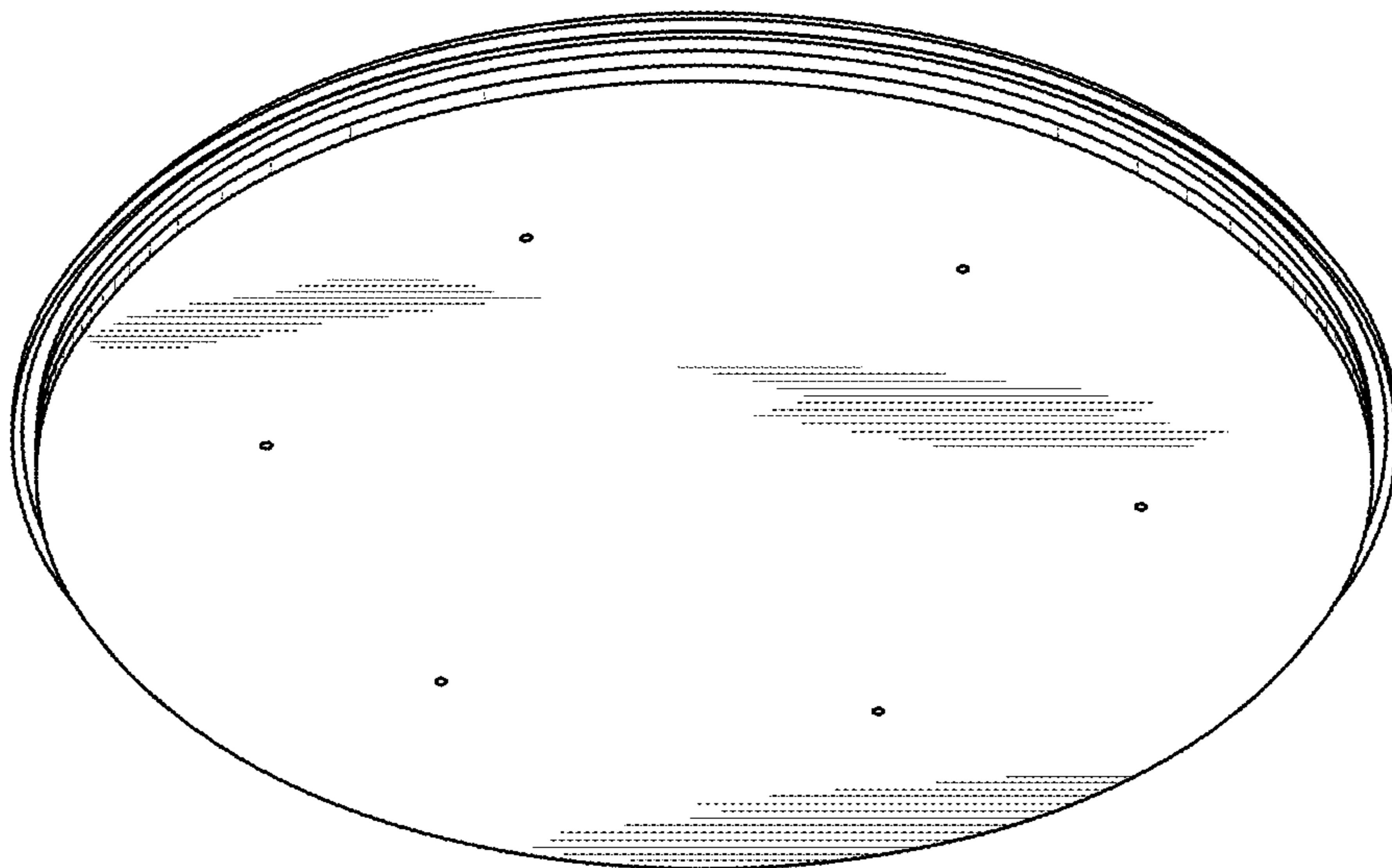


FIG. 3

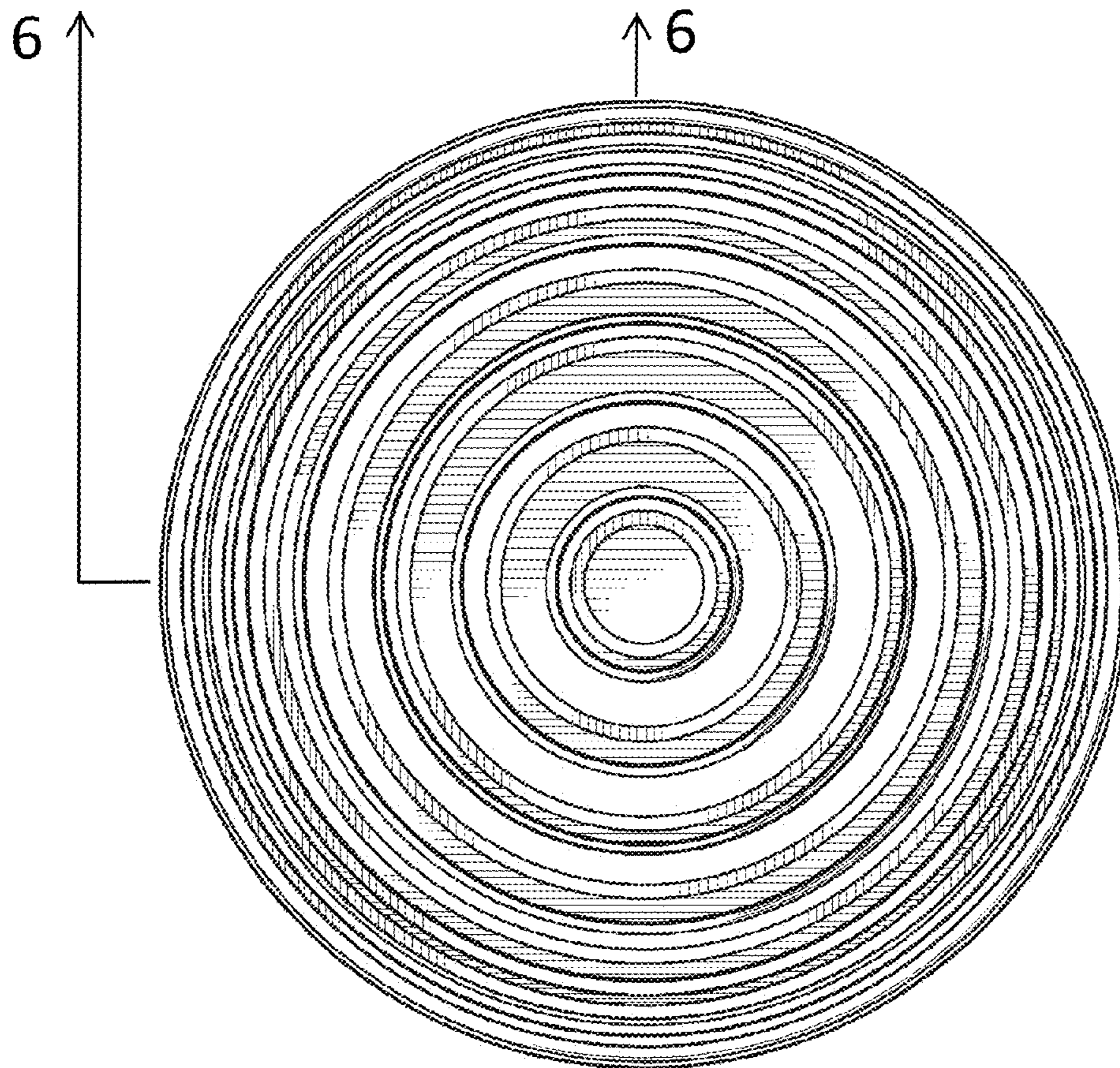


FIG. 4

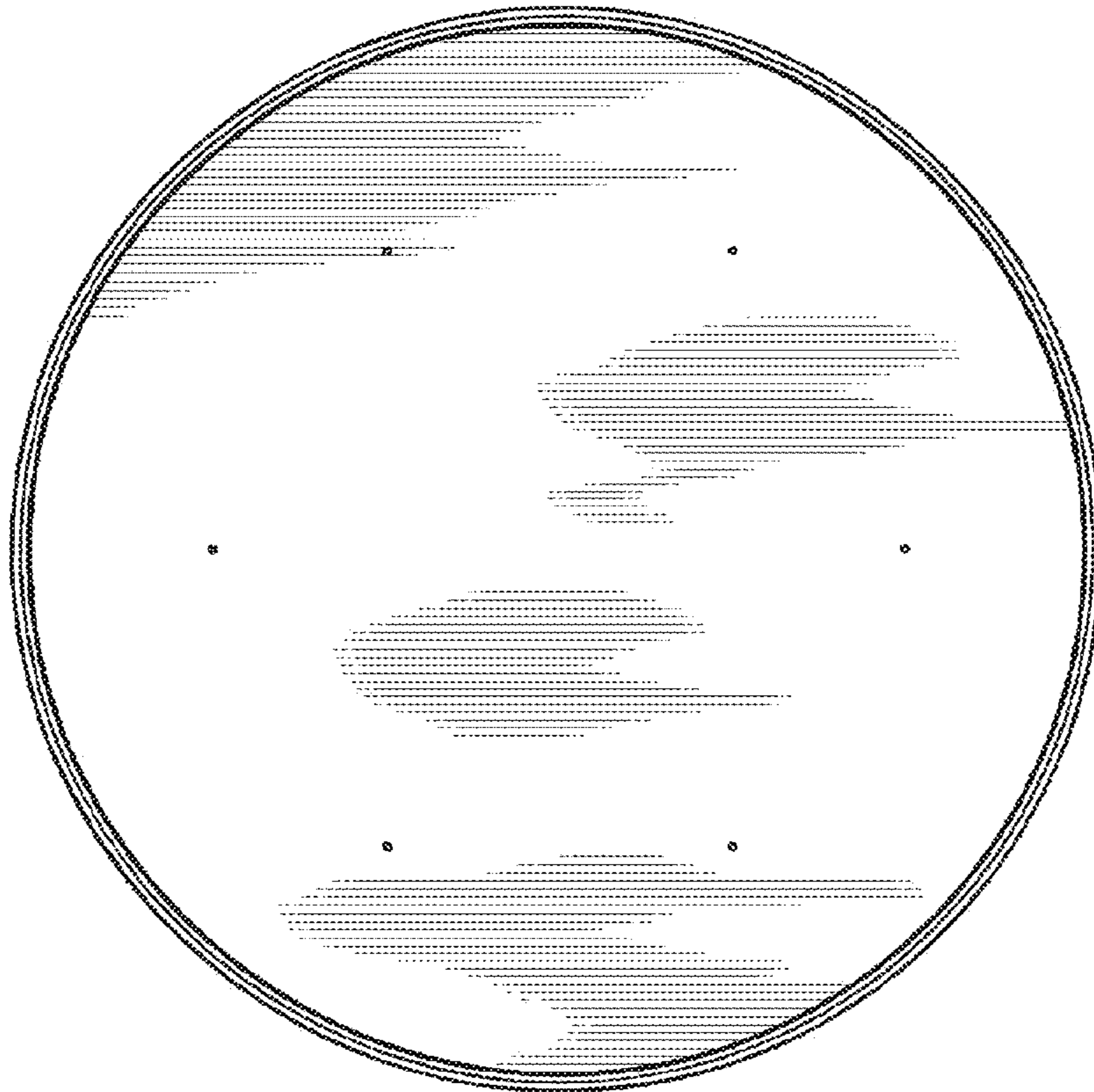


FIG. 5



FIG. 6

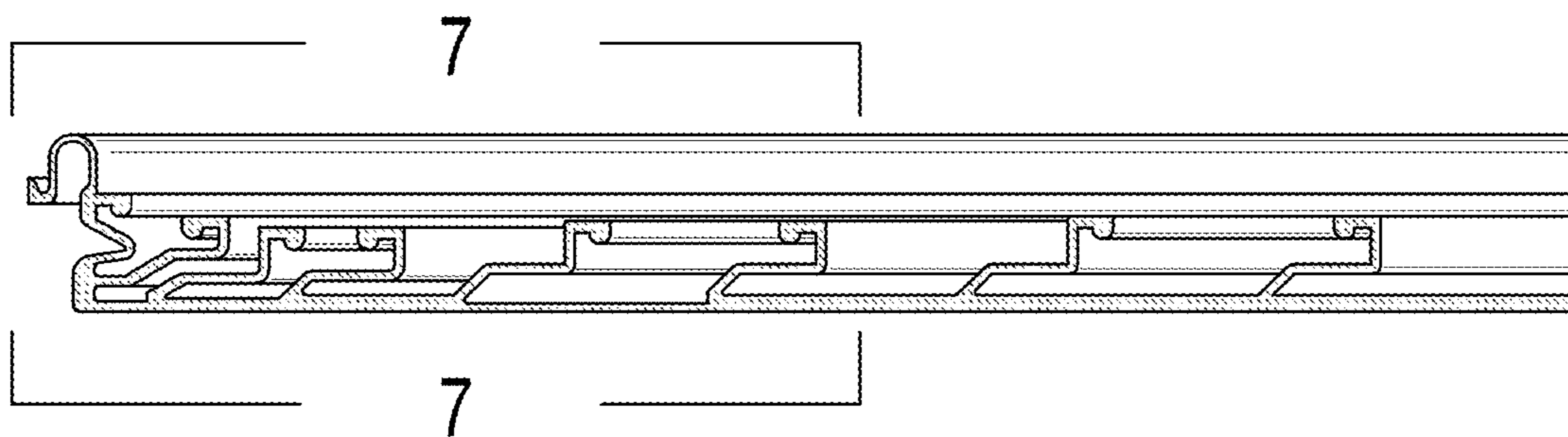


FIG. 7

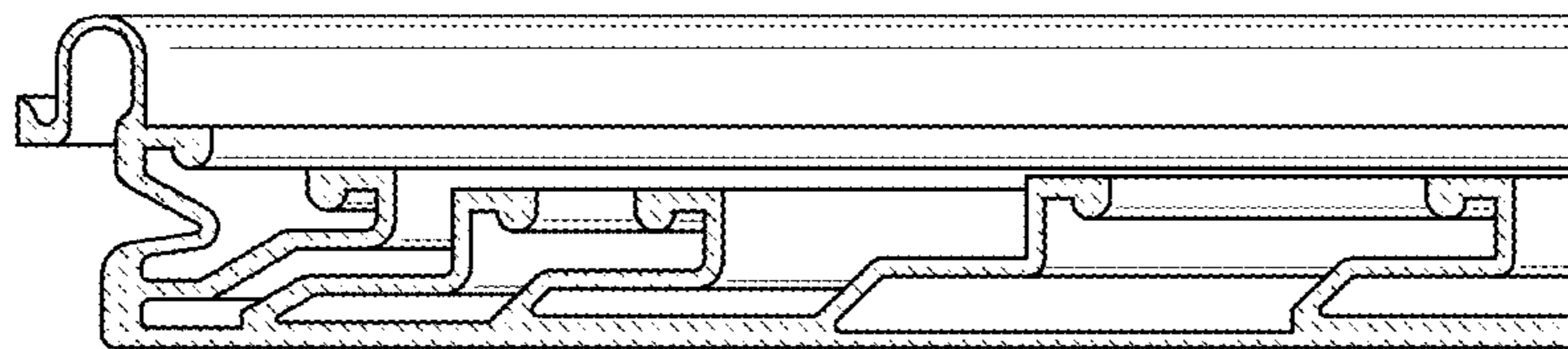


FIG. 8

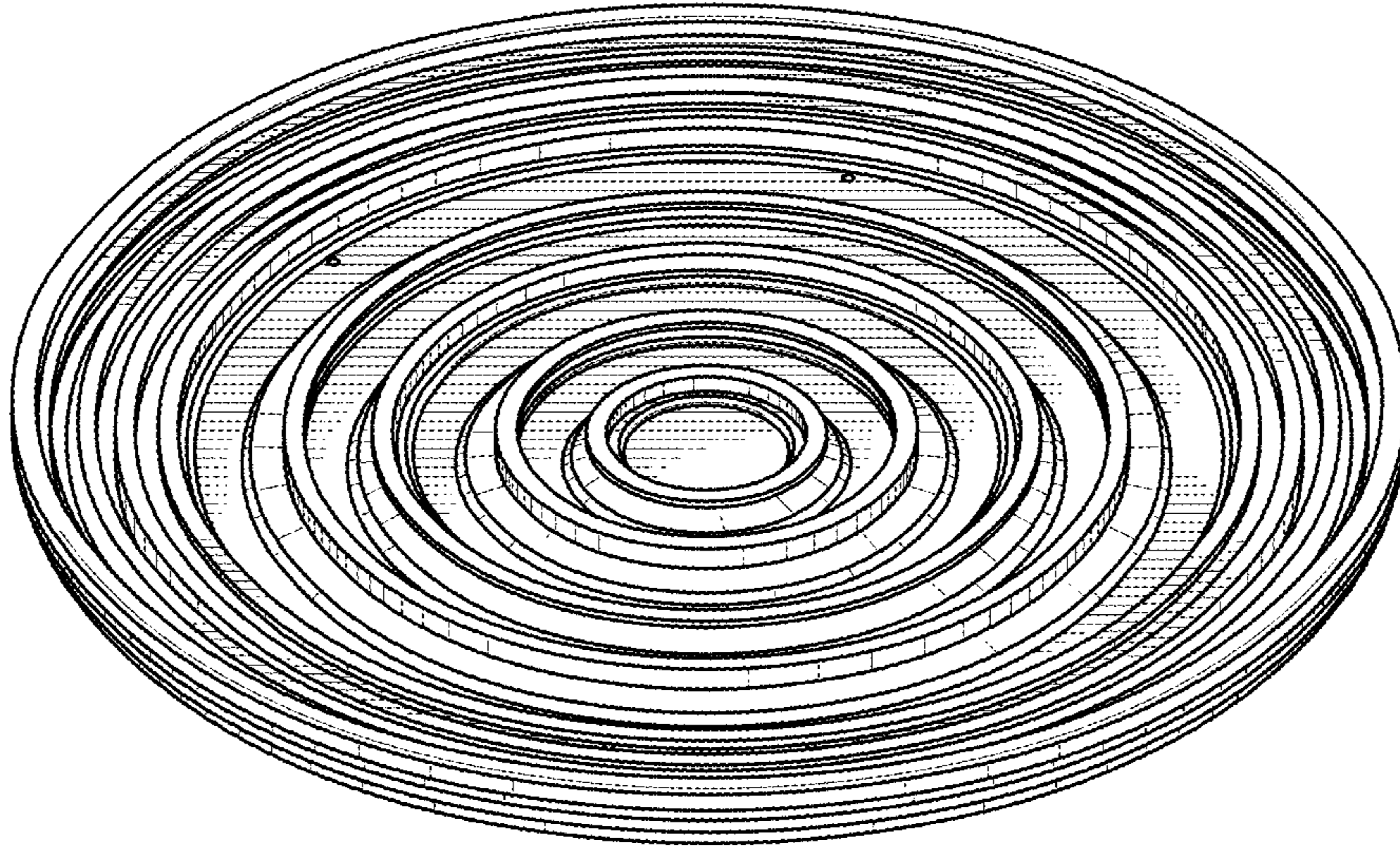


FIG. 9

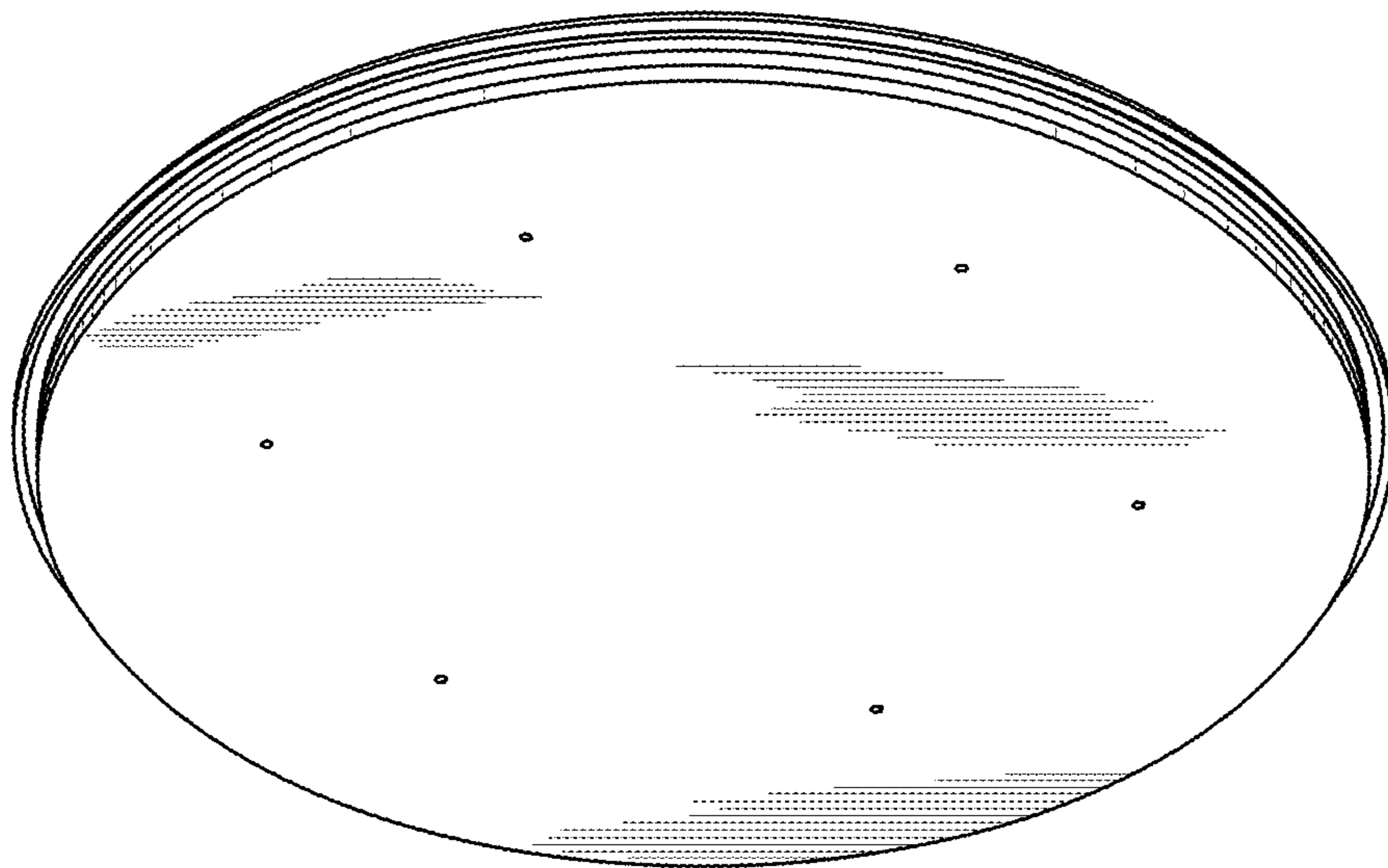


FIG. 10

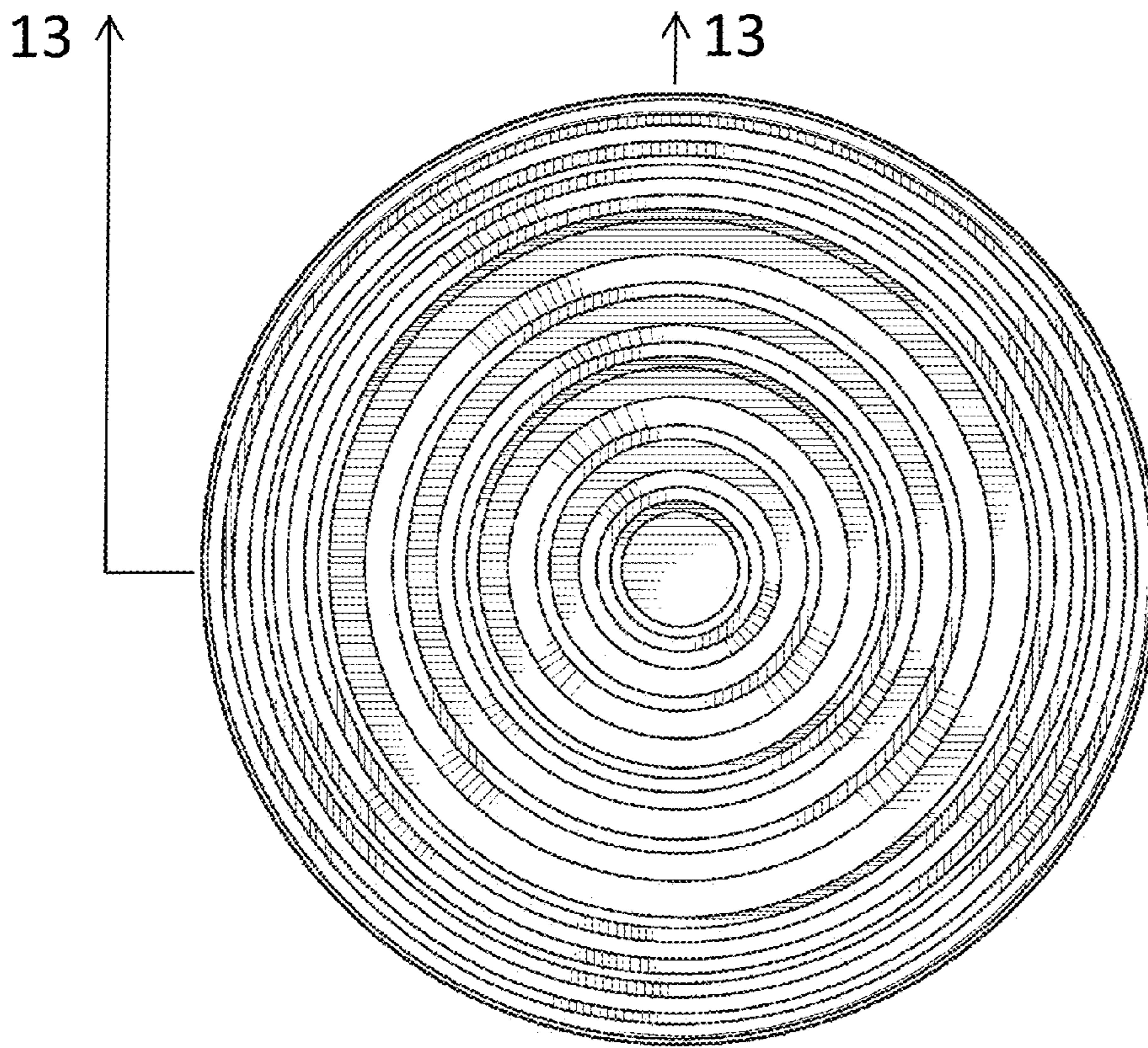


FIG. 11

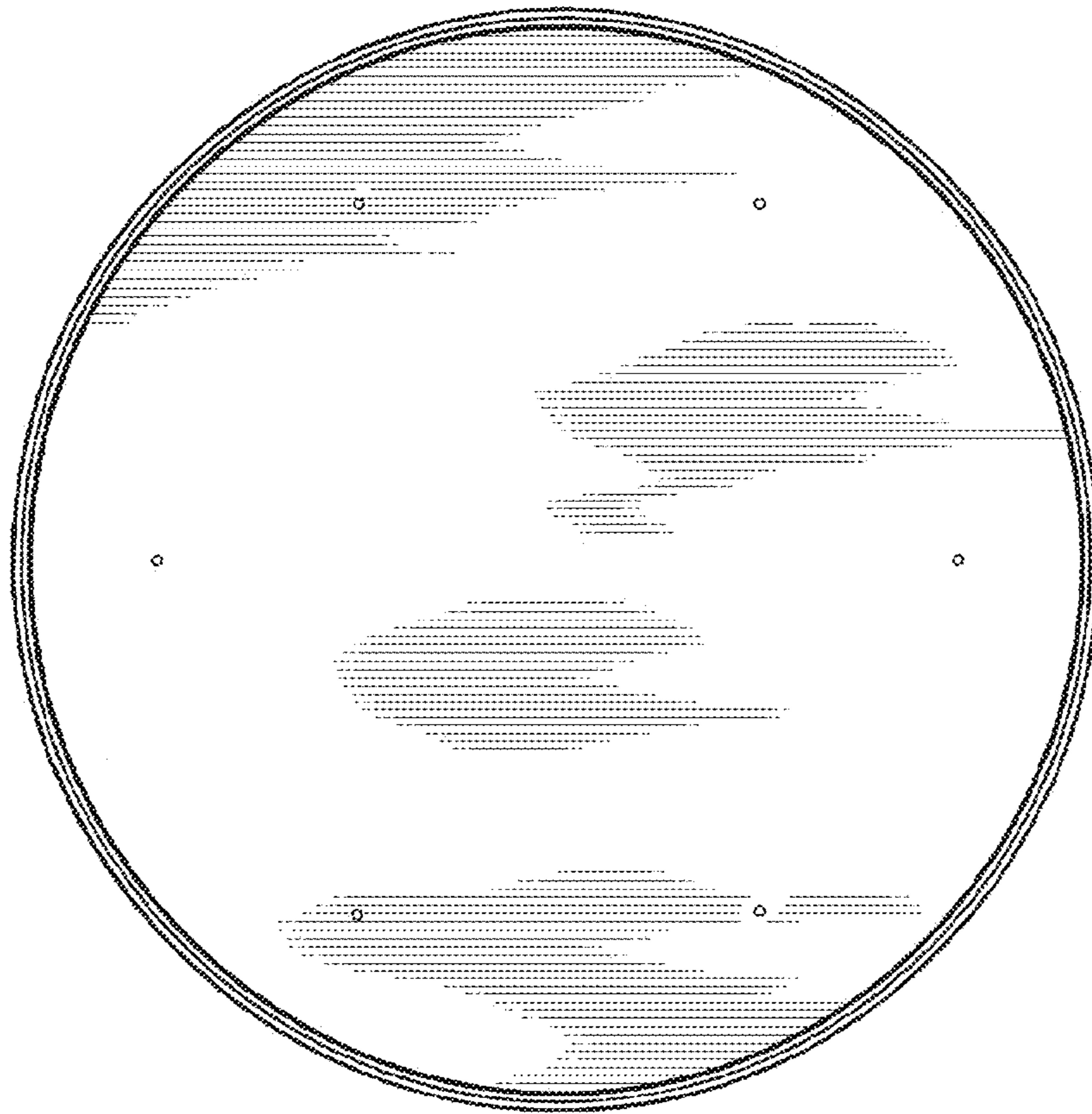


FIG. 12



FIG. 13

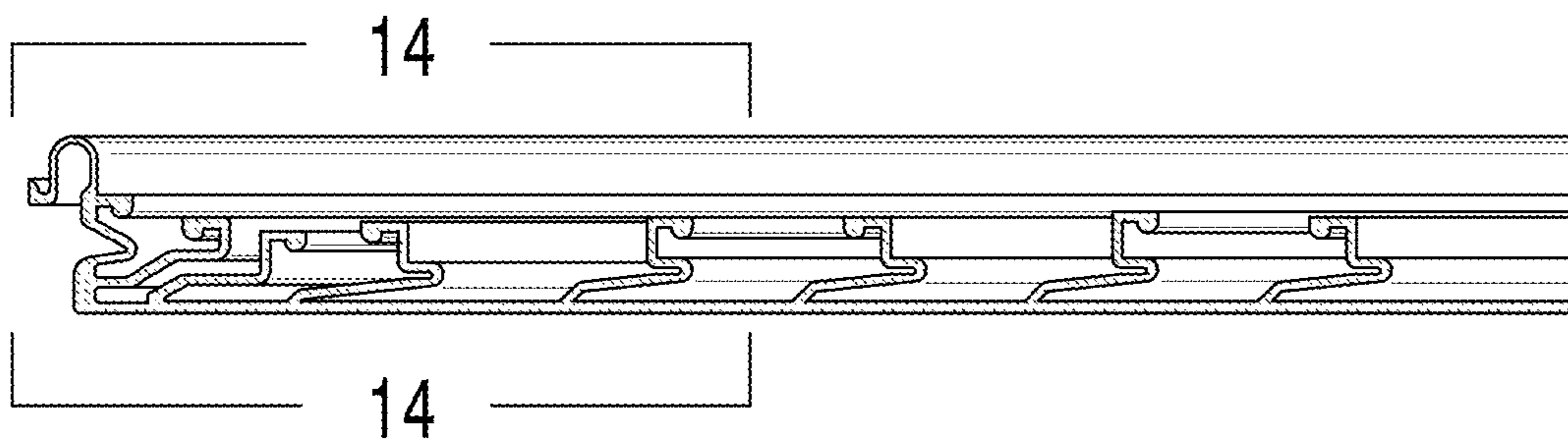


FIG. 14

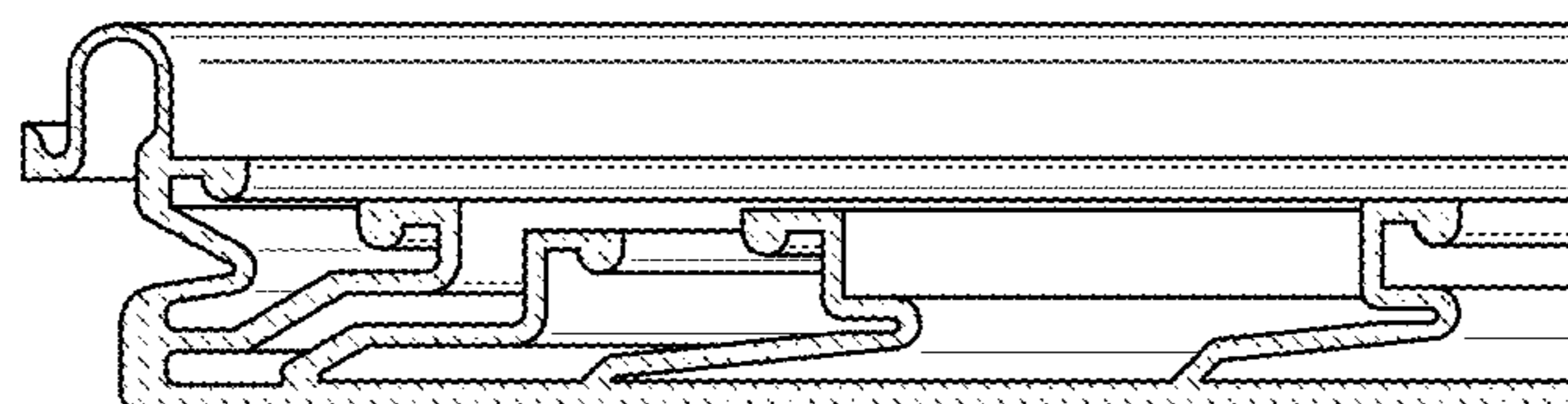


FIG. 15

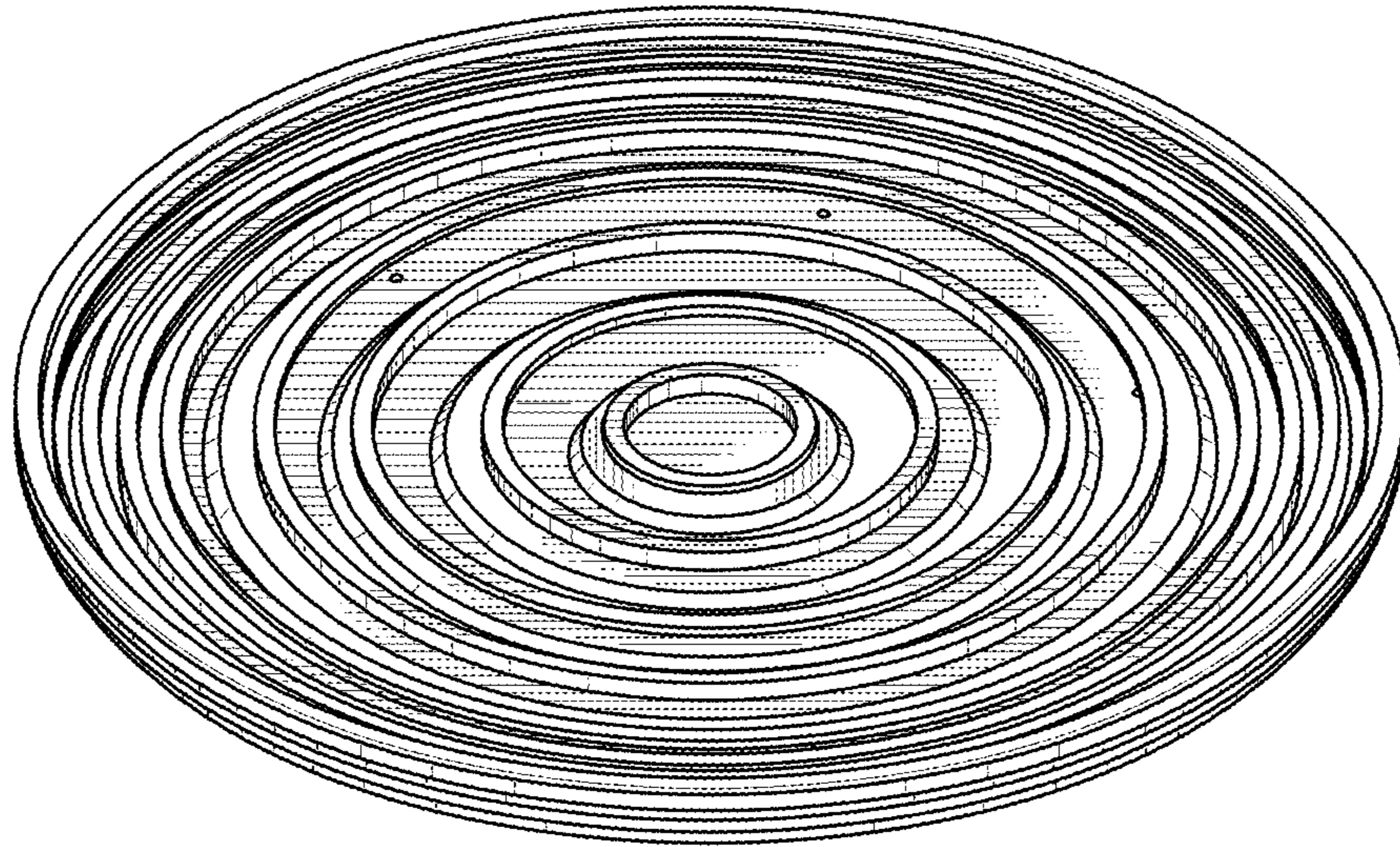


FIG. 16

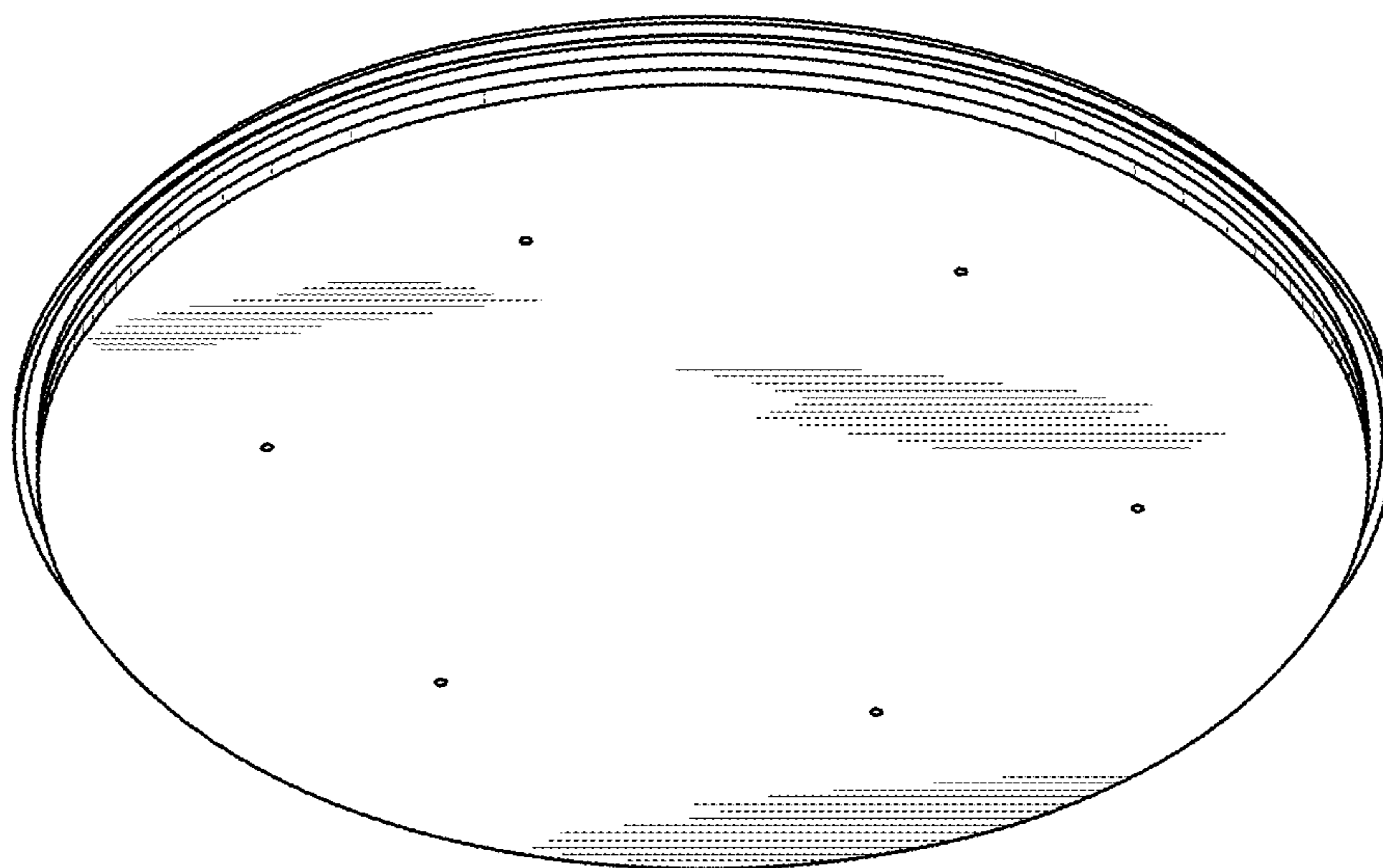


FIG. 17

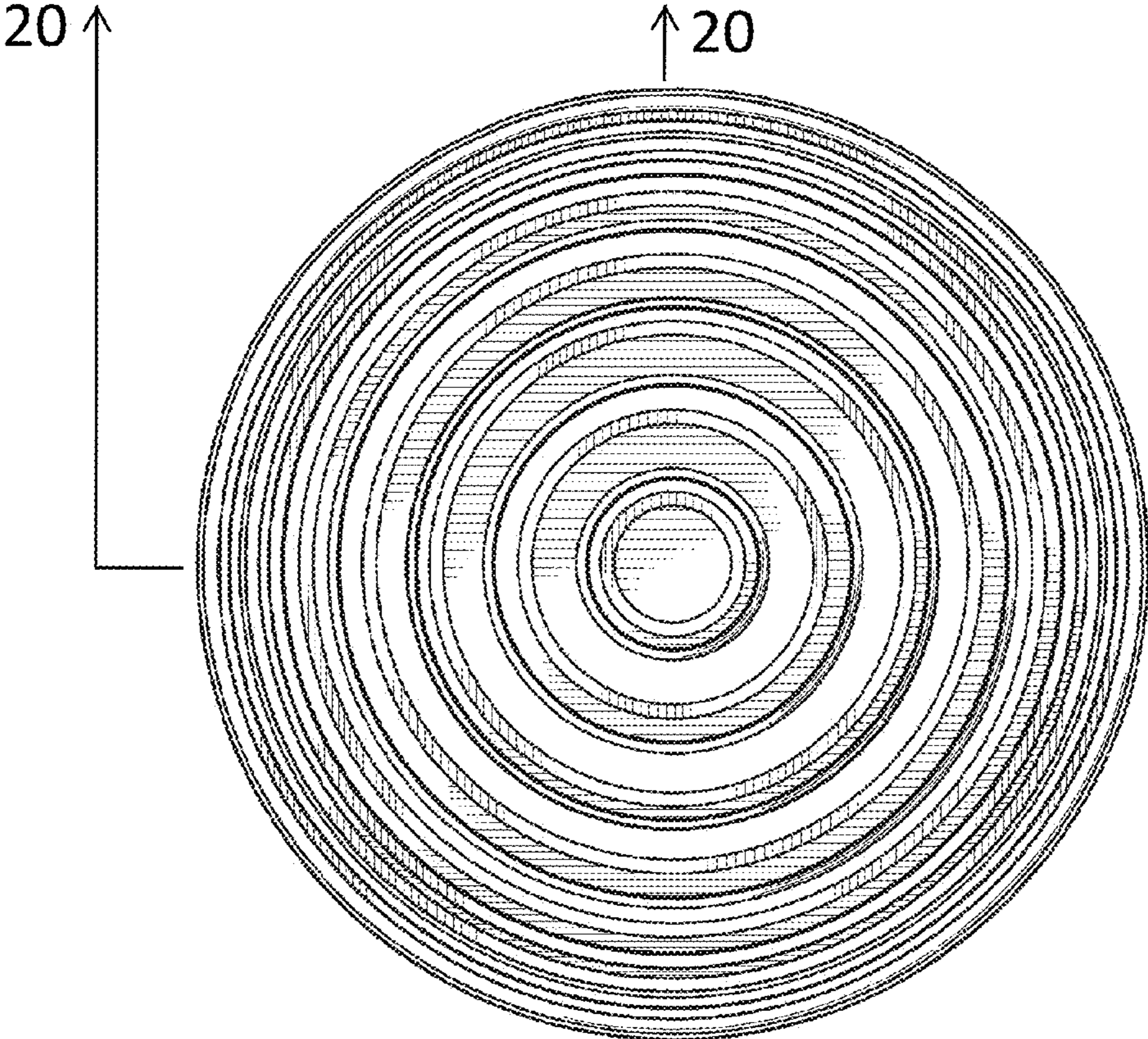


FIG. 18

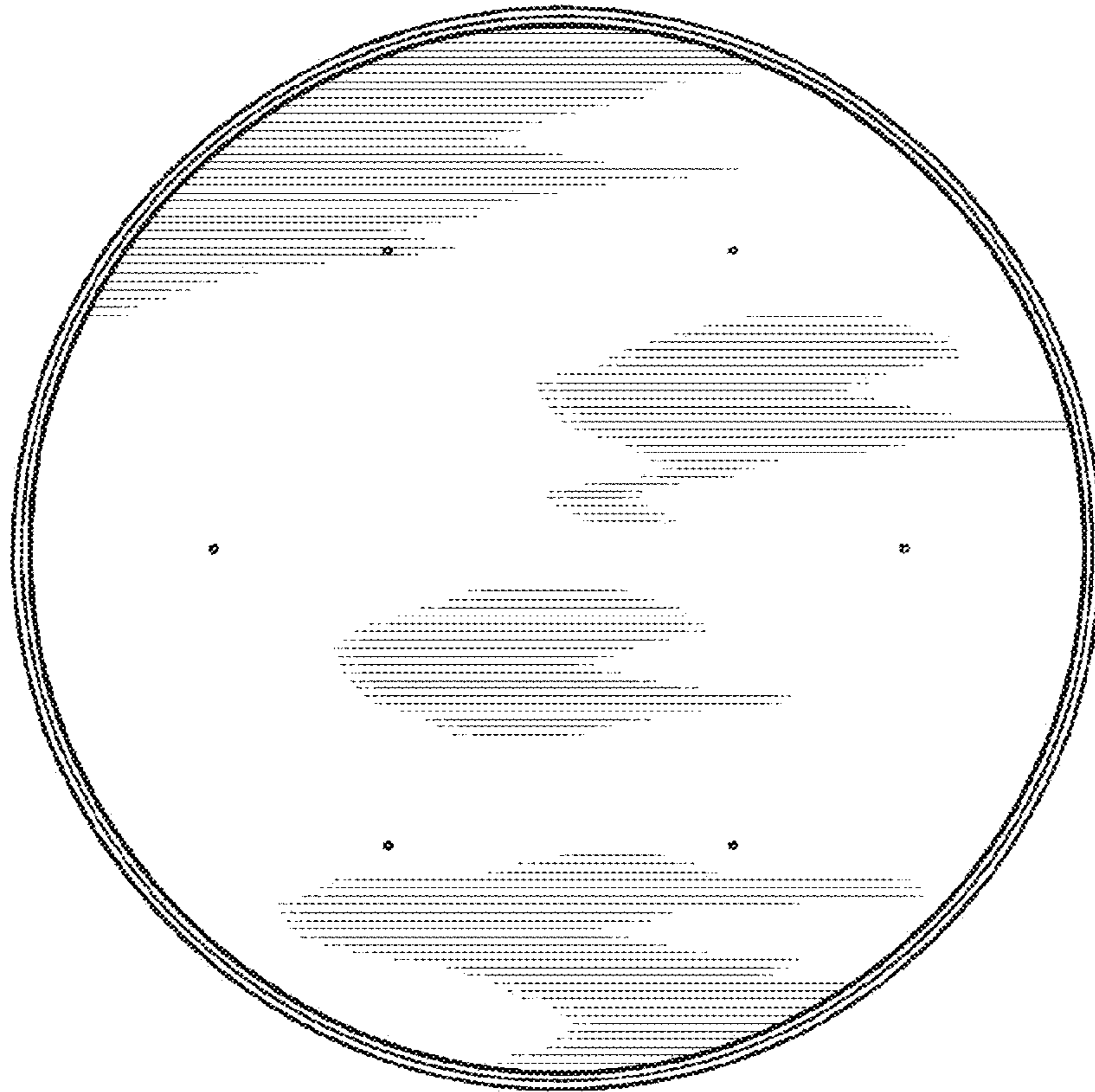


FIG. 19



FIG. 20

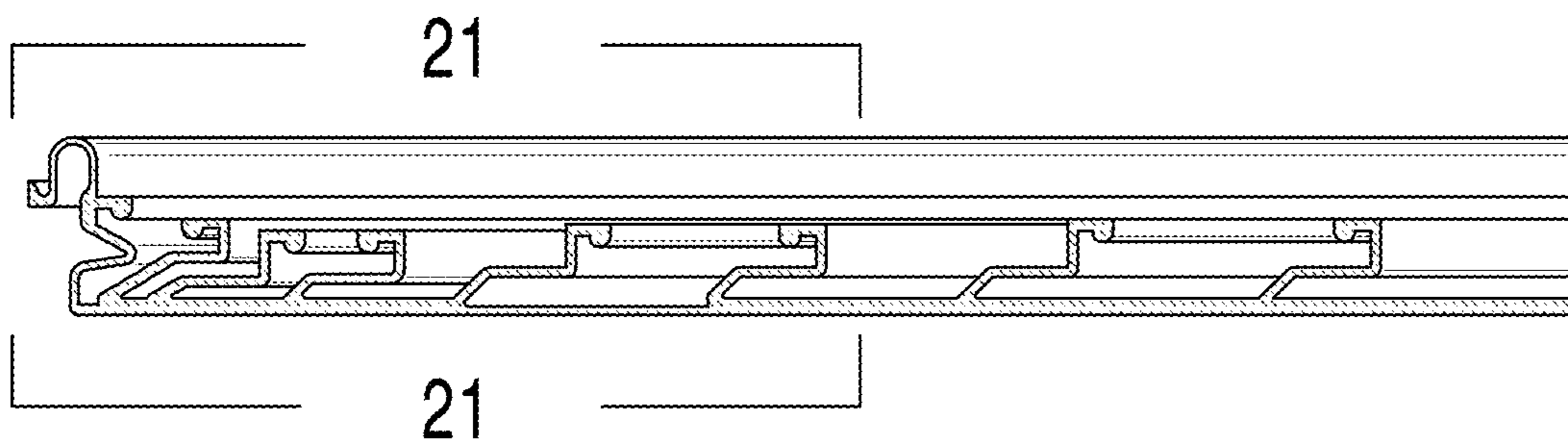


FIG. 21

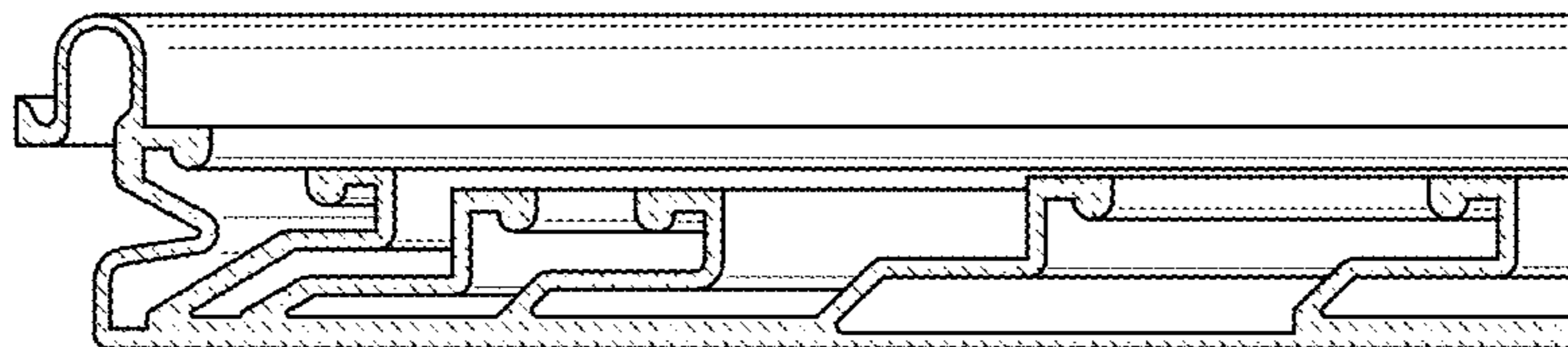


FIG. 22

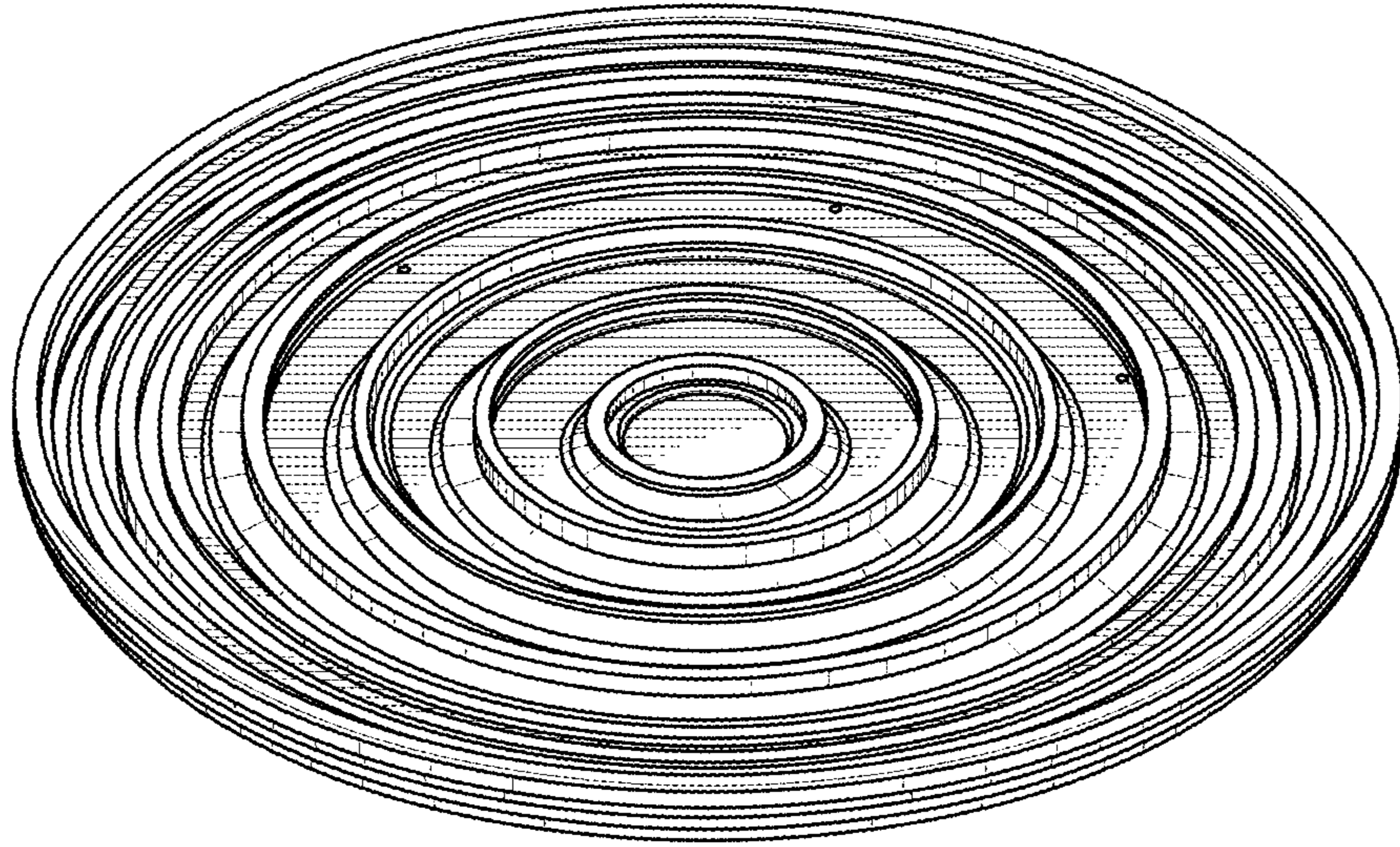


FIG. 23

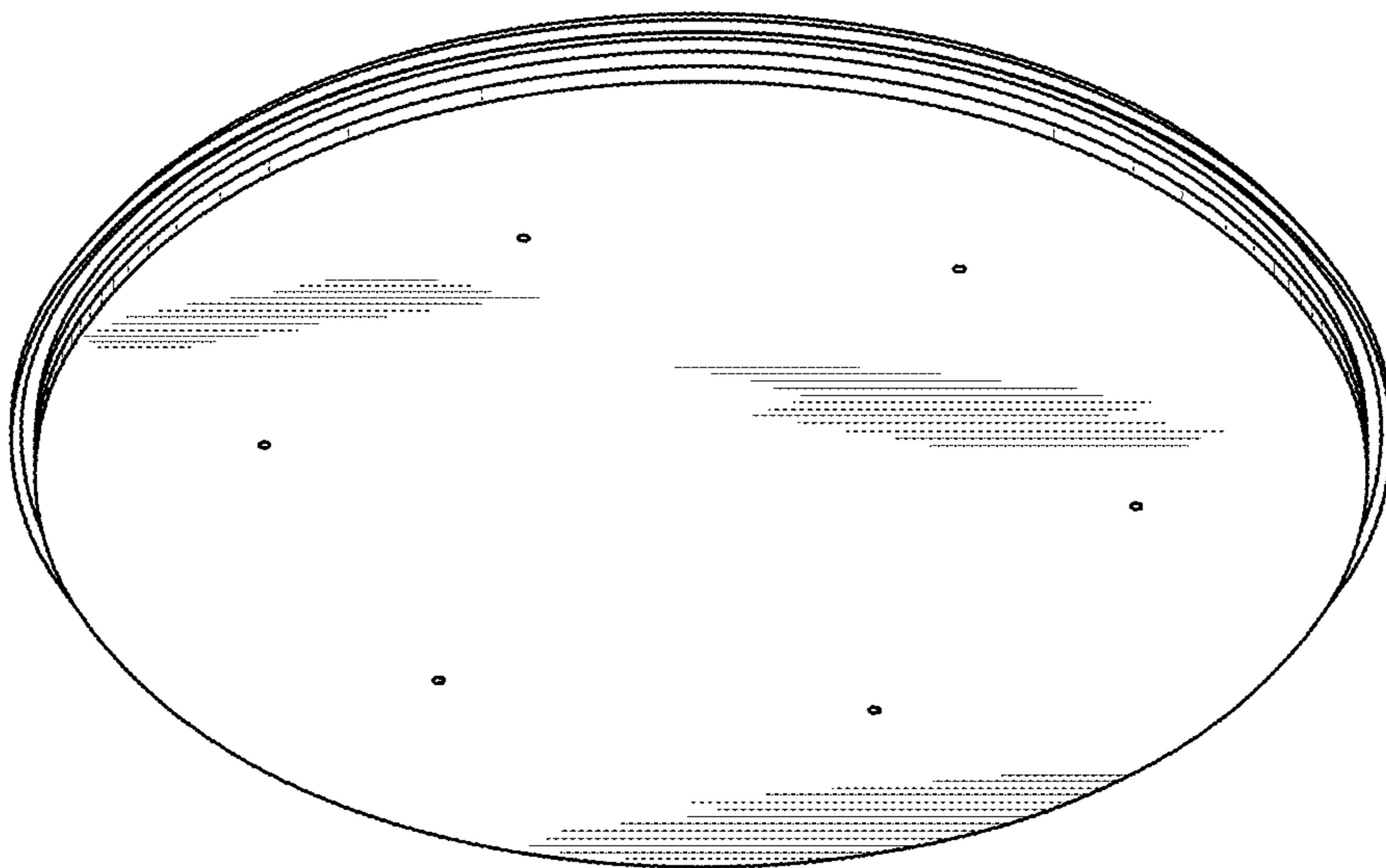


FIG. 24

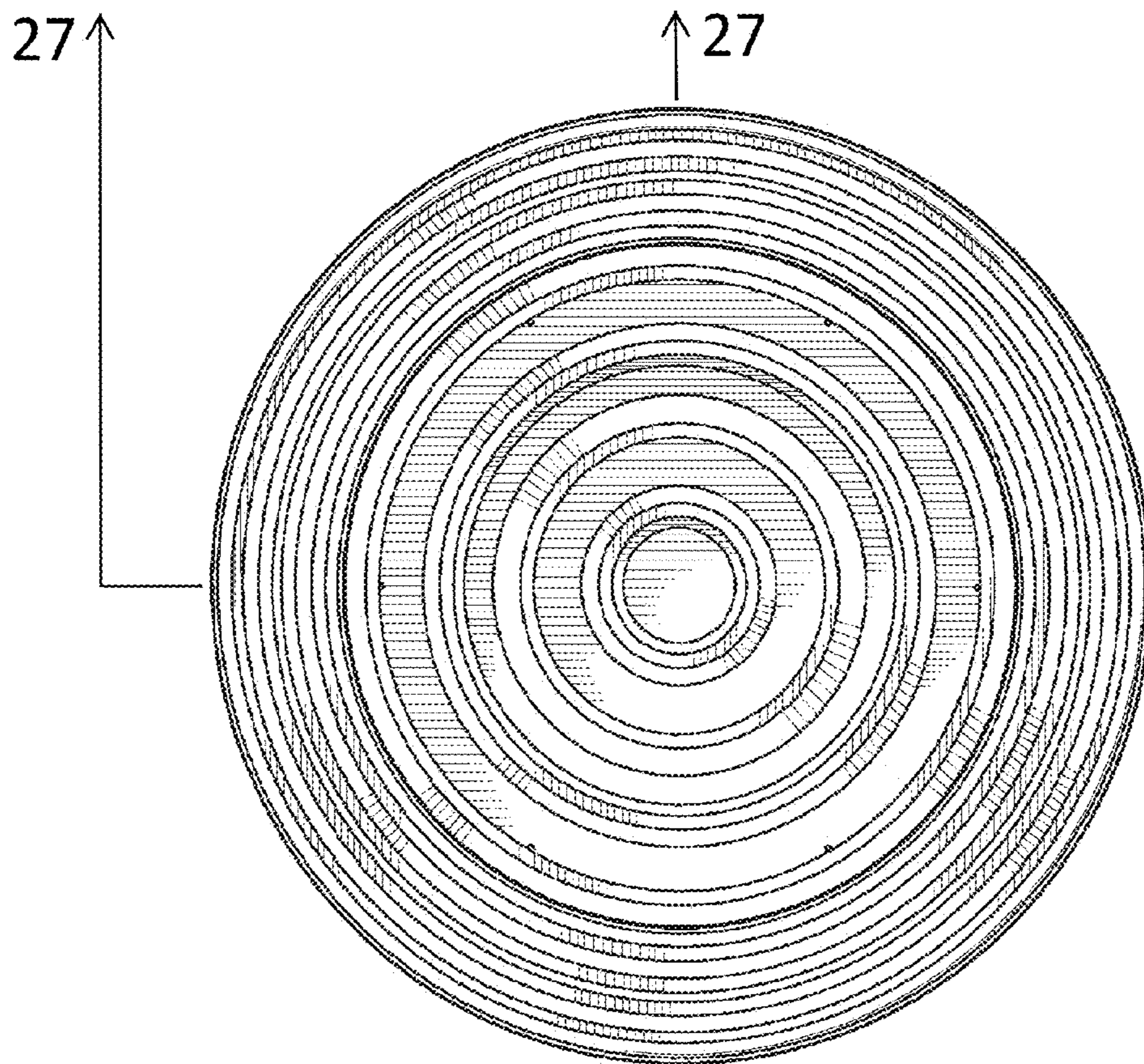


FIG. 25

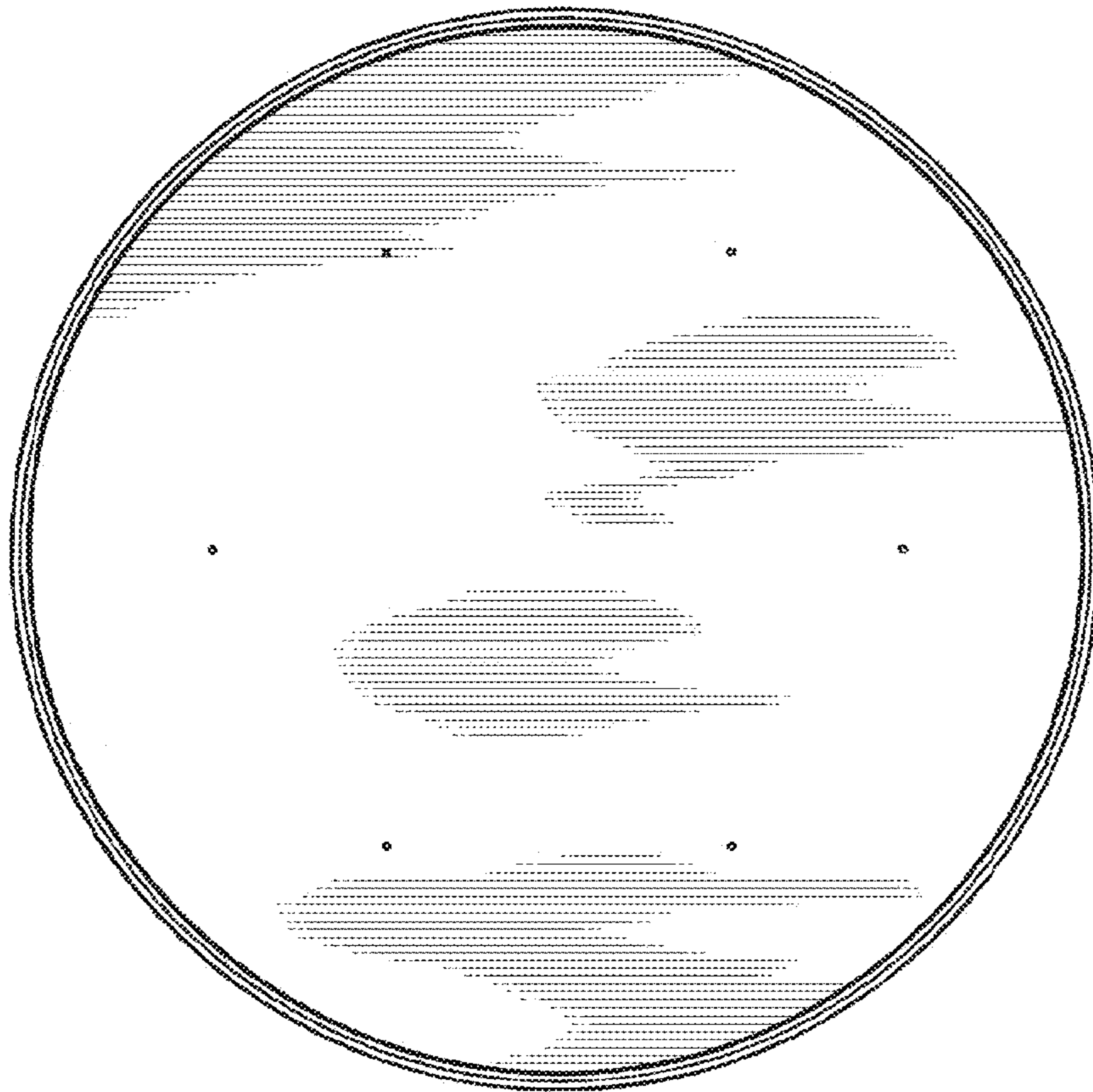


FIG. 26



FIG. 27

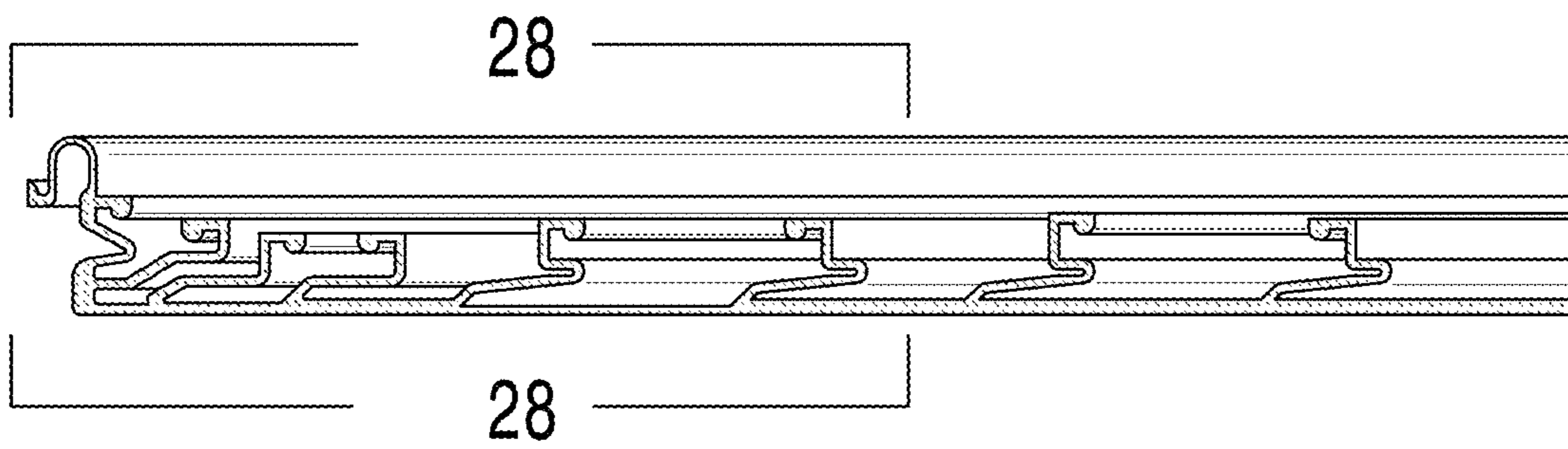


FIG. 28

